ANALYSIS, OPTIMIZATION, AND PRACTICAL DESIGN OF A SPLIT-PHASE DICKSON SWITCHED CAPACITOR CONVERTER FOR HIGH CURRENT APPLICATIONS

by

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Abstract

The Switched-Capacitor Converter (SCC) topology has been gaining attention from researchers because of their advantages of higher power density, better switch utilization, and low component stress. However, SCCs have a fundamental downside in which capacitor charge redistribution causes significant current spikes. This can be solved using as split-phase control, which addresses charge redistribution in the Dickson SCC by controlling the charging and discharging of the flying capacitors, such that the equivalent branch voltages line up when switching occurs.

In adapting the split-phase Dickson SCC topology for high-current applications, two significant sensitivities of split-phase control were identified. Differences between the actual values of the flying capacitors results in split-phase control not fully compensating for charge redistribution, due to the capacitors' uneven charge and discharge rates. Furthermore, input voltage ripple tends to cascade into the circuit, leading to voltage imbalance within the circuit.

To minimize capacitor mismatch and factoring in the problem of ceramic capacitor de-rating, the flying capacitors of the split-phase Dickson SCC were designed by referring to capacitor de-rating curves supplied by component suppliers. However, potential inaccuracies in the curves, combined with typical manufacturing tolerances of ±20%, led to the development of an in-circuit flying capacitor measurement method to allow for possible tuning of the flying capacitors.

The sensitivity of the Dickson SCC to input voltage ripple was initially bypassed by using a very large input capacitor to suppress input voltage ripple. However, this resulted in additional losses due to the equivalent resistance of the electrolytic capacitor that was

used. As such, an input voltage compensation method, which adjusts the duty cycles of the ‘split-phase’ switches to compensate for the additional voltage difference resulting from input voltage ripple interference, was developed.

The research presented in this thesis provides in-depth analyses of both sensitivities of the split-phase Dickson converter, as well as a discussion on their impacts on the design of components for the high-current split-phase Dickson SCC. Test results of a 48 V to 12 V, 35 A split-phase Dickson SCC prototype are also presented and discussed.

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D	Duty Cycle
f_{SW}	Switching Frequency
I_{IN}	Input Current
I_{OUT}	Output Current
N	Conversion ratio of power converter (N-to-1)
$R_{DS(on)}$	MOSFET on-resistance
R_{ESR}	Capacitor Equivalent Series Resistance
$R_{Winding}$	Inductor Winding Resistance
V_{IN}	Input Voltage
V_{OUT}	Output Voltage

Chapter 1

Introduction

1.1 Background

The field of Power Electronics is primarily concerned with the conversion and control of electrical power. For reasons of efficiency and ease of design, electrical power is often transmitted at voltage levels that are different to requirements at the consumer end. As such, power converters are necessary to step down, step up, or change the form of the transmitted electrical power to a level/form usable by the consumer-end loads. Common examples of such infrastructure are high-voltage AC transmission and data center bus architectures. Typical design considerations of power electronic circuits include efficiency, size, and cost.

1.1.1 Data Centers and Power Consumption

Data centers are one of the most energy intensive applications of electrical power to date [1]. Because they are concerned with the collection, storage, and manipulation of large amounts of data, they must operate 24 hours a day, every day of the year. This requirement to run 24/7 all year round not only consumes a substantial amount of power in itself, but it also creates the need for energy management, such as cooling systems, which further increases the amount of power consumed by data centers. Worldwide, the power consumed by data centers reached 269 TWh in 2012 [2]. Total power consumption by data centers is expected to continue growing exponentially with the increasing popularity of cloud storage and advances in information technology.

To reduce the energy consumption of data centers, many organizations have been working on improving the power architecture within them to allow for improved efficiency. The 48-volt power architecture, developed by Google, promises a 16x reduction in power distribution losses, as well as up to 30% reductions in power conversion losses compared to the existing 12-volt power architecture [1] [3] [4] [5]. However, for these improvements to be fully realized, better voltage conversion technologies are necessary to bridge the gap between the 48-volt power architecture and the existing 12-volt architecture [1].

Typically, power conversion within data centers is carried out using inductor-based pulse-width modulated (PWM) DC-DC converters. These power converters perform voltage conversion using single (or a pair of) switches, coupled with a low pass filter at the output. PWM converters have conversion ratios based on the length of time the switch is conducting. In voltage step-down applications, the most popular converter topology is presently the Buck converter, consisting of a pair of complementary switches and an LC filter at the output (Figure 1). A step-down (buck) PWM converter has a conversion ratio equation as defined in Equation 1.

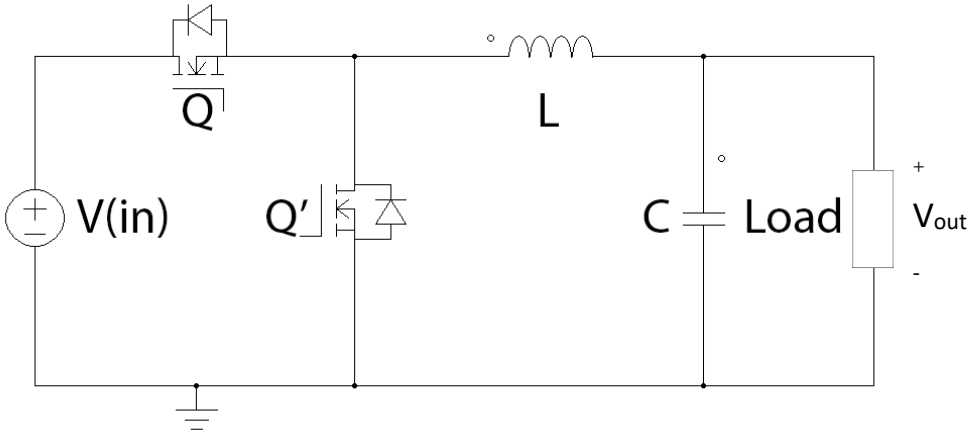

Figure 1: Circuit Schematic of Buck Converter

$$\frac{V_{out}}{V_{in}} = D \tag{1}$$

Where D represents the percentage of a switching period where the switch conducts (the duty cycle of the switch). For a 48 V to 12 V step-down application, referring to Equation 1, the duty cycle of the switch would be 25%. This represents a low utilization of the switch in the power converter. Concerning the high current loads in data centers, large passive components would need to be used for PWM converters. The use of these large components not only decreases the efficiency of the power converter, but also drastically increases the size of the circuit. The typical power density of PWM power converters is between 50 to 200 W/in^3 [6] [7], a low figure. Furthermore, components used for PWM-based power converters generally need to withstand high voltage and current stress. Utilizing components suitable for these voltage and current stresses further increases the size of the circuit, reduces performance, and drives up costs. The low power density and poor switch utilization of PWM converters would therefore not allow the 48-volt power architecture to fully realize its benefits.

1.1.2 Switched Capacitor Converters

A Switched-Capacitor Converter (SCC) is a non-isolated DC-DC converter topology that uses a network of switches and flying capacitors to perform voltage conversion. SCCs perform voltage conversion by using the principle of capacitive voltage dividers. The flying capacitors' voltage levels are kept constant throughout operation, and its switches rearrange the configuration of the flying capacitors throughout the switching cycle, effectively 'pumping' charge through the circuit. Unlike PWM voltage converters, the conversion ratio of SCCs is determined by their physical configuration, rather than the duty

cycles of the switches [8]. They are therefore ideal in applications with a constant line/bus voltage, such as in server rooms in data centers. The switches in an SCC are usually kept at constant duty cycles of 50%, leading to better switch utilization [9], as well as simplifying the control circuitry. Furthermore, unlike PWM converters, where switches must be able to block the entire input-output voltage difference (or sometimes more in buck-boost applications), the switches within SCCs only need to block voltages equal to the differences in voltage between flying capacitors, leading to an overall reduction in component stress compared to PWM power converters [10] [11] [12] [13] [14]. Passive components within a switched-capacitor converter are typically smaller in size than in PWM converters, thanks to reduced voltage stress. This, combined with a reduced reliance on magnetic components [15] [16], leads to a reduction in both the losses and size of the power converter, with a corresponding increase in the converter's power density [16] [17]. Because of their advantages of higher power density, better switch utilization, reduced component stress and losses, and simple control, the SCC topology has the potential to allow the improved data center power architectures to achieve their full benefits of loss reductions. As such, SCC topologies have, in recent years, been a considerable topic of interest for researchers [18] [19]. However, as will be discussed later, most current implementations of the switched-capacitor converter have been in low-current applications. Therefore, an analysis of new methods of control, as well as practical implications regarding high power, high current operations, must be performed to adapt the switched-capacitor converter for implementations beyond low-power applications.

1.2 Thesis Objectives

The objective of this thesis is to adapt the switched-capacitor DC-DC converter for a high current (>20 A) 48 V to 12 V step-down application with power levels appropriate for implementation in data centers. For this investigation, the Dickson-type switched-capacitor converter was the chosen topology to adapt for high-current loads. The benefits of smaller components, better switch utilization, simple control, and higher power density promised by the switched-capacitor converter, compared with existing PWM converters, would allow for efficiency improvements and space savings within data centers, if the implementation is successful.

As will be discussed in literature review, a major problem would need to be addressed to enable the switched-capacitor converter to be implemented in high current applications. SCCs suffer from the problem of current spikes due to charge redistribution, which not only cause significant switching and conduction losses in the converter, but could also result in the damage/destruction of circuit components, especially if it occurs in high-current applications. Charge redistribution is the main reason why most current implementations for SCCs have been in low-power, low-current applications. Methods to mitigate/eliminate charge redistribution will be discussed in literature review.

1.3 Thesis Outline

This thesis consists of six chapters:

Chapter 1 introduces the topic of power electronics, discussions on server room power architectures and methods to bridge the emerging 48-volt power architecture with the existing 12-volt architecture, as well as the motivations behind the research.

Chapter 2 provides in-depth discussions on the Dickson-type switched capacitor converter (the selected topology for implementation in high-current applications), as well as an analysis of charge redistribution and why this is a significant operational drawback in SCCs. A method of eliminating charge redistribution in the Dickson SCC, split-phase control, is introduced and discussed. Finally, this chapter provides a review of existing implementations of both the conventional Dickson SCC and the split-phase Dickson SCC.

Chapter 3 provides an analysis of the behavior of the split-phase Dickson SCC in the presence of various practical scenarios which may result in split-phase control not fully compensating for charge redistribution, such as input voltage ripple and flying capacitor mismatch. This analysis was performed because split-phase control has never been implemented in high-current applications prior to the current research. Sensitivities of this topology that are not of concern in low-power/low current applications may have significant impacts as the handled power increases, especially at high current loads.

Chapter 4 describes the design of hardware components for the prototypes of the 48 V to 12 V, 35 A split-phase Dickson converter. Measures to mitigate the sensitivities identified in Chapter 3 are discussed. In particular, the issue of flying capacitor matching in practical scenarios is discussed. The derivation of an in-circuit flying capacitor size estimation method is discussed. This chapter also describes the selection of other components, as well as the design of the circuit boards for the prototypes.

Chapter 5 discusses the performance of the 48 V to 12 V, 35 A split-phase Dickson converter prototype. The efficiency curve, loss breakdown, and temperature profile of the prototype are presented. The derivation and analysis of a control method to eliminate the sensitivity of input voltage ripple in the split-phase Dickson SCC is discussed. Finally,

simulation results of a two-circuit phase interleaved split-phase Dickson SCC configuration are presented and discussed.

Chapter 6 provides a summary and a conclusion to the thesis and discusses any future work to be completed on this subject.

Chapter 2

Background and Literature Review

This chapter provides an overview of the Dickson Switched-Capacitor topology, as well as the standard two-phase operation principle of the Dickson SCC. A discussion of the principle and impacts of charge redistribution is also presented in this chapter. Furthermore, examples of current implementations of the Dickson SCC are reviewed. Finally, this chapter discusses split-phase control, a switch control method that provides compensation to the problem of charge redistribution, by imposing voltage control on the Dickson SCC's flying capacitors.

2.1 The Dickson Switched Capacitor Converter – Overview and Two-phase control

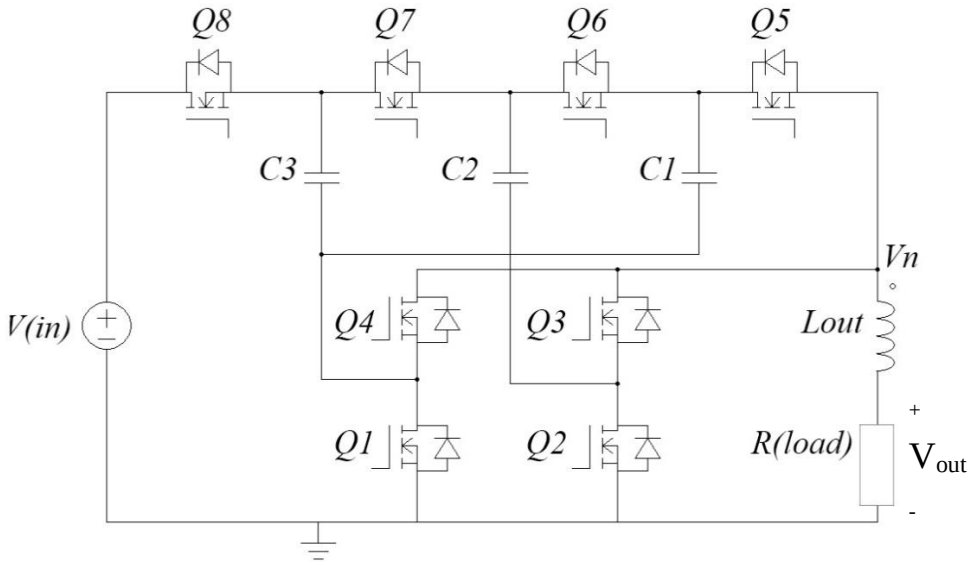

Figure 2: Circuit schematic of a 4-to-1 Dickson SC converter

Figure 2 shows the schematic of a Dickson switched-capacitor converter with a conversion ratio of 4 to 1. The output voltage of the 4-to-1 Dickson SCC is ¼ of the input voltage to the circuit. This conversion ratio is fixed by the circuit's configuration [8]. In a

4-to-1 Dickson converter at steady-state operation, flying capacitors C3, C2, and C1 each retain voltages of $3V_O$, $2V_O$, and V_O, respectively. These capacitors are pre-charged to these voltages during startup. As can be seen in the schematic, a small inductor (generally between 100 nH and 1 µH) can be added ahead of the load to smooth out the output current.

Traditionally, the Dickson switched-capacitor converter operates with two circuit states per switching cycle; referred to as two-phase operation. In two-phase operation, for the 4-to-1 Dickson SCC shown in Figure 1, all 8 switches have duty cycles of 50%; that is, each switch conducts current for exactly half of the switching cycle. Switches Q8, Q6, Q4, and Q2 are conducting, or 'on', in the first half of the switching cycle (Phase 1), with the remaining four switches remaining off during this phase. In the second half of the switching cycle (Phase 2), switches Q7, Q5, Q3, and Q1 are conducting, with the remaining switches switched off during this phase. The switching order of the two-phase Dickson SCC's switches is illustrated in the schematic diagram in Figure 3.

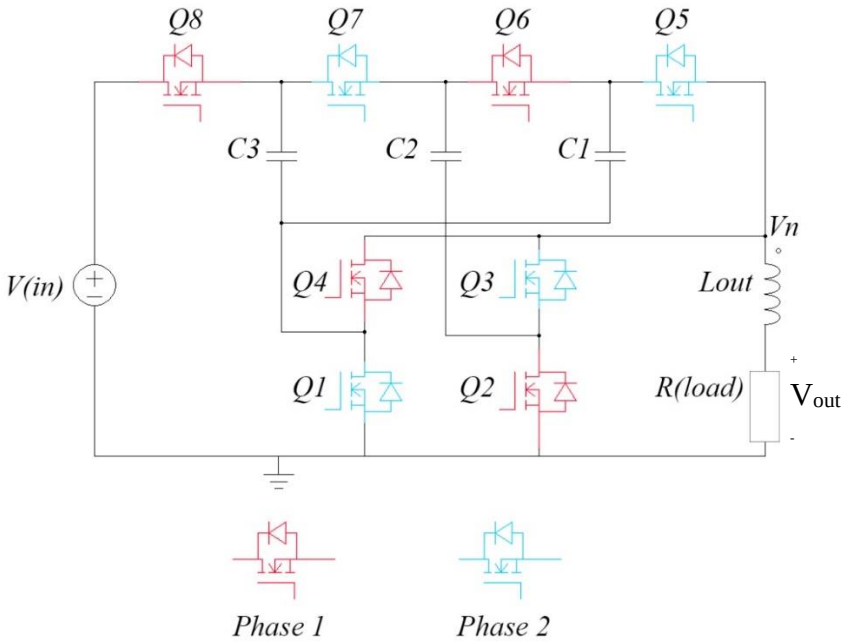

Figure 3: Circuit schematic of 4-to-1 Dickson SCC, with switching order illustrated

The operation of the switches in the order described above results in two equivalent circuits for the two-phase 4-to-1 Dickson SCC. In Phase 1, the input source is connected through switch Q8 in series with flying capacitor C3, which itself is connected through Q4 to the output node (labelled as V_n in Figure 2), forming one branch of the Phase 1 equivalent circuit. Flying capacitor C2 is connected between ground (via switch Q2) and capacitor C1 (via switch Q6), with C1 also connected to the output node, V_n through switch Q4, forming the second branch of the Phase 1 equivalent circuit. During Phase 1, the input source charges capacitor C3, while capacitor C2 charges capacitor C1. For the switches that are not conducting during Phase 1, Q7 blocks voltage equal to the voltage difference between the input source and the voltage of capacitor C2 ($V_{Q7} = V_{IN} - 2V_O = 2V_O$), Q5 and Q3 blocks voltage equal to the difference between the voltage of capacitor C2 and the load ($V_{Q5} = V_{Q3} = 2V_O - V_O = V_O$), and Q1 blocks voltage equal to the difference between the voltage of capacitor C1 and ground ($V_{Q1} = V_O$). Therefore, switch Q7 has a maximum voltage stress of $2V_O$, while switches Q5, Q3, and Q1 each have maximum voltage stresses equal to V_O.

The configuration of the 4-to-1 Dickson SCC circuit in Phase 1 is shown in Figure 4. The current paths and associated circuit components are highlighted in red with the direction of current flow illustrated with arrows. Switches not conducting during Phase 1 are shown as open circuits.

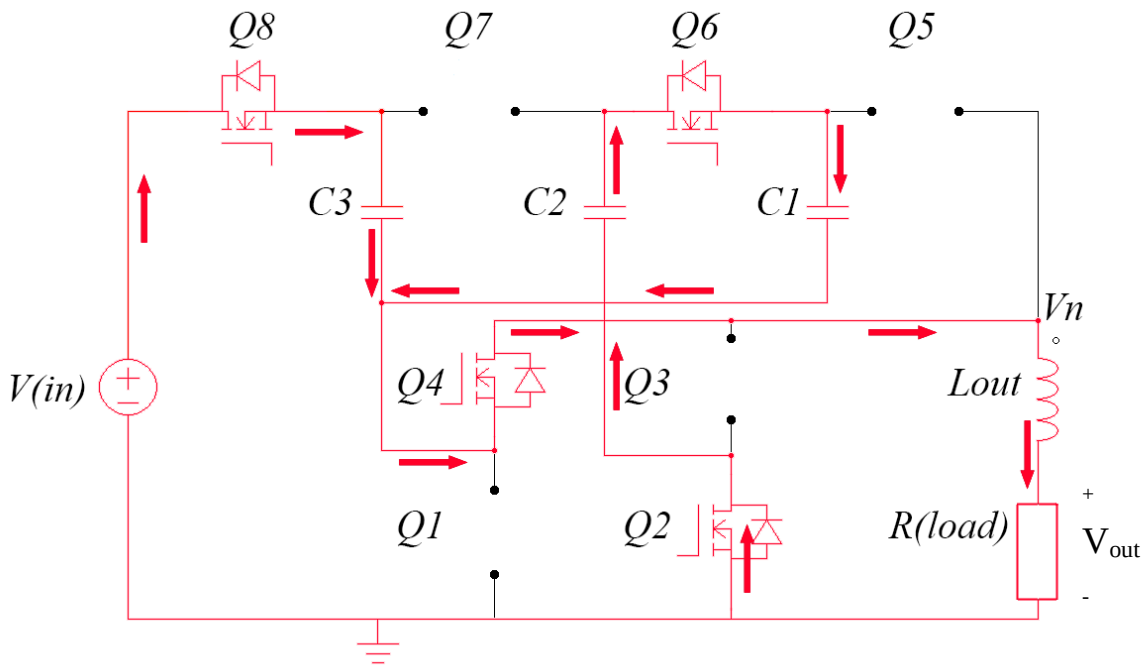

Figure 4: Circuit configuration of 4-to-1 Dickson SCC in Phase 1

In the Phase 2 equivalent circuit, C3 is connected to ground via switch Q1, and is also connected through switch Q7 in series with capacitor C2. C2 is itself connected through Q3 to the output node, forming one branch of the Phase 2 equivalent circuit. Capacitor C1 is connected between ground (via Q1) and the output node (via Q5), forming the second branch of the Phase 2 equivalent circuit. During Phase 2, capacitor C3 discharges into capacitor C2, while capacitor C1 discharges directly into the output. For the switches not conducting during Phase 2, Q8 blocks voltage equal to the difference between the input voltage source and the voltage of capacitor C3 ($V_{Q8} = V_{IN} – 3V_O = V_O$), Q6 blocks voltage equal to the voltage difference between capacitor C3 and C1 ($V_{Q6} = 3V_O – V_O = 2V_O$), and Q4 and Q2 blocks voltage equal to the difference between the output node and ground ($V_{Q4} = V_{Q2} = V_O$). Therefore, switch Q6 has a maximum voltage stress of $2V_O$, and switches Q8, Q4, and Q2 have maximum voltage stresses equal to V_O.

The configuration of the 4-to-1 Dickson SCC circuit in Phase 2 is shown in Figure 5. Current paths and associated components are highlighted in blue, with the direction of current flow illustrated with arrows. Switches not conducting during Phase 2 are shown as open circuits.

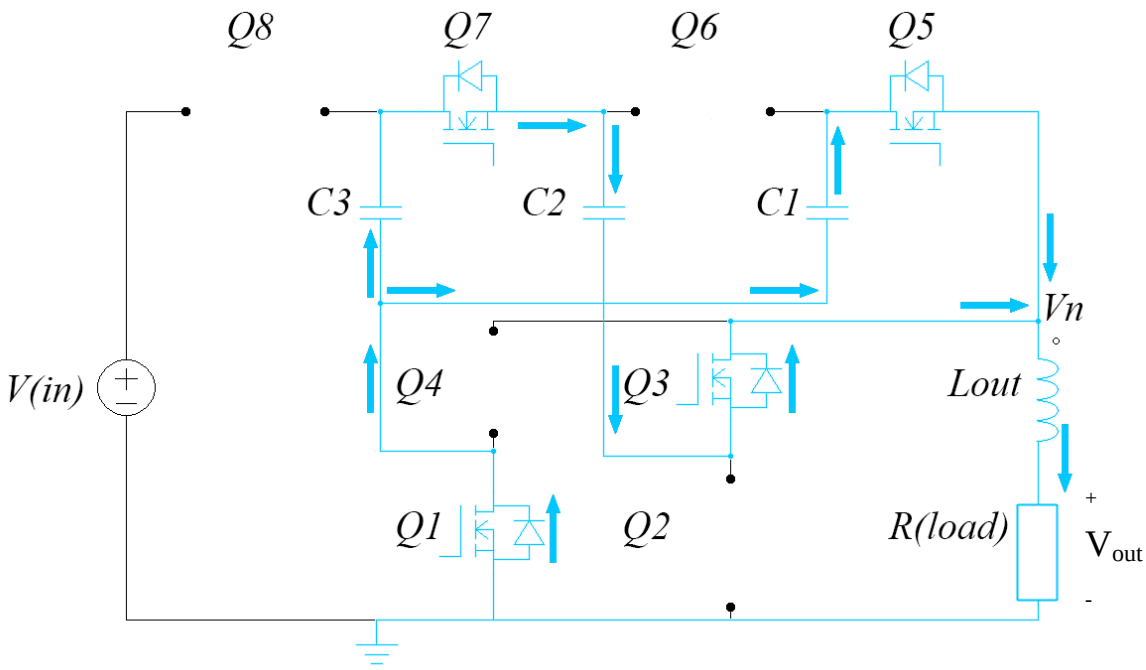

Figure 5: Circuit configuration of 4-to-1 Dickson SCC in Phase 2

The simplified two-phase equivalent circuits of the 4-to-1 Dickson converter, showing only the configurations of the flying capacitors, input source, and output load, are illustrated in the circuit diagram in Figure 6. These simplified diagrams are sourced from [20].

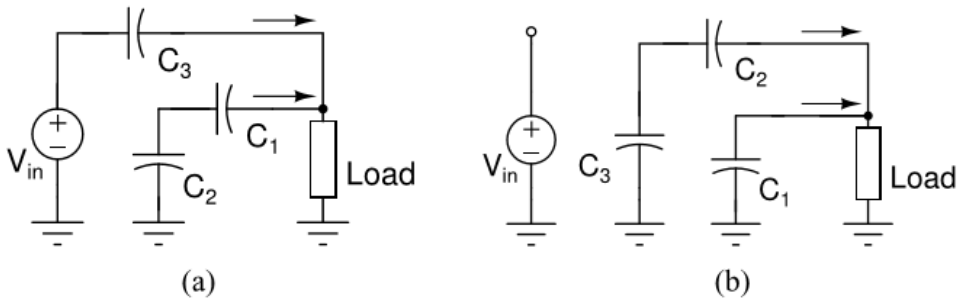

Figure 6: Simplified Two-phase operation equivalent circuit diagrams for Phase 1 (a) and Phase 2 (b) [20]

The operation of the switches as described above, along with the fixed voltages of the flying capacitors, result in the Dickson SCC operating much like a capacitive voltage divider, thus enabling voltage conversion. The charging and discharging over each switching cycle allow them to retain their average voltages, which are necessary to allow them to operate as voltage dividers. As described in the circuit phase descriptions, two of the circuit's switches, Q7 and Q6, have maximum blocking voltages of twice the output voltage, $2V_O$, while the other switches have maximum blocking voltages equal to the output voltage, V_O. Compared with the switch of a PWM-based buck converter, which would require a maximum blocking voltage equal to the input voltage (or $4V_O$) for a 4-to-1 voltage conversion ratio, the switches in the Dickson SCC experience far less voltage stress than the switches in a comparable PWM-based power converter.

For each circuit phase of the 4-to-1 Dickson SCC, due to the capacitive divider effect, the equivalent circuit branch with two flying capacitors always carries an average current equal to $1/3I_O$, while the equivalent circuit branch with a single flying capacitor always carries $2/3I_O$. Compared with PWM-based converters, where the maximum current through almost all circuit components is equal to the full load current, the components of the

Dickson SCC also experience overall less current stress than components in a comparable PWM power converter.

2.2 Charge Redistribution

As was discussed in the previous section, the Dickson switched-capacitor converter effectively uses the circuit's flying capacitors as voltage dividers to achieve voltage conversion. To maintain their functions as voltage dividers, the flying capacitors need to charge and discharge. This causes the voltages of the flying capacitors to exhibit voltage ripples. The voltage ripples of the flying capacitors cause problems whenever the circuit's state is rearranged; that is, whenever switching occurs. When two capacitors with different voltages are suddenly connected in parallel, charges between these two capacitors are rapidly redistributed between them so that their voltages are the same [21]. This phenomenon is called the Charge Redistribution mechanism [15] [21] [22], and incurs a 'charge redistribution' loss whenever this occurs [21]. Most significantly, the charge redistribution effect causes large current spikes through the two capacitors [23] [24]. The current spikes resulting from charge redistribution in SCCs contribute to significant switching and conduction losses within the converter [10] [11] [22] [25]. Moreover, especially in high-current applications, the magnitudes of the current spikes (and the resultant voltage noise) within the circuit may cause damage to circuit components of the SCC.

The conditions under which charge redistribution occurs applies to capacitive branches as well. For the 4-to-1 Dickson SCC topology previously discussed, charge redistribution occurs when there is a voltage difference between the two capacitive equivalent circuit branches, with respect to the output node V_n, prior to the circuit switching states to the

corresponding circuit phase. The equations for the voltage differences at the output node for the phase 1 and phase 2 equivalent circuits for the 4-to-1 Dickson SCC are shown in Equations 2 and 3, respectively

$$\Delta V_{n\,(Phase\ 1)} = (V_{IN} - V_{C3}) - (V_{C2} - V_{C1}) \quad (2)$$

$$\Delta V_{n\,(Phase\ 2)} = (V_{C3} - V_{C2}) - (V_{C1}) \quad (3)$$

As an example, during the transition from Phase 2 to Phase 1, if there is voltage difference between the Phase 1 equivalent circuit branch voltages when measured with respect to the output node (in Equation 2, when $\Delta V_{n\,(Phase\ 1)}$ is not zero when the circuit switches to Phase 1), then charge redistribution will occur.

To verify that charge redistribution is indeed a significant problem at high power/high current loads, the two-phase 4-to-1 Dickson SCC was simulated in the PSIM circuit simulation software using component parameters as listed in Table 1. The results of the simulation, shown in Figure 7, shows that the voltages of the equivalent circuit branches of the Dickson SCC are highly divergent when switching occurs, with an output node voltage difference of nearly 2 volts. The resultant current spikes due to charges redistributing after switching takes place have magnitudes of around 300 A, around 8.6 times the magnitude of the specified load current of 35 A.

Table 1: Simulation Parameters

SIMULATION PARAMETERS	
V_{IN}	48 V
V_{OUT}	12 V
I_{OUT}	35 A
C3, C2, C1	47 µF
C_{OUT}	47 µF
L_{OUT}	200 nH
f_{SW}	100 kHz
$R_{DS(on)}$	1 mΩ
R_{ESR}	1 mΩ
$R_{L(winding)}$	0.3 mΩ

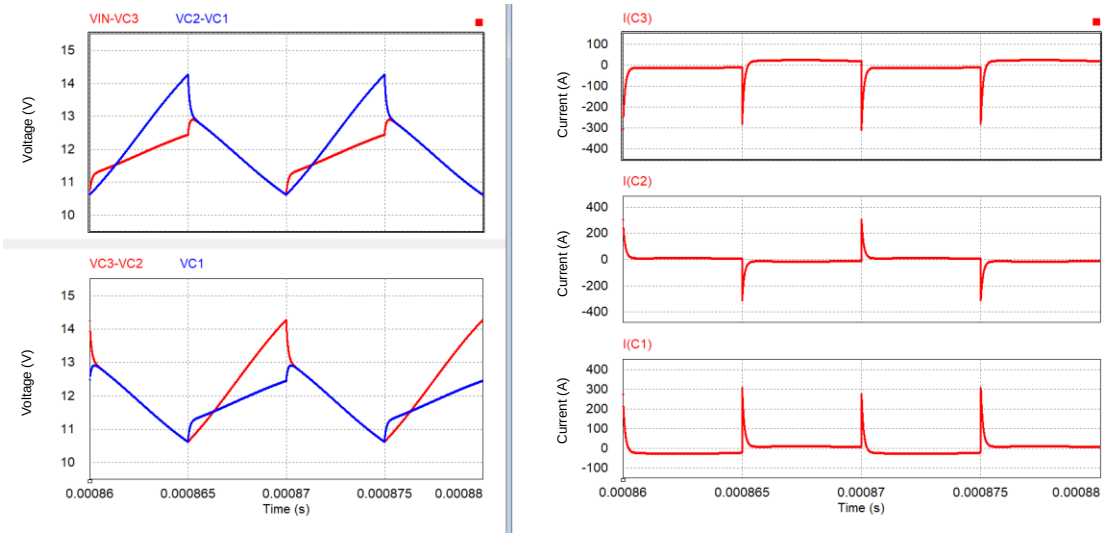

Figure 7: Simulated equivalent circuit branch voltage (left) and flying capacitor current (right) waveforms of two-phase 4-to-1 Dickson SCC

As discussed in [21], energy transfer between two similar components dissipates energy; when a capacitor is charged by a voltage source through a resistor with a constant voltage, it can be shown that the energy dissipated throughout the charging process is proportional to the size of the capacitor being charged, as well as the square of the difference in voltage between the charging source and the voltage across the resistor. The energy lost does not depend on the size of the resistor. This relationship is shown in Equation 4 [21].

$$E_R = \frac{1}{2} C (V_{DD} - V_R)^2 \quad (4)$$

Applying the above principle to two capacitors with unequal voltages suddenly being connected in parallel with each other, the above equation becomes the expression to calculate energy loss from charge redistribution. In this case, the charging voltage and the voltage of the 'resistor' are the initial voltages of the two capacitors, and the capacitance variable becomes the equivalent capacitance of the two capacitors when connected in parallel. The expression for the energy lost due to the charge redistribution effect is shown in Equation 5 [21].

$$E_{loss} = \frac{1}{2} (C_1 || C_2)(V_{C1} - V_{C2})^2 \quad (5)$$

As charge redistribution usually occurs within nanoseconds, the energy loss generated as a direct result of charge redistribution can contribute to significant power losses within the switched-capacitor converter.

The current spikes generated through the flying capacitors due to charge redistribution can also contribute to power loss, through increases in the switching and conduction losses within the MOSFET switches of the SCC. The equations to calculate switching and conduction loss through a MOSFET switch are shown below in Equations 6 and 7, respectively.

$$P_{(turn-on)} = \frac{1}{2} V_{ON} I_{ON} t_{ON} f_{sw} \quad (6)$$

$$P_{(conduction)} = I_{rms}^2 R_{ds(on)} \quad (7)$$

The equation to calculate the switch turn-on loss is shown in Equation 7. As can be seen, the turn-on switching loss is proportional to the switch voltage, the current through the

switch when it turns on, the turn-on time (rise time) of the switch, and the switching frequency of the switch. With current spikes of magnitudes of around 300 A through the switches at the time of switching, the magnitudes of the turn-on losses in the circuit would be massive. The equation to calculate conduction loss is shown in Equation 8 and is proportional to the square of the RMS current through the switch and the on-resistance of the switch. The current spikes due to charge redistribution contributes to an increase in the RMS current through the switch. Therefore, charge redistribution would also cause an increase in conduction losses in the circuit.

Aside from contributing to increases in losses within the circuit, the large current spikes would likely cause substantial damage to the Dickson SCC's components, either through breakdown due to excessive voltage noise or thermal failure caused by excessive current.

The problem of charge redistribution, and the corresponding increase in power losses and probability of circuit damage in switched-capacitor converters, have resulted in most implementations of SCCs being in low-power applications, typically with peak output currents of no more than 10 A (as in [8] and [26]). The implementation described in [8] is a 1.5 W 11V to 1.5 V step-down Dickson SCC. This low-power implementation achieved a fairly low efficiency (around 92%) but had a high power density of 750 W/in^3. The implementation described in [26] is a 300 W, 280 V to 28 V Dickson step-down converter. This implementation achieved a high peak efficiency of 99.1%, but a low power density of 87 W/in^3.

Charge redistribution within the Dickson SCC is primarily the result of voltage ripples within flying capacitors. Therefore, the effects of charge redistribution can be mitigated by either using large flying capacitors, as shown in the implementation described in [27] (to

directly reduce capacitor voltage ripple), or by increasing the switching frequency (to reduce the charging and discharging times of the flying capacitors, thus also reducing voltage ripple). However, using large flying capacitors requires space, therefore, the SCC's benefit of increased power density could be nullified. The implementation described in [27] has similar power ratings as those described in the thesis objectives, however, this implementation made use of very large flying capacitors (up to 500 µF) in order to compensate for charge redistribution. Aside from taking up substantial space, utilizing capacitors of this size would drive up the cost of implementation significantly. With regards to increasing the switching frequency, since switching losses are proportional to the switching frequency (as seen in Equation 4), increasing the switching frequency would cause a corresponding increase in switching losses, decreasing the performance of the converter. Furthermore, an increase in the switching frequency of the power converter can increase the possibility of electromagnetic interference [28] within the data center. Thus, for practical implementation in high-current applications, the problem of charge redistribution in SCCs must be overcome using a method that does not utilize large components or high switching frequencies.

2.3 Split-Phase Control

As was described in the previous section, charge redistribution occurs within the Dickson switched-capacitor converter when there are differences between the equivalent circuit branch voltages, measured from the output node V_n, when switching takes place. Instead of merely mitigating the effect of charge redistribution through the use of large components and/or switching frequencies, another approach to solve the problem of charge redistribution is to eliminate the voltage differences through more advanced control

mechanisms; that is to say, ensure that Equations 2 and 3 are always satisfied during switching by controlling the voltages of the flying capacitors using the circuit's switches. Elimination of the voltage differences during switching that cause charge redistribution therefore allows the use of smaller components in higher-power applications of the Dickson switched-capacitor converter without compromising the performance and reliability of the converter.

Split-phase control [20] is one such control method that greatly reduces or eliminates the effect of charge redistribution within the Dickson switched-capacitor converter by ensuring the voltages of the equivalent circuit branches are matched when switching takes place, by effectively implementing voltage control on the three flying capacitors. Split-phase control accomplishes this by imposing reduced duty cycles on some of the Dickson SCC's switches, such that they are turned off earlier than the other switches they are in phase with. The switches with reduced duty cycles imposed ('split-phase' switches) are typically ones that conduct within equivalent circuit branches consisting of a single flying capacitor, therefore that flying capacitor's charging and discharging, and thus its voltage, can be directly controlled. The duty cycle to be imposed on the 'split-phase' switches are dependent on the circuit's conversion ratio. As seen in the derivations shown in [20], the amount of duty cycle to be implemented on the 'split-phase' switches for a N-to-1 conversion ratio Dickson SCC can be calculated using Equation 8.

$$D_{(split-phase)} = \frac{N+2}{4N} \tag{8}$$

For a 4-to-1 Dickson SCC, referring to Equation 6, split-phase control is realized by setting duty cycles of 37.5% on switches Q5 and Q8, keeping the duty cycles of the other switches at 50%. Switch Q8 conducts within the equivalent circuit branch consisting of

capacitor C3 during Phase 1 (see Figure 4), and switch Q5 conducts within the equivalent circuit branch consisting of capacitor C1 during Phase 2 (see Figure 5). Therefore, imposing reduced duty cycles on these two switches would allow for the charging and discharging of capacitors C3 and C1 to be directly controlled. The imposition of duty cycles of 37.5% on switches Q5 and Q8, keeping the duty cycles of all other switches as 50%, results in four equivalent circuits, as can be seen in the simplified equivalent circuit diagrams in Figure 8, sourced from [20].

2.3.1 Split-Phase Operation

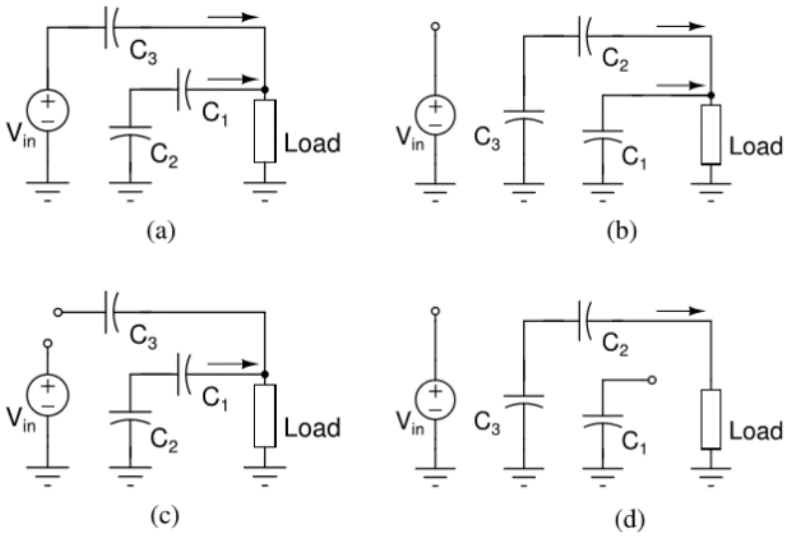

Figure 8: Simplified split-phase equivalent circuits for 4-to-1 Dickson SCC for Phase 1 (a), Phase 2 (b), Phase 1b (c), Phase 2b (d) [20]

Figures 8a and 8b show the existing equivalent circuit phases from two-phase operation of the 4-to-1 Dickson SCC, Phase 1 and Phase 2, while figures 8c and 8d show the added equivalent circuit phases resulting from the imposition of split-phase control on the 4-to-1 Dickson SCC. These additional phases will be referred to as Phase 1b (Figure 8c) and Phase 2b (Figure 8d).

The circuit begins the switching cycle in Phase 1. Switch Q8 is turned off at time instance t = 0.375T, transitioning the circuit into Phase 1b. This leaves one end of flying capacitor C3 floating and thus unable to discharge or charge. At the same time, capacitor C2 discharges into C1 at an increased rate, as with only one circuit branch connected to the load, the branch consisting of C2 and C1 carries the full load current. Since the voltage of C3 will be held steady during this phase, instead of continually charging through the first switching phase as in two-phase operation, its voltage will be smaller in value when switching occurs, when compared to its voltage before switching during two-phase operation. Similarly, as C2 discharges faster during Phase 1b than it does in Phase 1, its voltage will also be smaller in value when switching occurs. Finally, as C1 is being charged faster before switching in split-phase control, compared to in two-phase control, its voltage will be larger in value when switching occurs, compared to its voltage during switching during two-phase control. The Phase 2 equivalent branch voltage $V_{C3} - V_{C2}$ is reduced compared to two-phase control, while the Phase 2 equivalent branch voltage V_{C1} is increased compared to two-phase control. As shown in the previous two-phase simulation results in Figure 7, the branch voltage $V_{C3} - V_{C2}$ was divergent and was greater in magnitude than V_{C1} during switching, resulting in charges rapidly redistributing once switching takes place. With the voltage balancing provided by the intermediary circuit phase, the voltage difference between the equivalent branches would be greatly reduced before switching, allowing for a transition between Phase 1b and Phase 2 at the midpoint of the switching cycle with little to no current transients. The configuration of the 4-to-1 Dickson SCC circuit during Phase 1b, with current paths highlighted, is shown in Figure 9.

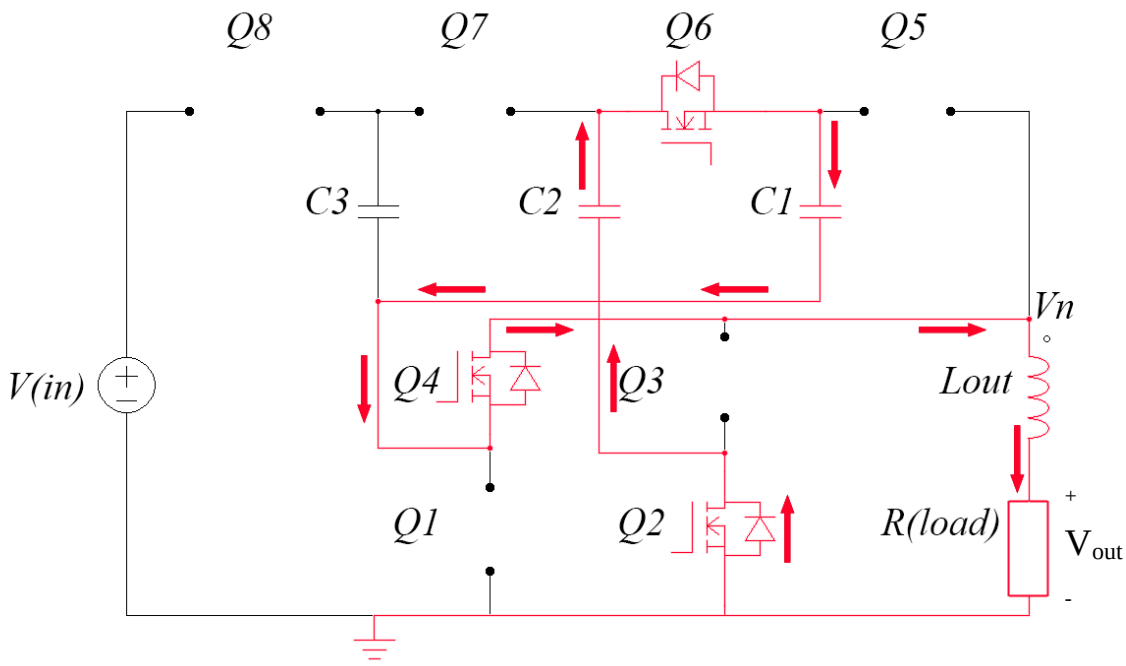

Figure 9: Circuit configuration of 4-to-1 Dickson SCC in Phase 1b

At time instance t = 0.875T, switch Q5 is turned off, transitioning the circuit from Phase 2 into Phase 2b. With switch Q5 off, flying capacitor C1 is left floating and thus unable to charge or discharge. At the same time, capacitor C3 discharges into C2 at an increased rate since, being the only active equivalent circuit branch in Phase 2b, this branch is carrying the full load current. At the end of the switching cycle, the circuit transitions from Phase 2b back to Phase 1, again with little or no current transients. The configuration of the 4-to-1 Dickson SCC circuit during Phase 2b, with current paths highlighted, is shown in Figure 10.

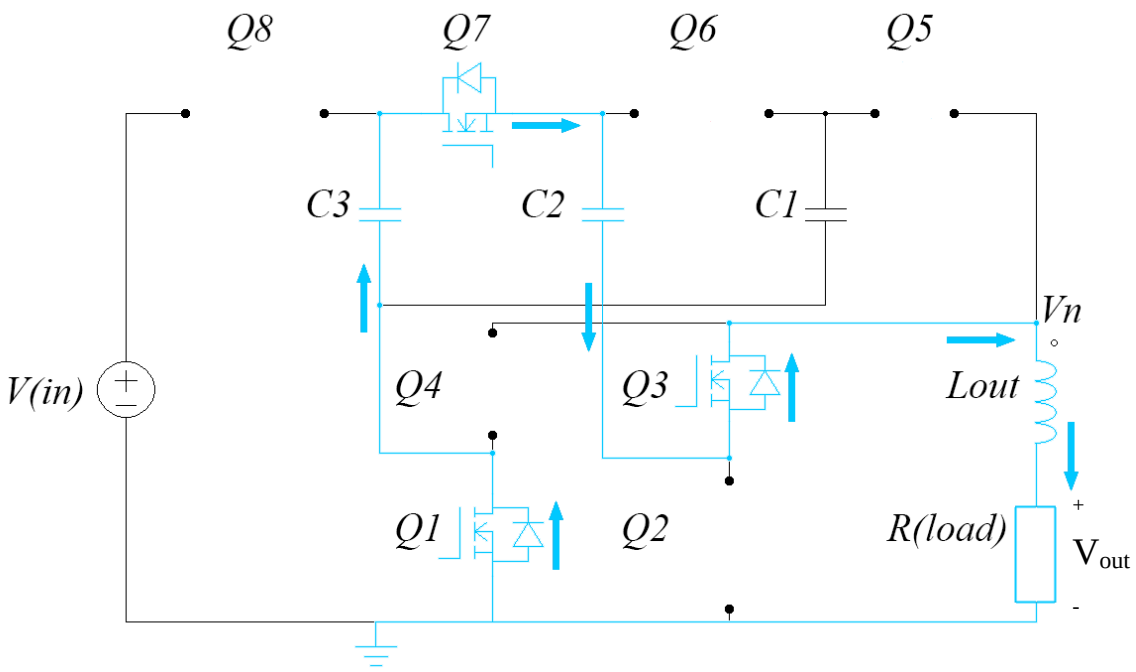

Figure 10: Circuit configuration of 4-to-1 Dickson SCC in Phase 2b

For split-phase control to effectively reduce the equivalent circuit voltage differences, a small inductor is required to be added between the output node and the load, to ensure that, during the intermediary circuit phases, the current continues to flow to the load.

To verify that split-phase control would indeed greatly reduce or eliminate the voltage differences between the equivalent circuit branches during switching, and thus reduce or eliminate the effects of charge redistribution, the 4-to-1 Dickson SCC circuit, with component parameters as shown in Table 1, was simulated with split-phase control. The results of this simulation, shown in Figure 11, show that even with relatively small (47 µF) flying capacitors and a relatively high output current of 35 A, the imposition of split-phase control has greatly reduced the equivalent circuit branch voltage differences during switching, thereby also greatly reducing the effects of charge redistribution.

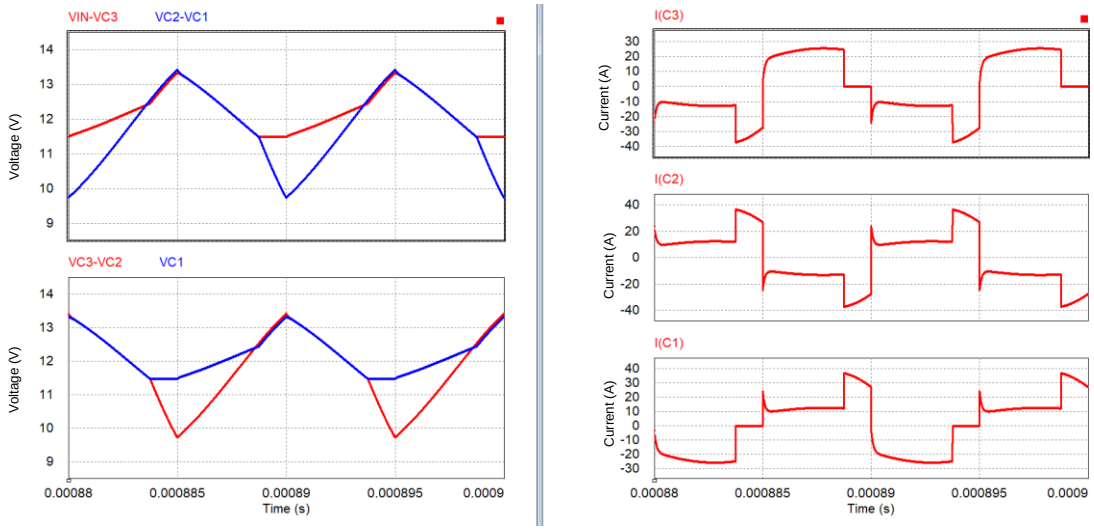

Figure 11: Simulated equivalent circuit branch voltage (left) and flying capacitor current (right) waveforms of split-phase 4-to-1 Dickson SCC

With the reduction of the problem of charge redistribution in the Dickson SCC, and the corresponding reduction of current spikes through the circuit, the performance of the Dickson SCC is improved, thanks to lower switching and conduction losses. Split-phase control thus allows the Dickson SCC to be implemented in higher-power and higher-current applications using relatively small flying capacitors, while dispensing with the need to increase switching frequency to compensate for charge redistribution, thereby maintaining its benefits of increased power density and increased performance.

By reducing the effects of charge redistribution significantly, split-phase control can allow for feasible implementation of the Dickson switched-capacitor converter in high-current applications. However, to date, no implementations of the split-phase Dickson SCC in high-current applications have been reported. Existing implementations of Dickson converters with split-phase control have been in low-current applications with load currents of no more than 6 A [10] [20] [25]. Therefore, in-depth analysis of practical factors that could impede the effectiveness of split-phase control would need to be performed in order

to successfully adapt the split-phase Dickson SCC to operate effectively in 48 V to 12 V, 35 A operation. Practical considerations such as mismatch and variance of flying capacitor values and the impact of input voltage ripple, which may not have much impact on implementations handling low currents, may have significant impacts on performance of the split-phase Dickson SCC at higher power loads. Should these factors be identified as major sensitivities of the split-phase Dickson SCC, measures to mitigate these practical considerations would need to be devised.

2.4 Conclusion

This chapter provided an overview on the basic (two-phase) operation of the Dickson SCC topology. The problem of charge redistribution was also highlighted, and its effects demonstrated through computer simulation. Considering the impacts of charge redistribution on the operation of the circuit, compensatory measures would be required for high-current applications of the Dickson SCC. This chapter also introduced Split-Phase Control, a method that eliminates charge redistribution within the Dickson SCC through capacitor voltage control. The effectiveness of split-phase control was also demonstrated through simulation. Finally, a review of current implementations of both the two-phase and split-phase Dickson SCC topologies was presented in this chapter. These reviews highlighted the fact that most current implementations of the Dickson SCC topology were in low-power, low-current applications.

Chapter 3

Sensitivity Analysis of Split-Phase Control

As discussed in the Literature Review, the split-phase control method has been seen to be effective at reducing the effects of charge redistribution significantly. This paves the way for a well-performing implementation of the Dickson switched-capacitor converter in high-current applications. However, as all applications of split-phase control thus far have been in low-power applications, it is unknown what, if any, sensitivities are exhibited by the split-phase Dickson SCC. The effects of real-world factors and limitations, while typically not a concern in low-power applications, tends to become amplified with increases in the amount of power handled. The effects of these practical factors could be such that they severely impede the split-phase control method's effectiveness of reducing/eliminating charge redistribution. Analysis of the effects of practical factors on the operation of the split-phase Dickson SCC, through circuit simulation, is therefore a necessary step to ensure that the circuit can be successfully implemented at power levels applicable in data centers.

Split-phase control, as discussed in Section 2.3.1, eliminates charge redistribution by effectively implementing voltage control on the flying capacitors, through the imposition of reduced duty cycles on some switches. The derivations for split-phase control, presented in [20], assumed that the split-phase Dickson SCC operates with matched flying capacitors. From the information stated above, two potential sensitivities related to practical limitations and factors can be identified. These factors are (1) mismatched flying capacitors, and (2) input voltage ripple. These factors could result in the voltage control imposed on the flying capacitors becoming less effective at reducing the equivalent circuit

branch voltage differences during switching, and thus resulting in split-phase control not fully compensating for charge redistribution.

The most effective method to gauge the impact on split-phase control of these sensitivities, in simulation, is to observe the equivalent circuit branch voltage differences during switching, as well as the currents through the flying capacitors during switching. If differences in the equivalent circuit branch voltages are present during switching, there will be corresponding current spikes through the flying capacitors during switching. The magnitudes of the voltage differences and current spikes can then be used to gauge the sensitivity of split-phase control to the practical factors.

3.1 Flying Capacitor Mismatch

The derivations for split-phase control, as shown in [20], were made under the assumption that the flying capacitors of the Dickson SCC were equally matched. Split-phase control relies on the control of the charging and discharging of the flying capacitors to eliminate voltage differences at the output node during switching, and thus eliminate charge redistribution. If the flying capacitors of the split-phase Dickson SCC are mismatched in capacitance, the flying capacitors will not charge and discharge at equal rates, given a fixed current. Without the addition of significant control complexity, the uneven charging and discharging caused by flying capacitor mismatch may cause voltage differences between the equivalent circuit branch voltages to appear at the output node during switching. In other words, equations 2 and 3 are no longer satisfied. In this scenario, split phase control will not be completely effective at eliminating charge redistribution. In low current applications, flying capacitor mismatch is not a significant issue in the split-phase Dickson SCC, as the current is low enough for the flying capacitors' voltage ripples,

and therefore equivalent circuit branch voltage differences resulting from capacitor mismatch, to be negligibly small anyway. However, as the amount of current handled is increased, the voltage ripples of the flying capacitors will increase correspondingly, increasing the probability that mismatched flying capacitors will result in significant differences in voltage between the equivalent circuit branches during switching. Therefore, it is imperative that the flying capacitors for a high-current split-phase Dickson SCC circuit be matched in capacitance as closely as possible.

Practical limitations that result in mismatched flying capacitors include capacitor de-rating and manufacturing tolerance. The flying capacitors for switched-capacitor converters are typically implemented using ceramic capacitors because of their high capacitance-to-volume ratio, as well as their low equivalent series resistance (ESR) values. Ceramic capacitors are known to lose capacitance when a DC voltage is applied across them. Additionally, the processes in which capacitors are fabricated typically have tolerances of ±20%. The combined factors of ceramic capacitor de-rating and manufacturing tolerances of ±20% makes exactly matching the flying capacitors in the split-phase Dickson SCC difficult to accomplish in practice.

3.1.1 Simulation Analysis of Flying Capacitor Mismatch

Simulations were performed on the 4-to-1 split-phase Dickson SCC circuit using the PSIM simulation software to investigate sensitivity of the split-phase control method, when the possibility of mismatched flying capacitors is considered. For each simulation, individual flying capacitors had their capacitances varied by ±20%, with the remaining capacitors held at nominal value. The figure of ±20% was used for the flying capacitor

variances given typical ceramic capacitor manufacturing tolerances. Nominal simulation parameters used for this analysis are shown in Table 2.

Table 2: Simulation Parameters Used for Sensitivity Analysis

SIMULATION PARAMETERS	
V_{IN}	48 V
V_{OUT}	12 V
I_{OUT}	35 A
C3, C2, C1	47 µF
C_{OUT}	47 µF
L_{OUT}	200 nH
D_5	0.375
D_8	0.375
$D_{(All\ other\ switches)}$	0.5
f_{SW}	100 kHz
$R_{DS(on)}$	1 mΩ
R_{ESR}	1 mΩ
$R_{L(winding)}$	0.3 mΩ

In an ideal scenario, with the flying capacitors exactly matched, split-phase control should ensure that the voltages of the equivalent circuit branches equalize before switching takes place; in other words, equations 2 and 3 are satisfied. Correspondingly, the currents through the flying capacitors experience little to no transient spikes when switching occurs, as shown in the branch voltage and capacitor current waveforms in Figure 12

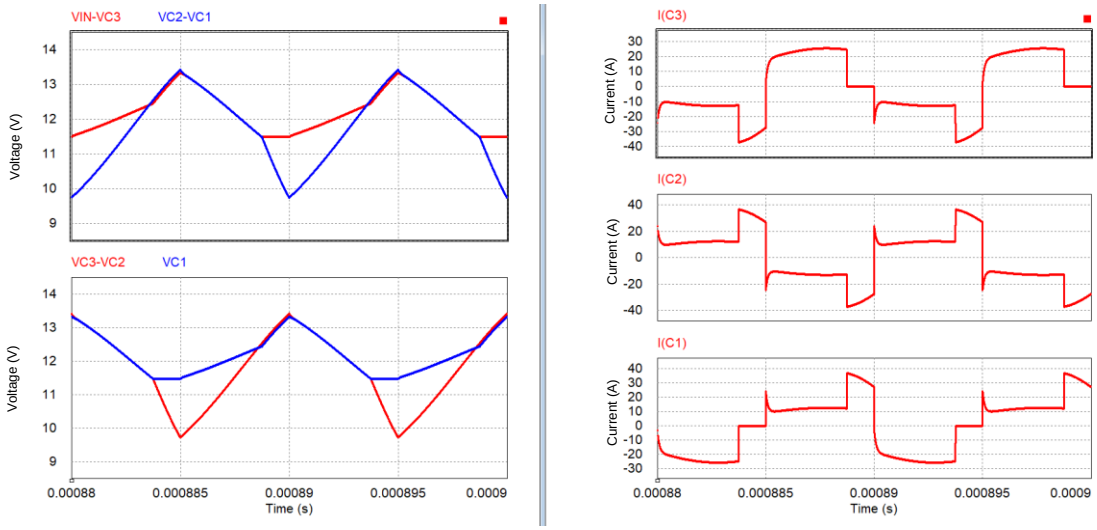

Figure 12: Ideal branch voltage (left) and flying capacitor current (right) waveforms of simulated 48 V to 12 V, 35 A split-phase Dickson SCC with 47 µF flying capacitors

As previously discussed, if there is mismatch of capacitance between the flying capacitors, they will have different charging and discharging rates. Consequently, the voltage control imposed by split-phase control will not be able to fully eliminate the voltage differences at the output node during switching, therefore it will no longer fully compensate for charge redistribution. When the capacitance of flying capacitor C3 was reduced by 20% in the simulation, voltage differences of 0.28 V were introduced between the equivalent circuit branch voltages during both the Phase 1 to Phase 2 transition, as well as the Phase 2 to Phase 1 transition. This voltage difference resulted in current spikes with maximum magnitudes of 60 A appearing through the flying capacitors during switching, as shown in Figure 13.

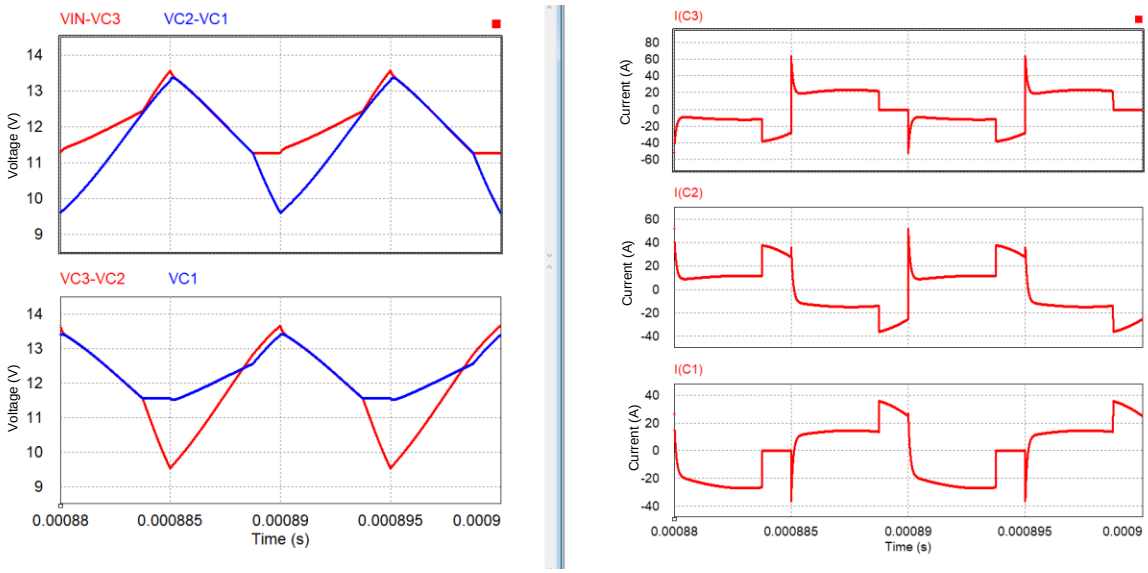

Figure 13: Branch voltage (left) and flying capacitor current (right) waveforms of simulated 48 V to 12 V, 35 A split-phase Dickson SCC with 47 µF flying capacitors, C3 20% smaller than other flying capacitors

Current spikes and branch voltage differences of similar magnitudes were observed in simulations with variances in capacitance applied to other flying capacitors. Observations of output node voltage differences and maximum flying capacitor currents throughout the simulations are shown quantitatively in Tables 2 and 3.

Table 3: Summary of Capacitor Variance Analysis Simulations – Branch Voltage Differences

Scenario	C3 size (µF)	C2 size (µF)	C1 size (µF)	Branch voltage difference (Phase 1)	Branch voltage difference (Phase 2)
Ideal	47.00	47.00	47.00	-0.09	0.09
C3 -20%	37.60	47.00	47.00	0.28	0.27
C3 +20%	56.40	47.00	47.00	-0.32	-0.02
C2 -20%	47.00	37.60	47.00	-0.33	0.33
C2 +20%	47.00	56.40	47.00	0.06	-0.07
C1 -20%	47.00	47.00	37.60	-0.27	-0.27
C1 +20%	47.00	47.00	56.40	0.02	0.33

Table 4: Summary of Capacitor Variance Analysis Simulations – Maximum Capacitor Currents

Scenario	C3 size (µF)	C2 size (µF)	C1 size (µF)	IC3 (A, max)	IC2 (A, max)	IC1 (A, max)
Ideal	47.00	47.00	47.00	36.89	36.89	36.87
C3 -20%	37.60	47.00	47.00	64.14	52.30	36.29
C3 +20%	56.40	47.00	47.00	35.99	62.31	62.31
C2 -20%	47.00	37.60	47.00	62.66	62.86	62.86
C2 +20%	47.00	56.40	47.00	36.71	36.71	36.69
C1 -20%	47.00	47.00	37.60	36.47	52.50	64.30
C1 +20%	47.00	47.00	56.40	62.02	62.02	35.97

As shown in Tables 2 and 3, only the scenario in which a +20% variance was applied on capacitor C2 did not result in significant capacitor current spikes. The waveforms obtained from simulation of this scenario can be seen in Figure 14. Recalling the output node voltage equations shown in Chapter 2 (Equations 2 and 3) and the simulation results from the ideal scenario, it can be seen in Table 2 that, for the ideal scenario, the voltage difference during the transition to Phase 1 was a negative value ($(V_{IN} - V_{C3}) < (V_{C2} - V_{C1})$), while the voltage difference during the transition to Phase 2 was a positive value ($(V_{C3} - V_{C2}) > V_{C1}$). When the size of capacitor C2 was increased, the resulting decreased voltage ripple of C2 meant that the terms ($V_{C2} - V_{C1}$) and ($V_{C3} - V_{C2}$) became smaller compared to the ideal scenario. Consequently, the voltage differences during switching also became smaller. This was the reason why a +20% variance on capacitor C2 did not result in any significant current spikes through the flying capacitors.

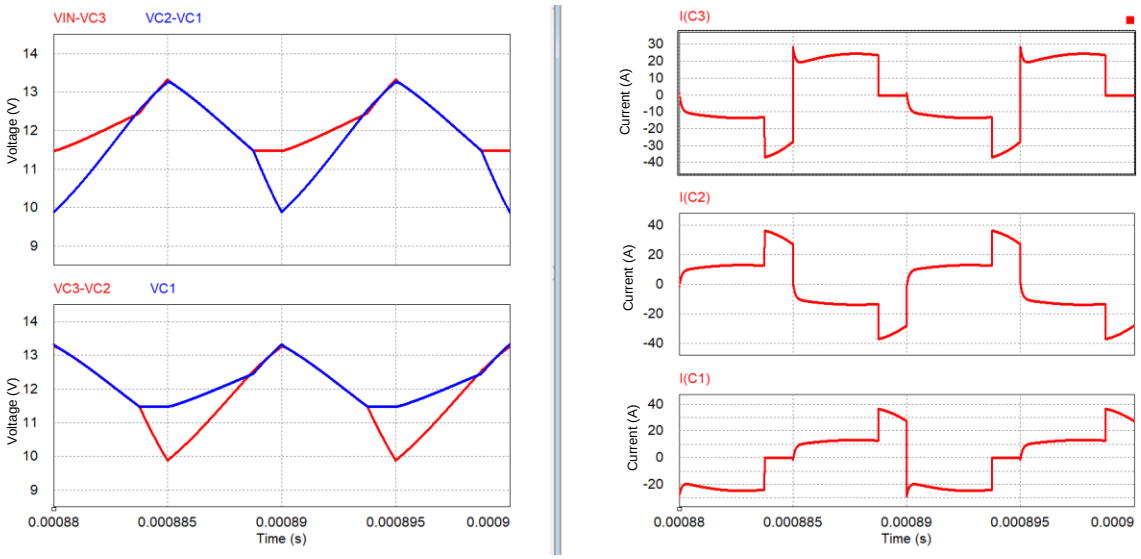

Figure 14: Branch voltage (left) and flying capacitor current (right) waveforms of simulated 48 V to 12 V, 35 A split-phase Dickson SCC with 47 µF flying capacitors, C2 20% larger than other flying capacitors

The simulation results shown in Figure 8 and summarized in Tables 2 and 3 show that almost all flying capacitor variance scenarios tested in simulation resulted in current spikes of around double the output current through the flying capacitors. This clearly indicates that the split-phase Dickson converter exhibits a significant sensitivity pertaining to variances in the sizes of the flying capacitors relative to each other; the unequal capacitor charging and discharging rates caused by capacitor mismatch results in split-phase control not fully eliminating the problem of charge redistribution.

In a scenario where all flying capacitors have a different capacitance, the current transients through the flying capacitors resulting from uneven charging and discharging of flying capacitors could be much higher. As an example, Figure 15 shows the branch voltage and capacitor current waveforms obtained from a simulation of the 4-to-1 split-phase Dickson SCC with truly mismatched flying capacitors. For this simulation, capacitor C3 had a size of 56.4 µF (+20%), capacitor C2 had a value of 37.6 µF (-20%), and capacitor

C1 had a value of 47 µF. The maximum voltage difference observed was during the transition to Phase 1, with a value of 0.543 V. This resulted in current spikes of up to 97 A appearing through the flying capacitors during this transition, highlighting the split-phase Dickson SCC's sensitivity to flying capacitor mismatch.

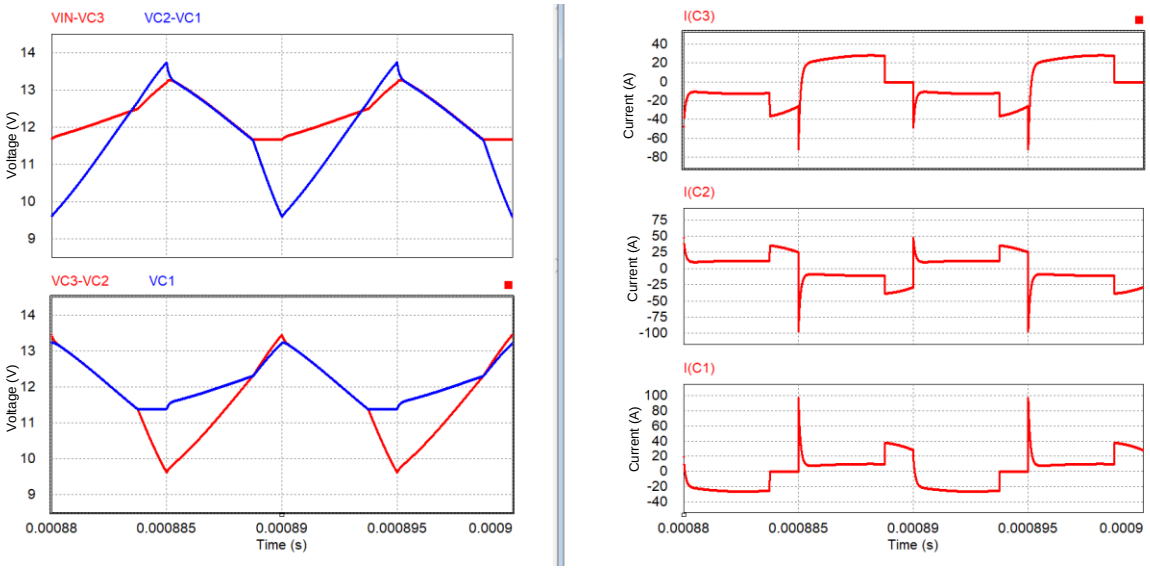

Figure 15: Branch voltage (left) and flying capacitor current (right) waveforms of simulated 48 V to 12 V, 35 A split-phase Dickson SCC. All flying capacitors mismatched

In practice, the current spikes resulting from charge redistribution due to mismatched flying capacitors contribute to additional switching losses and conduction losses. Furthermore, as previously discussed, the current spikes and/or the voltage noise resulting from charge redistribution could cause damage to circuit components. It follows that, as a conclusion for this simulation analysis, for best performance, and especially in high-current applications, the actual capacitances of the flying capacitors of the split-phase Dickson converter should be matched in capacitance as closely as possible to minimize the risk of charge redistribution due to flying capacitor mismatch. Unfortunately, as previously discussed, due to real-world limitations including ceramic capacitor de-rating due to voltage, as well as typical manufacturing tolerances, the values of the flying capacitors in

operation may be different compared to the designed values. As such, precisely matching the flying capacitors is very difficult in practice. Practical design of the flying capacitors for the 48 V to 12 V, 35 A split-phase Dickson converter will be further discussed in the Hardware Design section of this thesis.

3.2 Input Voltage Ripple

In ideal operating circumstances, as shown in Figure 12, the voltage control of the flying capacitors provided by split-phase operation allows the Dickson SCC's equivalent branch voltages to satisfy equations 2 and 3, and therefore would be able to fully eliminate charge redistribution. However, since SCCs are not isolated from the input in any way, any input voltage ripple would cascade into the circuit. The ripple of the input voltage could superimpose itself onto the voltages of the flying capacitors, to the point where Equations 2 and 3 are no longer satisfied and charge redistribution is therefore not fully eliminated. In low-power applications of the Dickson SCC, the current loads are typically low enough such that the magnitude of input voltage ripple is also kept very low. As such, the effects of input voltage ripple at low power are minimal, if present at all. Input voltage ripple is a much more significant concern for high-power applications of the split-phase Dickson SCC, as the potential reintroduction of charge redistribution due to input voltage ripple could result in much greater adverse effects on the performance of the circuit.

3.2.1 The Input Filter

In practical applications of DC-DC power converters, it is necessary to insert an input filter between the power supply and the power converter circuit. The input filter ensures that the power supply delivers a purely DC current, since it is unrealistic for the power supply to deliver pulsating current; this would result in dramatic increases of noise within

the circuit. Input filters for DC-DC converters are typically in the form of a passive low-pass filter, consisting of an input capacitor connected between the power supply and ground, and optionally, an input inductor connected in series between the power supply and the input capacitor, as shown in the revised Dickson SCC circuit diagram in Figure 16.

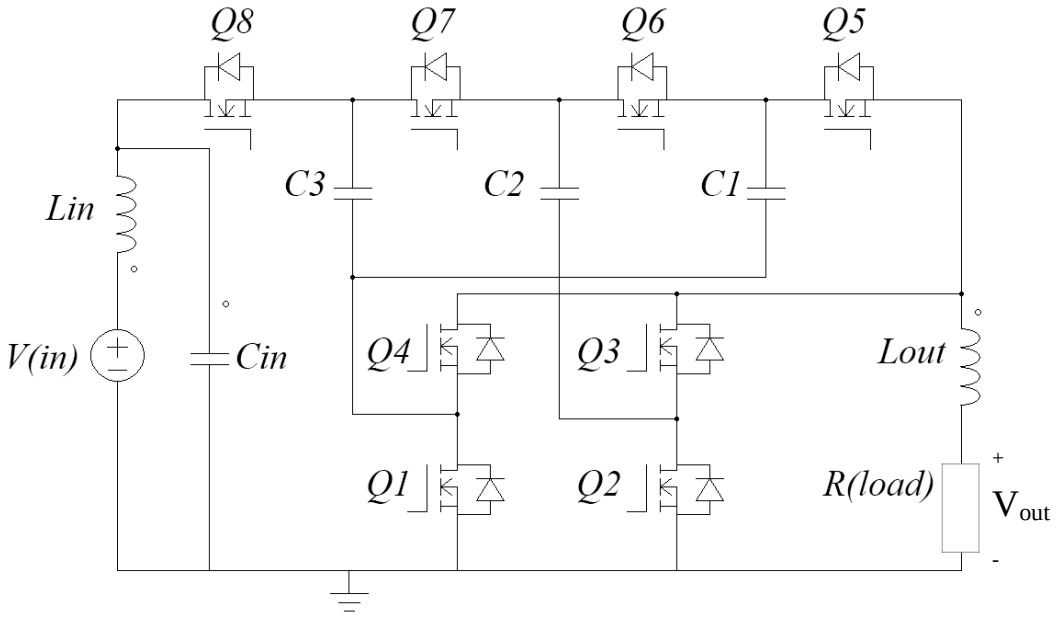

Figure 16: Circuit schematic of a 4-to-1 Dickson SCC with input filter

In the 4-to-1 Dickson SCC, the power supply always supplies an input current equal to a quarter of the output current (the input current is equal to the output current divided by the conversion ratio). During Phase 1 when the power supply is directly connected to the circuit, the input capacitor discharges into the circuit, complementing the current supplied by the input source. When the power supply is disconnected from the rest of the circuit (all other circuit phases), the current from the power supply charges the input capacitor for the next switching period. This charging and discharging cycle of the input capacitor, along

with the fact that the input capacitor is tied to the power supply, causes the input voltage to effectively exhibit a voltage ripple.

For the split-phase 4-to-1 Dickson SCC, the input source is in series with flying capacitor C3 during Phase 1 of the switching cycle. This causes any input voltage ripple to superimpose itself onto the voltage of C3, in turn causing Equation 3 to no longer be satisfied when the circuit switches from Phase 1b to Phase 2. Due to capacitor-capacitor interactions, the input voltage ripple then cascades through the rest of the circuit over the course of the switching cycle, causing Equation 2 to no longer be satisfied when the circuit switches from Phase 2b to Phase 1. In steady-state operation, voltage ripple at the input causes branch voltage differences of roughly equal magnitudes to appear during switching transition, thereby indicating that input voltage ripple is disrupting the ability of the split-phase control theory to eliminate charge redistribution.

3.2.2 Impact of Input Voltage Ripple through Computer Simulation

Using the same component parameters shown in Table 2 and assuming matched flying capacitors, simulations were performed on the 4-to-1 split-phase Dickson SCC to analyze the effects of input voltage ripple on split-phase operation. Figure 17 shows the equivalent circuit branch voltages, as well as flying capacitor current waveforms, when the split-phase Dickson SCC was simulated with an input filter comprised of a 47 μF input capacitor.

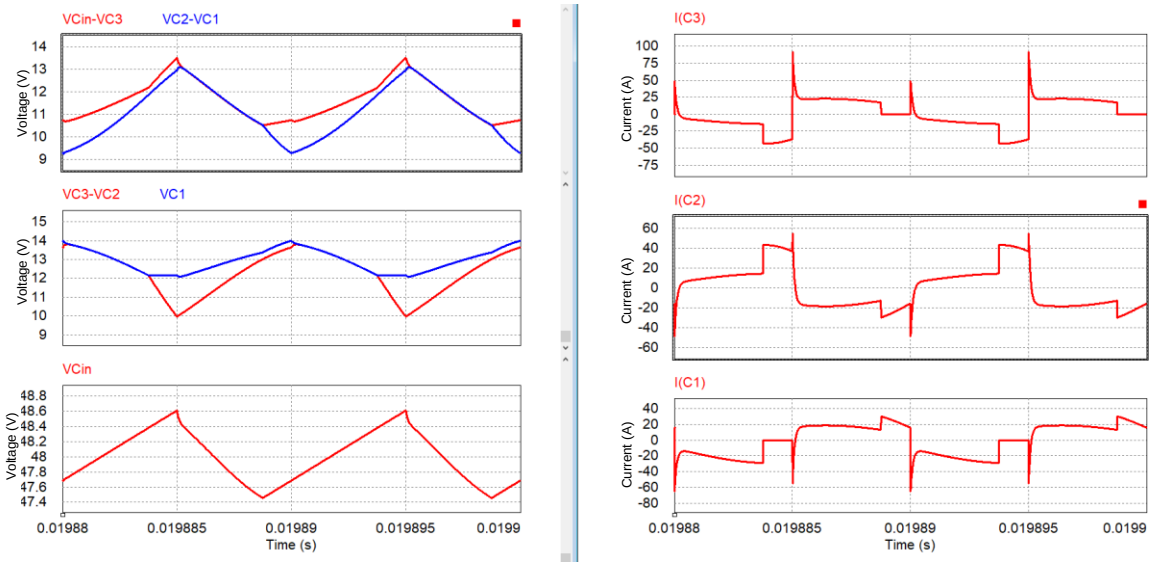

Figure 17: Branch voltage (left) and flying capacitor current (right) waveforms of simulated 48 V to 12 V, 35 A split-phase Dickson SCC with 47 µF flying capacitors, 47 µF input capacitor

The simulation results in Figure 17 show that a peak-to-peak input voltage ripple of 1.15 volts resulted in equivalent circuit branch voltage differences of between 0.36 V and 0.55 V during switching. This resulted in current spikes of up to 90 A through the flying capacitors. The magnitudes of these current spikes are close to three times the output current of 35 A. In operation, these current spikes result in significant switching and conduction losses and could also result in component damage due to excessive voltage noise. Therefore, the sensitivity of the split-phase Dickson SCC to input voltage ripple is a significant design consideration.

Additional simulations were performed using different sizes of input capacitor to determine the effects of different magnitudes of input voltage ripple on the maximum flying capacitor currents in the split-phase Dickson SCC. As shown in Table 4, the effects of input voltage ripple on the split-phase Dickson SCC decreases sharply with larger input

capacitors, since larger capacitors inherently exhibit small voltage ripples while charging and discharging continually.

Table 5: Summary of Input Voltage Ripple Simulation Analysis - Branch voltage differences and maximum capacitor currents relative to input capacitor size

Input Capacitance (uF)	I(C3) (max, A)	I(C2) (max, A)	I(C1) (max, A)	Cin Voltage Ripple (mV p-p)	Phase 2 to Phase 1 voltage difference (mV)	Phase 1 to Phase 2 voltage difference (mV)
30	**147**	**106**	**106**	1810	987	548
47	**91**	**54**	**64**	155	550	359
100	**43**	40	35	502	188	142
220	38	38	35	246	34	20
500	37	37	36	108	31	41

Since it is known that larger input capacitors can suppress a greater amount of voltage ripple, it was decided that, for Prototype 1 of the 48 V to 12 V, 35 A split-phase Dickson SCC (presented in Chapter 4), the sensitivity of the split-phase Dickson converter to input voltage ripple would be mitigated by using a large electrolytic capacitor as the input filter. Since the primary objective of the first prototype was to prove that the split-phase Dickson SCC could be implemented in a high-current application, the usage of a large electrolytic capacitor for the first prototype was deemed acceptable. However, as will be later shown in Chapter 5, the use of the electrolytic input capacitor resulted in significant power losses due to its inherently large ESR.

3.3 Conclusions from Sensitivity Analysis

This chapter presented in-depth analyses of potential real-world sensitivities exhibited by the split-phase Dickson SCC, as well as discussions on their impacts on the performance of the circuit in high-power, high current applications. It has been concluded that mismatches in capacitance between the split-phase Dickson SCC's flying capacitors could

result in the split-phase control mechanism not fully compensating for charge redistribution, since the resultant uneven charge/discharge rates between the flying capacitors interferes with the voltage control imposed on the flying capacitors by split-phase control.

In addition, input voltage ripple tends to superimpose itself onto the voltage waveforms of the split-phase Dickson SCC's flying capacitors, interfering with the operation of the split-phase control mechanism, reducing the effectiveness of split-phase control in compensating for charge redistribution.

The sensitivities of the split-phase Dickson SCC to flying capacitor mismatch, as well as input voltage ripple, are therefore important design considerations in adapting the split-phase Dickson SCC to perform at high-power, high current applications.

Chapter 4

Design Methodologies

As discussed in the previous chapter, the split-phase Dickson SCC exhibits two significant sensitivities in the form of flying capacitor mismatch and input voltage ripple. Both factors tend to reduce the effectiveness of split-phase control at compensating for the problem of charge redistribution. The degradation in performance due to these sensitivities is far more noticeable in high-power, high current applications, where the possibility of increased losses and component failure due to transients is far higher than in low-power applications. The design of the circuit components for high-power, high current split-phase Dickson SCCs must therefore take these sensitivities into account. Two prototypes of the 48 V to 12 V, 35 A split-phase Dickson SCC were designed. Due to the onset of the COVID-19 pandemic in early 2020, only one of these prototypes were able to be tested.

This chapter presents a discussion on the design of the flying capacitors for the prototypes. A derivation of an in-circuit flying capacitor measurement method is also presented. Discussions on the selection of other circuit components, as well as the design of the two printed circuit boards (PCBs) used for the prototypes, are also presented.

4.1 Flying Capacitor Design

It has been established through the investigations presented in section 3.1 that the split-phase Dickson SCC exhibits a significant sensitivity regarding flying capacitor mismatch. It is therefore imperative that the sizes of all three flying capacitors in the 48 V to 12 V, 35 A split-phase Dickson SCC prototype are matched in capacitance.

Flying capacitors for switched-capacitor converters are typically constructed with arrays of ceramic capacitors. Ceramic capacitors offer low equivalent series resistance (ESR) values, as well as a high capacitance-to-volume ratio. They are therefore ideal in applications requiring high power density and efficiency. However, ceramic capacitors have a fundamental downside, whereby they lose capacitance when a DC voltage is applied across them. This de-rating behavior must therefore be considered when designing the flying capacitors for the split-phase Dickson SCC, to ensure that the flying capacitors are matched in capacitance in operation, especially when each flying capacitor will have different steady-state blocking voltages in operation.

The flying capacitors for the 4-to-1, 48 V to 12 V, 35 A split-phase Dickson SCC prototype were initially matched to 60 µF using capacitor de-rating curves provided by the component manufacturers. Table 5 shows the components used to construct the three flying capacitors, their expected de-rating at the required DC bias levels for each flying capacitor, and the corresponding number of units required to construct each capacitor.

Table 6: Flying Capacitor Values and Quantities Used for Prototype, based on De-rating

Capacitor size, maximum rated voltage, and nominal capacitance	Expected DC bias voltage	Expected de-rating at DC bias	Per-unit capacitance at expected DC bias	Units needed for 60µF
1210, 4.7 µF, 100 V rating (Capacitor C3)	36 V	-57%	2.02 µF	30
1210, 10 µF, 50 V rating (Capacitor C2)	24 V	-42%	5.8 µF	10
1206, 10 µF, 35 V rating (Capacitor C1)	12 V	-40%	6 µF	10

Along with ceramic capacitor de-rating, another source of mismatch between the flying capacitors is manufacturing tolerance. This figure is typically ±20% for ceramic capacitors. Unlike ceramic capacitor de-rating, however, variances in capacitance due to manufacturing tolerance is much more difficult to predict. Because of this, along with the

possibility of inaccuracies in the supplied de-rating curves, an in-circuit measurement method was developed to measure the actual flying capacitor sizes based on their voltage waveforms obtained during testing. This in-circuit measurement method would allow for verification of the capacitances of the flying capacitors in the prototype, as well as allow for later fine-tuning of the flying capacitors for better performance, if desired. The derivation of the in-circuit capacitor measurement method is described in detail in the following subsection. An example using one of the voltage waveforms obtained from later prototype testing is also provided to demonstrate the method.

4.1.1 Derivation of In-Circuit Capacitor Measurement Method

As previously discussed in Chapter 3, the flying capacitors of the split-phase Dickson SCC should be matched as closely as possible to minimize voltage differences between the equivalent circuit branches during switching transition. As this requires precise values of capacitance, it is desired that, in operation, the real capacitances of the flying capacitors be as close as possible to the expected capacitances at the level of expected DC voltage bias as specified by the ceramic capacitors' data sheets. However, practical limitations such as component tolerance, as well as the possibility of inaccurate supplier de-rating curves, make this difficult to accomplish without some fine-tuning of the flying capacitors.

As discussed in the split-phase control overview in section 2.3 of this thesis, the operation of the 4-to-1 split-phase Dickson SCC consists of four circuit states. For reference, the simplified equivalent circuits for the 4-to-1 split-phase Dickson SCC, sourced from [20], are shown in Figure 18.

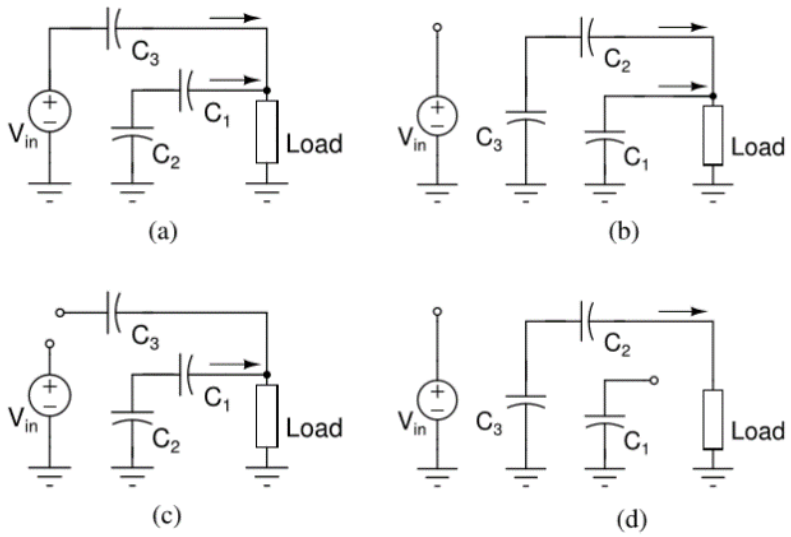

Figure 18: Simplified split-phase equivalent circuits for 4-to-1 Dickson SCC for Phase 1 (a), Phase 2 (b), Phase 1b (c), Phase 2b (d) [20]

Two of these states (Phase 1 and Phase 2; see Figures 18a and 18b [20]) have the same equivalent circuits as those in two-phase operation, while the other two states (Phase 1b and Phase 2b; see Figures 18c and 18d [20]) are sub-phases resulting from the application of split-phase control to the circuit. From Figure 18, while the equivalent circuits for phases 1 and 2 consist of two branches that conduct current, the equivalent circuits for phases 1b and 2b (the sub-phases resulting from split-phase control) only consist of one circuit branch which conducts current, comprised of two flying capacitors, with the remaining flying capacitor disconnected from the circuit. Since there is always a small inductor connected in series with the load, the current through the load will stay constant throughout the switching cycle. Therefore, it can be immediately deduced from the above information that the flying capacitors that conduct current during Phases 1b and 2b always carry the full load current.

From the split-phase equivalent circuit diagrams in Figure 18, it can also be observed that each flying capacitor carries current for at least one sub-phase per switching cycle. Therefore, since the load current is always known, the real value of the flying capacitors of the 4-to-1 split-phase Dickson SCC prototype can be obtained using the above information through first principles.

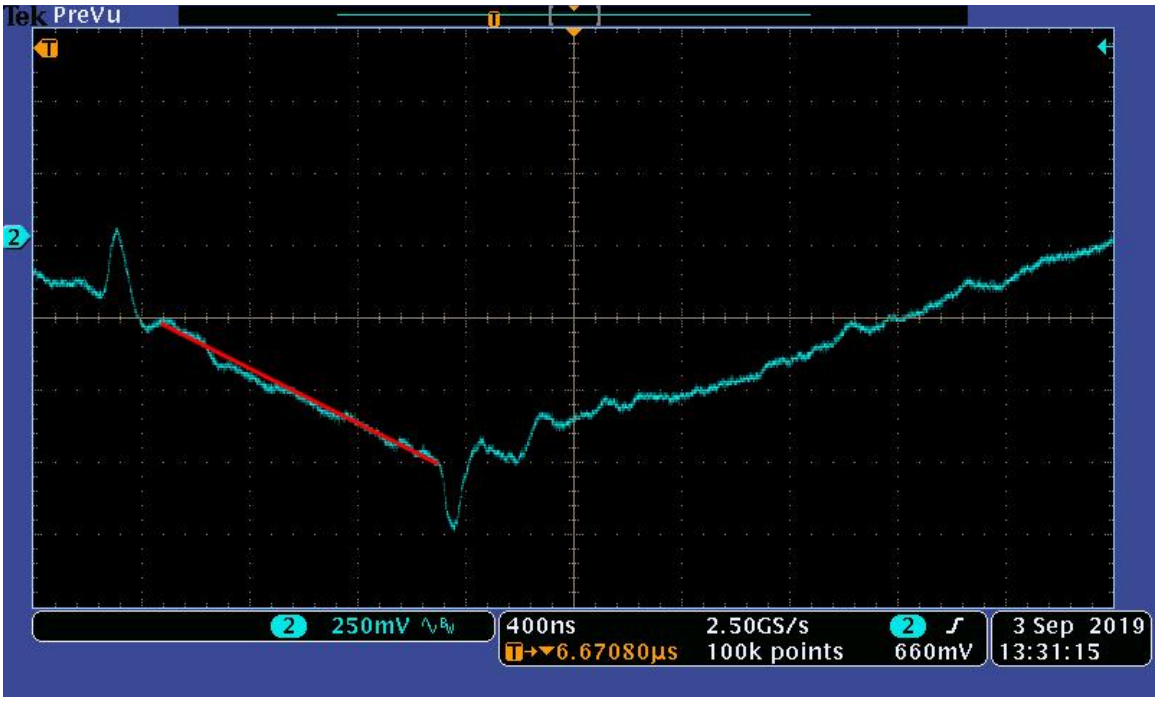

Figure 19: Magnified voltage waveform of capacitor C3 in 35 A output current operating condition, centered around the instance where it carries the full load current

As an example, Figure 19 shows the magnified waveform of flying capacitor C3 that was obtained from prototype testing. The time interval where the flying capacitors carry the full load current can be identified by instances where the slope of the voltage waveforms are the steepest. In the figure above, this time instance is highlighted with a red line. The change in voltage of this capacitor during this instance was measured to be 1.9 vertical oscilloscope divisions, over a time interval of 2.6 horizontal divisions. Given a scale of 250 mV per vertical division and 400 ns per horizontal division, the capacitor's

voltage thus changed by 0.45 V over a time of 1.04 µs. Substituting these values, along with the load current of 35 A, into the current-voltage equation for capacitors (Equation 9), the real capacitance of C3 as calculated using the waveform in Figure 14 was 78.7 µF.

$$C = I_{Load} * \frac{\Delta t}{\Delta V} \tag{9}$$

4.2 Selection of Other Components

4.2.1 Other Components for Prototype 1 of 48 V to 12 V, 35 A split-phase Dickson SCC

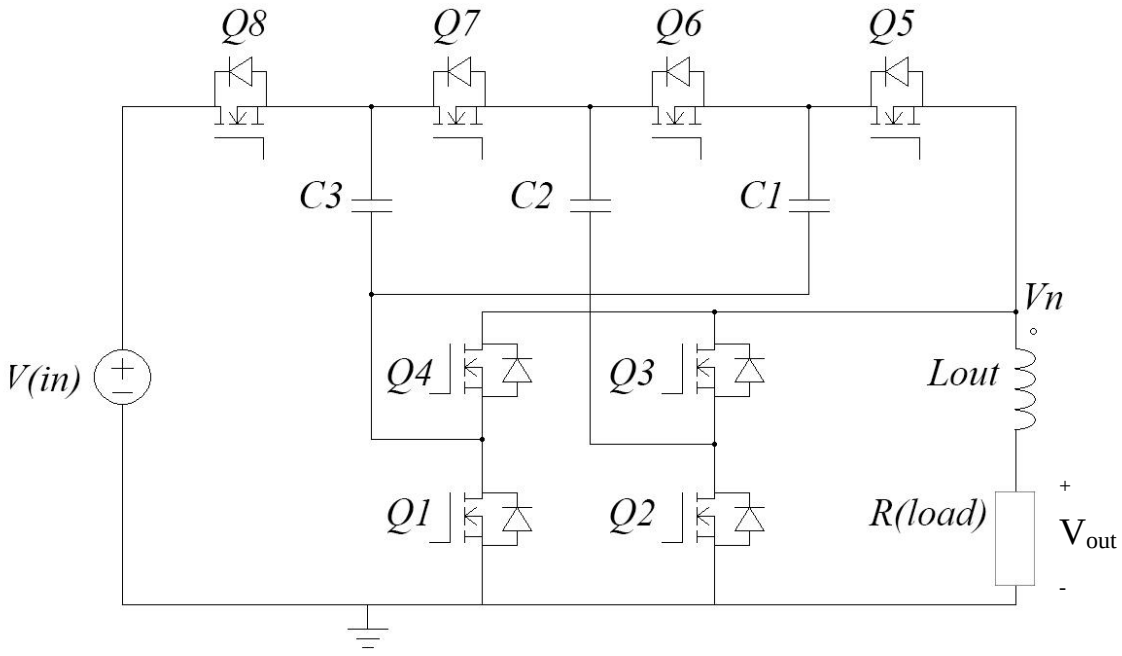

Figure 20: Circuit schematic of 8-switch 4-to-1 Dickson SCC

Prototype 1 of the 48 V to 12 V, 35 A split-phase Dickson SCC used an 8-switch design, as shown in the circuit diagram in Figure 20. As discussed in Chapter 2, switches Q6 and Q7 are expected to block a maximum of twice the output voltage (24 V), while all other switches are expected to block a maximum voltage equal to the output voltage (12 V). A large margin of voltage rating was desired for the switches due to the possibility of noise within the circuit should the flying capacitors turn out to be mismatched. Therefore,

MOSFET switches with 40 V ratings were selected for the 24 V switches, and MOSFET switches with 25 V ratings were selected for the 12 V switches. All MOSFET switches used for the first prototype have a 5 mm by 6 mm packaging.

A small output inductor was needed to ensure a continuous flow of current to the load throughout split-phase operation. A 200 nH output inductor was used for the first prototype. The list of components used to construct the power stage of Prototype 1 of the 48 V to 12 V, 35 A split-phase Dickson SCC is tabulated in Table 7.

Table 7: Other Components for Prototype 1 of the 48 V to 12 V, 35 A split-phase Dickson SCC

Component	Manufacturer Part #	Number Required
MOSFET (25V rating)	SIRC16DP-T1-GE3 [29]	6
MOSFET (40V rating)	BSC010N04LSI [30]	2
Inductor (200 nH)	PA3790.201HL [31]	1

4.2.2 Circuit Components for Prototype 2 of 48 V to 12 V, 35 A split-phase Dickson SCC

Prototype 2 of the 48 V to 12 V, 35 A split-phase Dickson SCC used a 10-switch design similar to the configuration described in [27]. The 10-switch Dickson SCC design effectively splits both switches Q1 and Q4 into two switches in parallel. This reduces the current stress experienced by these two switches (Q1 and Q4). In the 8-switch design, Q1 and Q4 both have maximum current stresses equal to the full load current. The splitting of the two switches in the 10-switch design results in each of the resulting four switches to experience a current stress equal to half of the load current. This allows a greater range of MOSFET switches to be selected. The 10-switch Dickson SCC schematic, along with the switching order for the circuit's switches, is shown in Figure 21. Note that switches Q1 and

Q4 from the 8-switch circuit configuration has been split into switches Q1a, Q1b, Q4a, and Q4b.

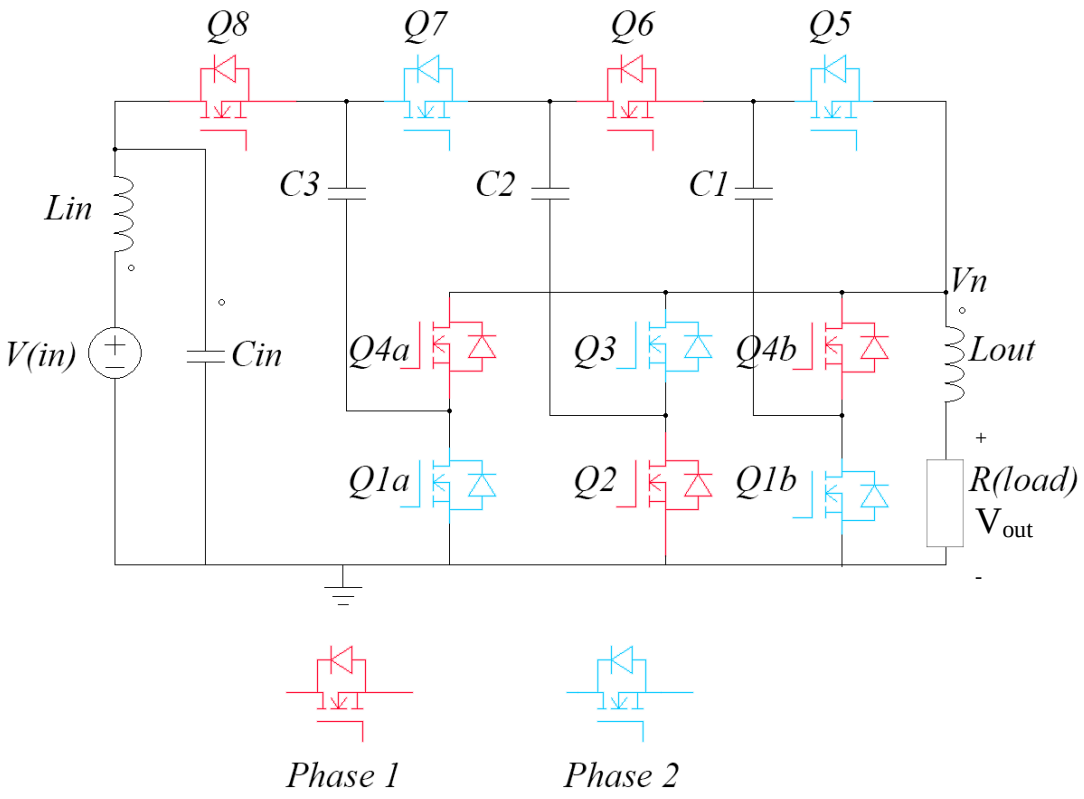

Figure 21: 10-switch 4-to-1 Dickson SCC with switching order illustrated

The splitting of switches Q1 and Q4 allowed the selection of smaller 3 mm by 3 mm MOSFET switches for switches Q1a, Q1b, Q4a, and Q4b to save space. All other components for the second prototype were identical to those used for the first prototype.

4.2.3 Input Filter Design

As discussed in Section 3.2 of this thesis, the split-phase Dickson SCC was found to exhibit a significant sensitivity to input voltage ripple. However, it was also found that the effect of input voltage ripple on the operation of the circuit decreases significantly as larger input capacitors are used. As the primary objective of the first prototype was to prove its feasibility in a high power, high current application, it was decided that the sensitivity

would be bypassed by simply using a large (2200 µF) input capacitor. While this guaranteed the reliability of the first prototype, upon conclusion of testing, it was found that the electrolytic input capacitor was responsible for a significant amount of power loss due to its inherently high ESR. Therefore, upon conclusion of testing for the first prototype of the high-current split-phase Dickson SCC, an input voltage ripple compensation method was developed using the existing split-phase control framework, to allow for the usage of smaller ceramic capacitors for future input filters. The development of this method is outlined Chapter 5.

4.3 Circuit Board Design

4.3.1 Prototype 1 PCB Design

As discussed in Chapter 1, some of the main benefits of utilizing the switched-capacitor converter are its compact size and therefore increased power density. Therefore, the circuit board for the first prototype was designed with space-efficiency in mind. The selected switching frequency of the prototype was 100 kHz; therefore, to minimize noise, the switches of the power stage were configured to be near each other, as well as other power stage components. The gate drivers for operating the MOSFET switches were placed directly beneath the switches themselves to minimize noise. The power stage copper traces were made as short and wide as possible to reduce power loss. The final design of the power stage of the printed circuit board (PCB) for the first 48 V to 12 V, 35 A split-phase Dickson SCC prototype was a spiral configuration, with switches Q8 to Q5 placed on the sides of the power stage in a circular formation, and switches Q4 and Q1 placed centrally. The flying capacitors were located in between the outer ring of switches and the centrally located switches. The input, output, and grounding pads of the PCB extend out from the

power stage to the edges of the board. The control components (such as the microcontroller) are placed to the side of the board. Compared to the power stage components and gate drivers, the control components are not as sensitive to noise. As such, the connections from the control components to the power stage components were made with thin traces. The configuration of the PCB for the first prototype of the 48 V to 12 V, 35 A split-phase Dickson SCC is shown in Figure 22. As shown in the PCB schematic, the input capacitor was originally to be implemented using ceramic capacitors. However, after simulations confirmed that the split-phase Dickson SCC exhibits significant sensitivities to input voltage ripple, the pads intended for the input capacitor were instead used to attach a larger electrolytic input capacitor to the circuit.

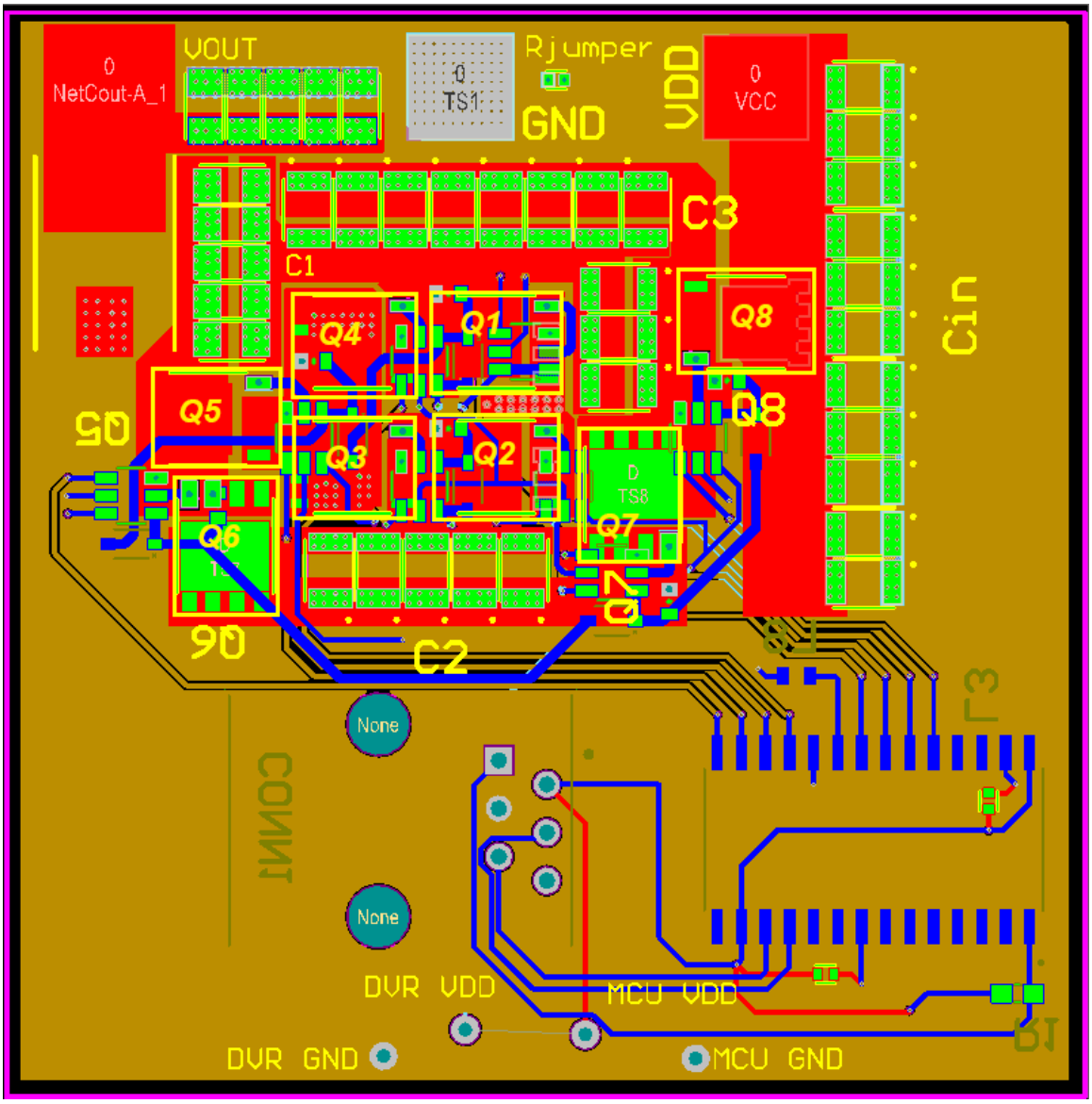

Figure 22: PCB configuration for first 48 V to 12 V, 35 A split-phase Dickson SCC prototype

4.3.1.1 Control system design

The control code for the microcontroller of the first 48 V to 12 V, 35 A split-phase Dickson SCC prototype was written using the MPLAB development environment. Split-phase operation is initiated in the microcontroller by first assigning pulse lengths and frequencies to individual PWM generators, then assigning the outputs of the PWM

generators to individual pins of the control chip, depending on the switch the pins are connected to. The full control code is shown in Appendix A.

A dead time of 75 ns was programmed into the pulse signals that control the switches of the circuit. Unlike ideal switches, which turn on and off immediately when the switching signal is applied or switched off, MOSFET switches transition between their off-state and on-state over a specific period (the turn-on and turn-off time). During these turn-on and turn-off times, the switch continues to conduct current. The introduction of dead time to the switch control is therefore necessary to prevent a situation where all the circuit's switches are conducting current simultaneously, which would cause short circuits and correspondingly, component failures.

Since the conversion ratio of SCCs are fixed by their physical configuration, open-loop control was employed for the 48 V to 12 V, 35 A split-phase Dickson SCC prototype. The control system block diagram is shown in Figure 23.

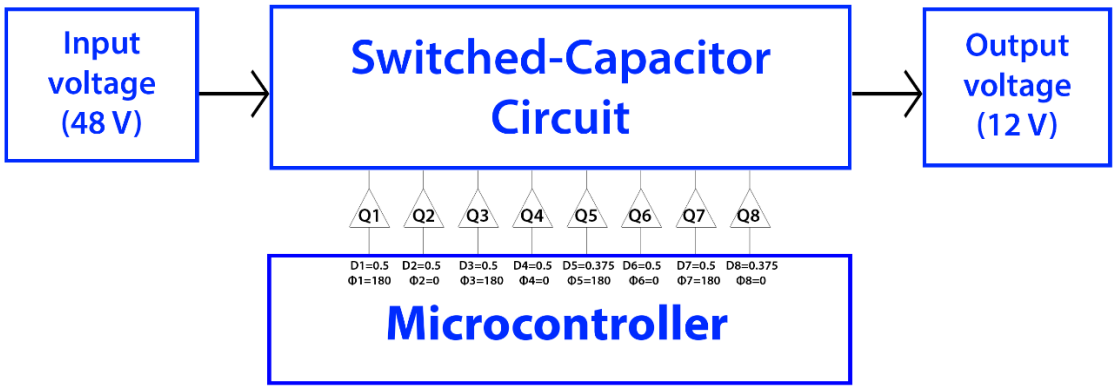

Figure 23: System Diagram of Prototype 1 of 48 V to 12 V, 35 A split-phase Dickson SCC

4.3.1.2 Prototype 1 Assembled Specifications

The overall board measures approximately 2 inches by 2 inches, with the power stage taking up a 1.125-inch by 1.563-inch space, for a total area of 1.76 in^2. When fully

assembled, with a height of 0.5 inches, the volume of the power stage was 0.88 in^3. With a maximum power output of 420 W, the power density of the power stage of Prototype 1 is 477 W/in^3. The power density of this prototype is around 20% (or 77 W/in^3) better than the two-phase 4-to-1 prototype tested in [27] which achieved a 400 W/in^3 power density. The top and bottom views of the power stage of the fully assembled first prototype is shown in Figure 24.

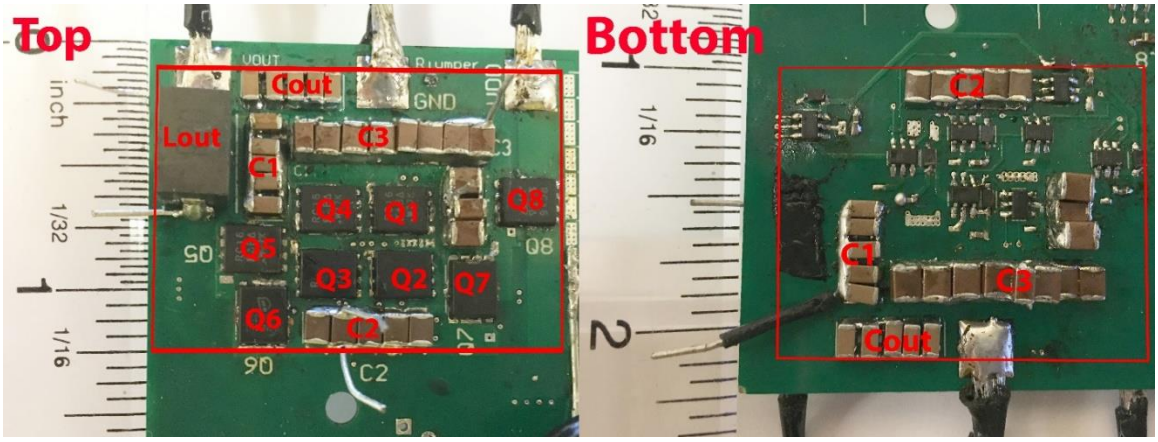

Figure 24: Top and bottom views of the assembled power stage of the first 48 V to 12 V, 35 A split-phase Dickson SCC prototype

4.3.2 Prototype 2 PCB Design

As mentioned in Section 4.2.2, the design of Prototype 2 is a 10-switch configuration, similar to that shown in [27]. Because switches Q1a, Q1b, Q4a, and Q4b are implemented using 3mm by 3mm MOSFET switches, the addition of two switches to the design did not cause a compromise in space-efficiency compared to Prototype 1.

The configuration of the PCB for Prototype 2 of the 48 V to 12 V split-phase Dickson SCC was completely redesigned. Instead of a spiral configuration of power stage components, a spinal configuration was adopted, with switches Q8 to Q5 making up the central spine of the power stage. The remaining six switches were placed on the outer edges

of the power stage to allow for better connections to ground, with the flying capacitors placed between the outer and central switches. The overall placements of the power stage components are also closer together. The current paths of the PCB were optimized to allow for shorter copper traces within the power stage compared to Prototype 1. The optimized current paths would allow for better power efficiency compared to the Prototype 1. The power stage, as well as the input/output stages, of the PCB for Prototype 2 of the 48 V to 12 V split-phase Dickson SCC, is shown in Figure 25.

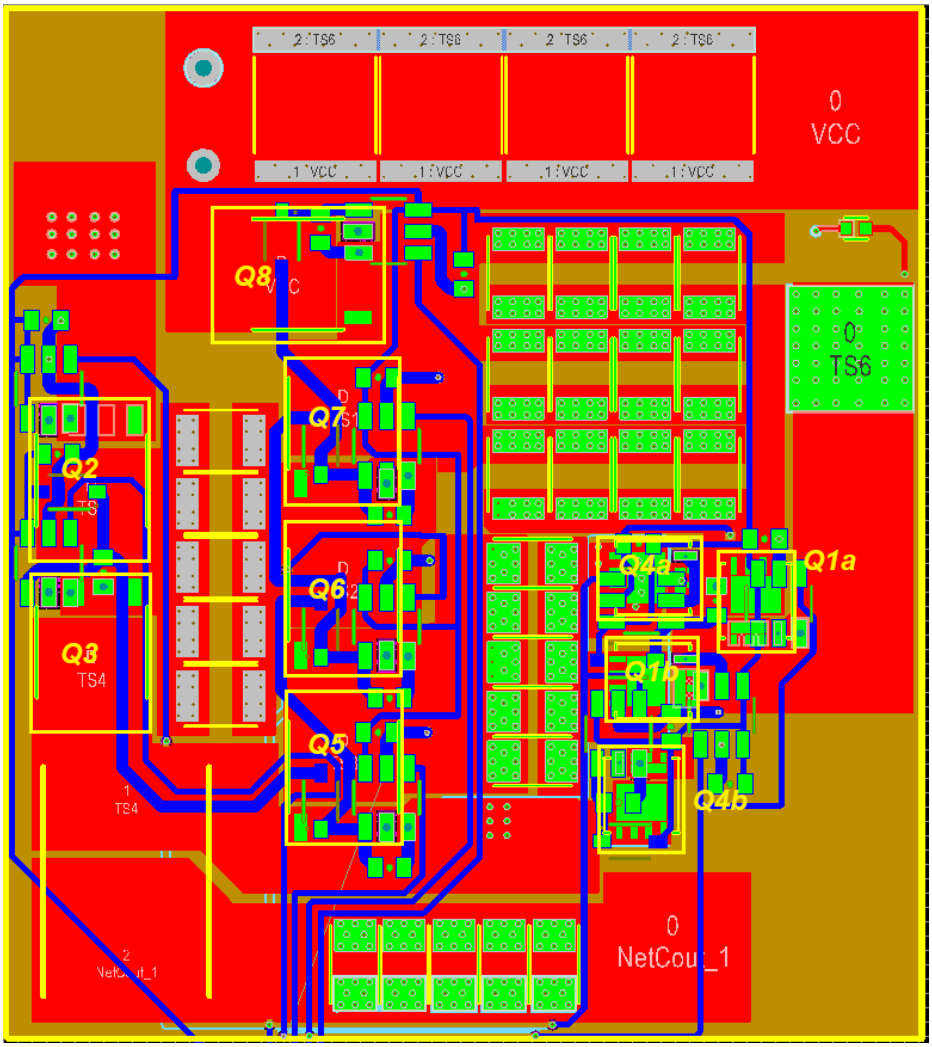

Figure 25: PCB configuration for power stage of second 48 V to 12 V, 35 A split-phase Dickson SCC prototype

The power stage of Prototype 2 takes up an area of 1.345 inches by 1.085 inches, for a total area of 1.46 in^2. This is an improvement of 0.32 in^2 in area compared to that taken up by the power stage of Prototype 1. The height of the completed prototype would have been 0.5 inches, identical to the height of Prototype 1. If Prototype 2 were to be fully assembled, the volume of the power stage would take up a space of 0.73 in^3. With a maximum output power of 420 W for an application with an output current of 35 A, the power density of the power stage of the second prototype would be 575 W/in^3. This is an improvement of nearly 100 W/in^3 compared to the power density of Prototype 1 and compared to the two-phase prototype tested in [27], the power density of the split-phase operated Prototype 2 is 44% (or 175 W/in^3) better.

The PCB for the second prototype of the 48 V to 12 V split-phase Dickson SCC is optimized for interleaved multi-phase implementation, due to the input and output pads being placed on opposite sides of the power stage area, rather than on the same side as with the first prototype. The final PCB design is a 4-circuit phase configuration, with the control components connected such that the operation of the four stages is interleaved with each other. This configuration allows testing and verification of both the single phase 35 A design, as well as interleaved designs with a maximum combined output current of 140 A. Figure 26 shows the final configuration of the PCB for the second 48 V to 12 V split-phase Dickson SCC, configured allow a maximum of 4 individual power stages to be implemented. Note that in this context, ‘circuit phase’ refers to a single power stage of an interleaved power circuit, rather than a circuit state during a switching cycle.

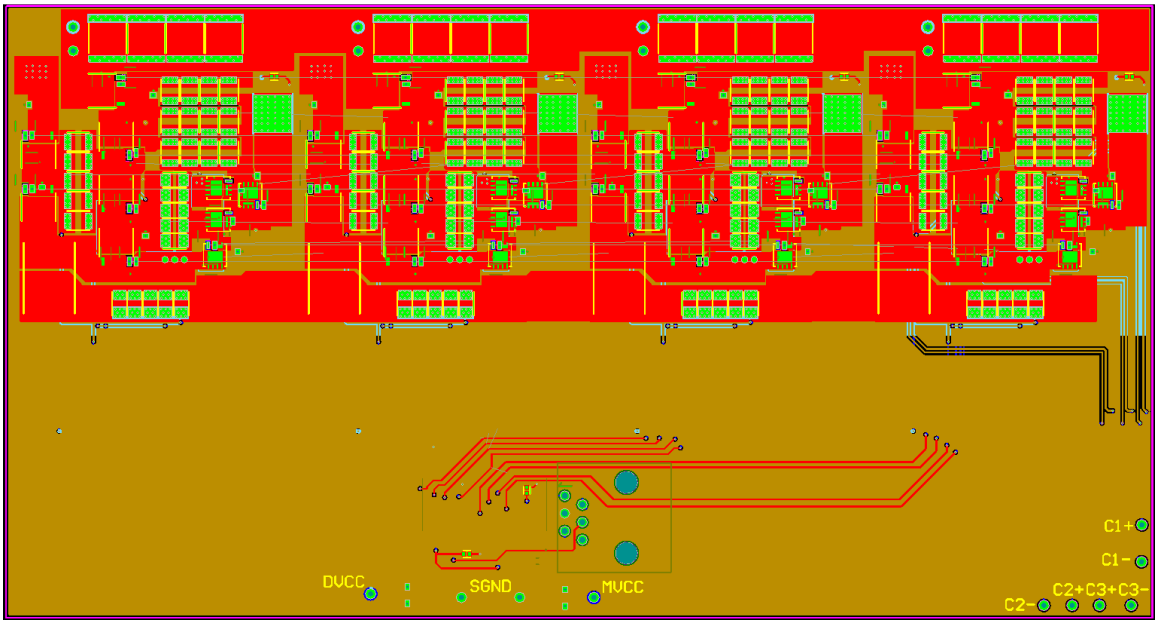

Figure 26: PCB configuration for second 48 V to 12 V split-phase Dickson SCC prototype. PCB configured to implement up to 4 power stages, for up to 140 A output current.

4.4 Conclusion

This chapter provided detailed discussions and analyses on the design processes for the two prototypes of the 48 V to 12 V, 35 A split-phase Dickson SCC. Using the analysis of the impact of flying capacitor mismatch on the operation of the split-phase Dickson SCC, it was determined that the flying capacitors for the split-phase prototypes should be matched according to the supplied de-rating curves of the ceramic capacitors used. Considering the possibility of inaccurate de-rating curves, as well as typical ceramic capacitor manufacturing tolerances of ±20%, an in-circuit flying capacitor measurement method was developed to allow verification of the actual capacitances of the flying capacitors, as well as allow fine-tuning of the prototype, if desired.

Due to the onset of the COVID-19 pandemic in early 2020, only Prototype 1 was able to be fully tested. The following chapter will provide test results obtained from Prototype 1, as well as further work resulting from the findings of prototype testing.

Chapter 5

Experimental Results

This chapter discusses the test results of Prototype 1 of the 48 V to 12 V, 35 A split-phase Dickson SCC. The efficiency curve, loss breakdown, and temperature profile of the prototype is presented and analyzed. This chapter also discusses performance improvements on the split-phase Dickson SCC prototype, as well as comparisons of the work presented in this thesis against existing implementations of SCCs. Furthermore, a proposed control method to mitigate the effects of input voltage ripple will be presented.

Due to the ongoing COVID-19 pandemic and the subsequent closure of labs, only Prototype 1 of the 48 V to 12 V, 35 A split-phase Dickson SCC was able to be tested. Therefore, the performance of the 10-switch 4-to-1 split-phase Dickson SCC, the configuration used for Prototype 2, will be analyzed through simulation, in both single-phase and two-phase interleaved configurations. The simulations of the 10-switch 48 V to 12 V split-phase Dickson SCC configuration are discussed in Sections 5.5 of this chapter.

5.1 Initial Test Results of Prototype 1 with Untuned Flying Capacitors

The split-phase Dickson SCC prototype was tested over a wide range of load conditions to analyze its performance in both light load conditions as well as maximum load conditions. This was accomplished using an electronic load connected to the output of the prototype. During the test, the output current was incrementally raised from 1 A to 35 A through the electronic load. A desk fan was utilized for temperature management throughout the test.

Table 8: Initial Prototype 1 Flying Capacitor Configurations

Capacitor size, maximum rated voltage, and nominal capacitance	Expected DC bias voltage	Expected de-rating at DC bias	Per-unit capacitance at expected DC bias	Units needed for 60µF
1210, 4.7 µF, 100 V rating (Capacitor C3)	36 V	-57%	2.02 µF	30
1210, 10 µF, 50 V rating (Capacitor C2)	24 V	-42%	5.8 µF	10
1206, 10 µF, 35 V rating (Capacitor C1)	12 V	-40%	6 µF	10

The 48 V to 12 V, 35 A split-phase Dickson SCC prototype, with the initial flying capacitor configuration shown in Table 8, achieved a peak efficiency of 98.6% at ¼ of the full load conditions, and achieved a full load efficiency of 96.0%. The efficiency curve attained by the prototype in initial testing is shown in Figure 27.

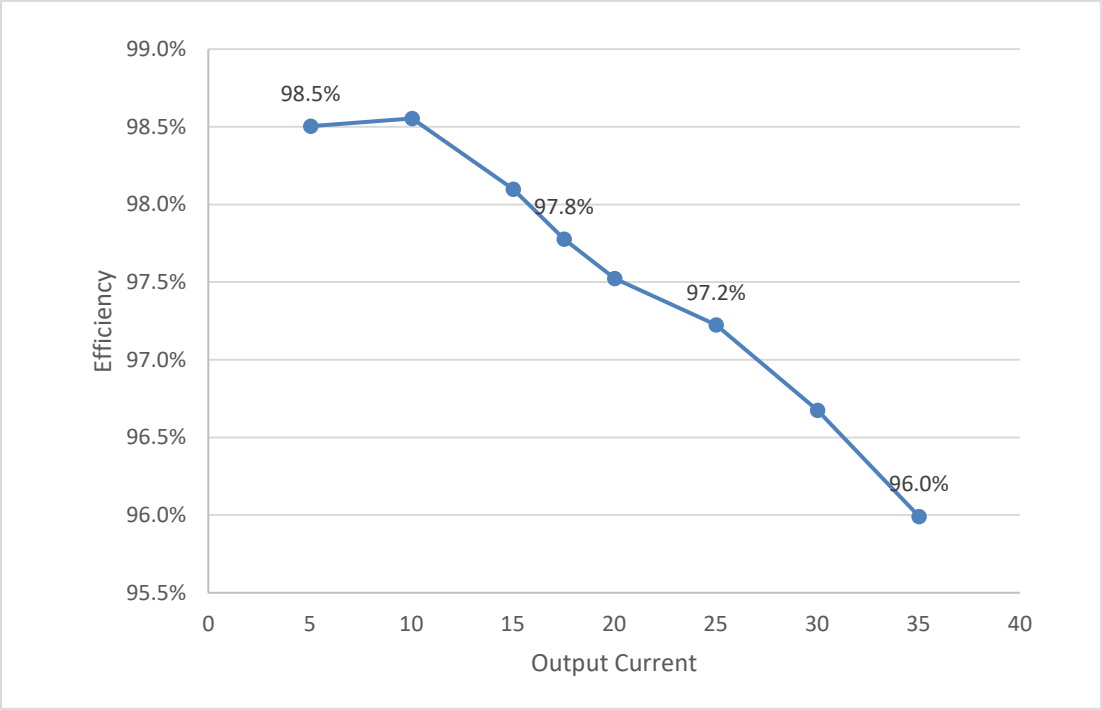

Figure 27: Efficiency curve for Prototype 1 of 48 V to 12 V, 35 A split-phase Dickson SCC; initial test results

The maximum temperature recorded on the prototype at full-load conditions was 80 °C. The thermal image obtained from the prototype at full-load conditions during initial testing is shown in Figure 28.

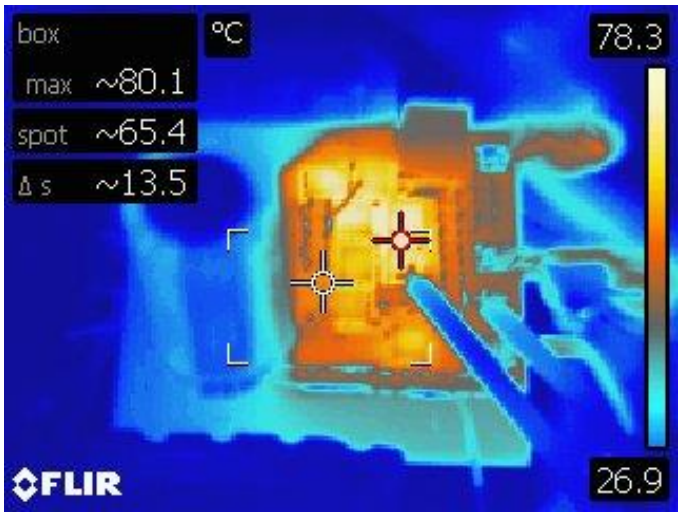

Figure 28: Thermal image of top side of Prototype 1 of 48 V to 12 V, 35 A split-phase Dickson SCC at full load. Initial test results

A theoretical loss model was constructed using Prototype 1's voltage, current, and efficiency figures obtained from testing, as well as the characteristics of the electrical components used in the prototype. The loss breakdown chart obtained from the loss model is shown in Figure 29.

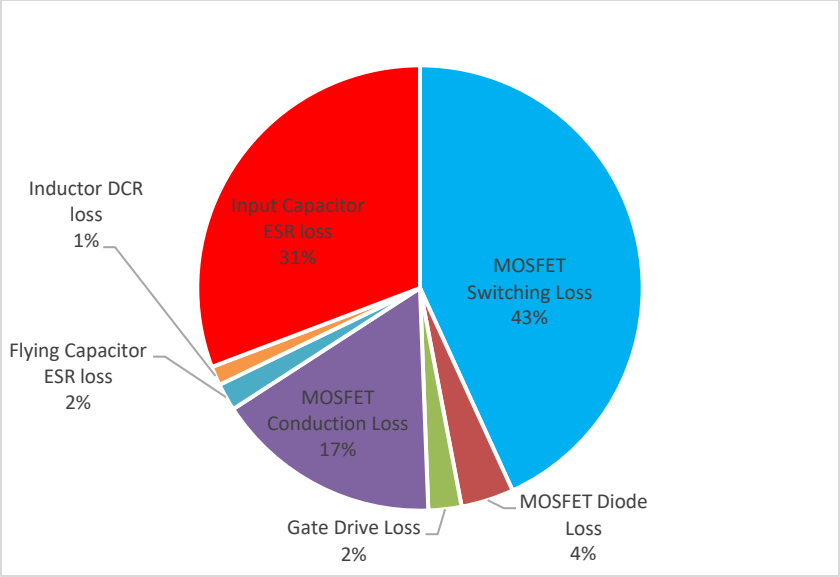

Figure 29: Loss breakdown chart for Prototype 1 of 48 V to 12 V, 35 A Dickson SCC

The loss breakdown chart shows that the predominant cause of power loss at full load is switching loss, accounting for 43% of total losses, followed by loss due to the input capacitor's ESR, accounting for 31% of total losses. Compared to the two-phase 48 V to 12 V Dickson SCC shown in [27], the initial test results showed that the split-phase prototype achieved a higher peak efficiency at 98.6% compared to 98% for the two-phase implementation, but slightly lower full-load efficiency, at 96% compared to around 96.3% for the two-phase implementation. The overall performance of the split-phase prototype is on par with the two-phase prototype in [27], however the split-phase prototype achieved a 19% better power density compared to the two-phase prototype.

5.1.1 Key Waveforms

Figures 30, 31, and 32 show the voltage waveforms for the flying capacitors C1, C2, and C3 of Prototype 1, respectively, under full load conditions.

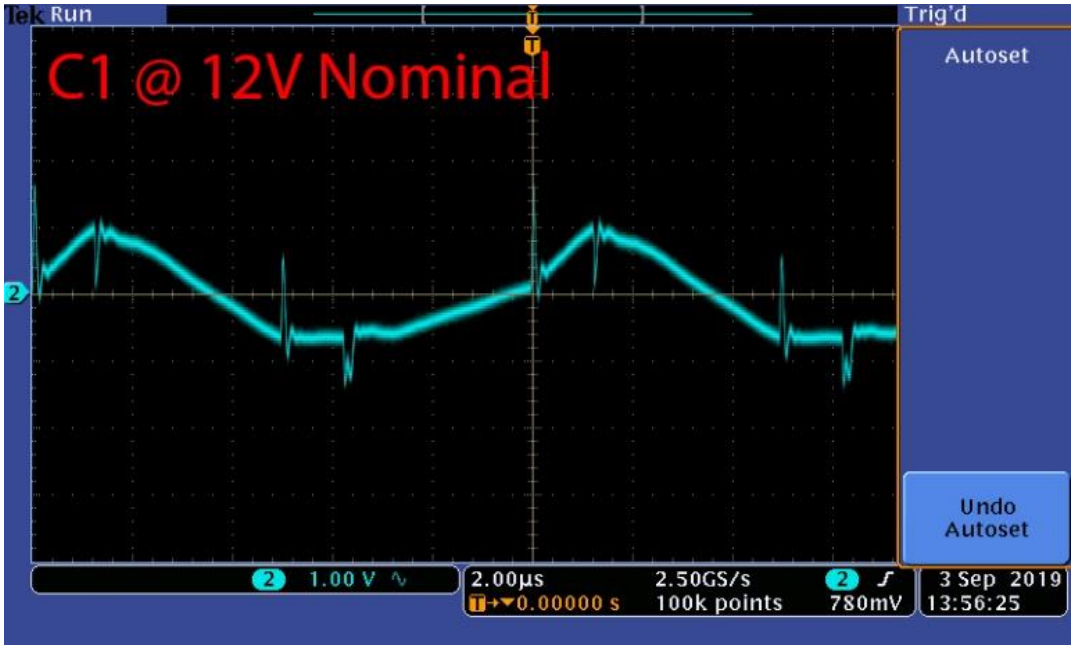

Figure 30: Voltage waveform of flying capacitor C1 at full load. Initial test results

Figure 31: Voltage waveform of flying capacitor C2 at full load. Initial test results

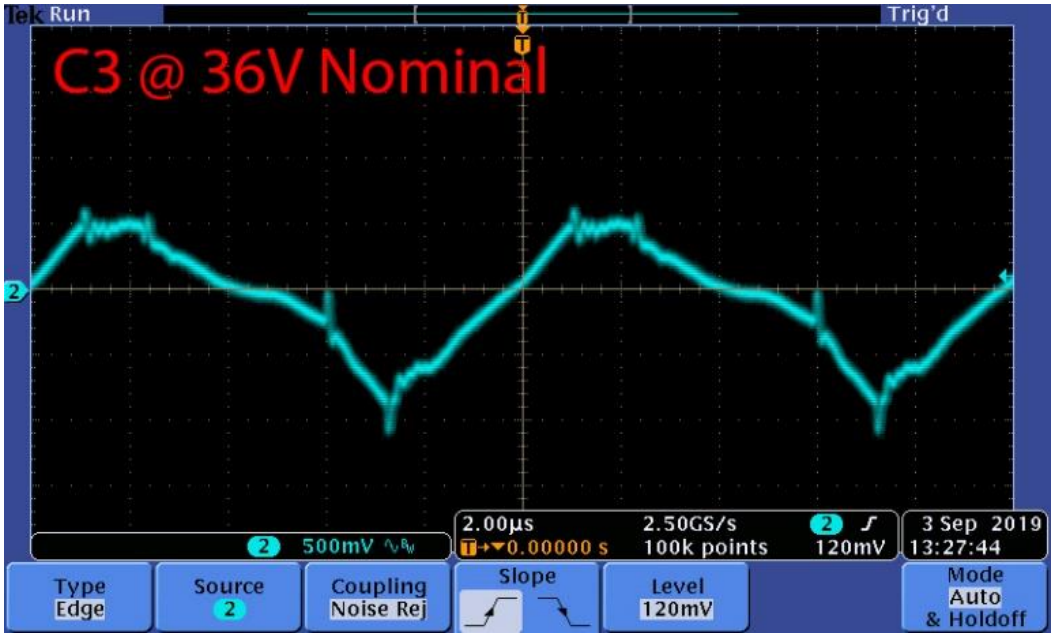

Figure 32: Voltage waveform of flying capacitor C3 at full load. Initial test results

The waveforms obtained during initial testing are relatively noise-free; the maximum amount of noise observed in full-load conditions was around 1.5 V through capacitor C1.

5.2 Flying Capacitor Measurement and Discussion

To investigate whether the performance of the split-phase Dickson SCC prototype could be improved, it was decided to utilize the in-circuit capacitor measurement method discussed in Section 4.1.1 to verify the values of the flying capacitors and therefore, observe whether flying capacitor mismatch was present. To gain an accurate measurement of the flying capacitor values, the flying capacitors were measured under both full-load (35 A output current) and half-load (15 A output current) conditions. The full-load waveforms of flying capacitors C3, C2, and C1, magnified to show the instance where the capacitors carry the full load current, are shown in Figures 33, 34, and 35, respectively.

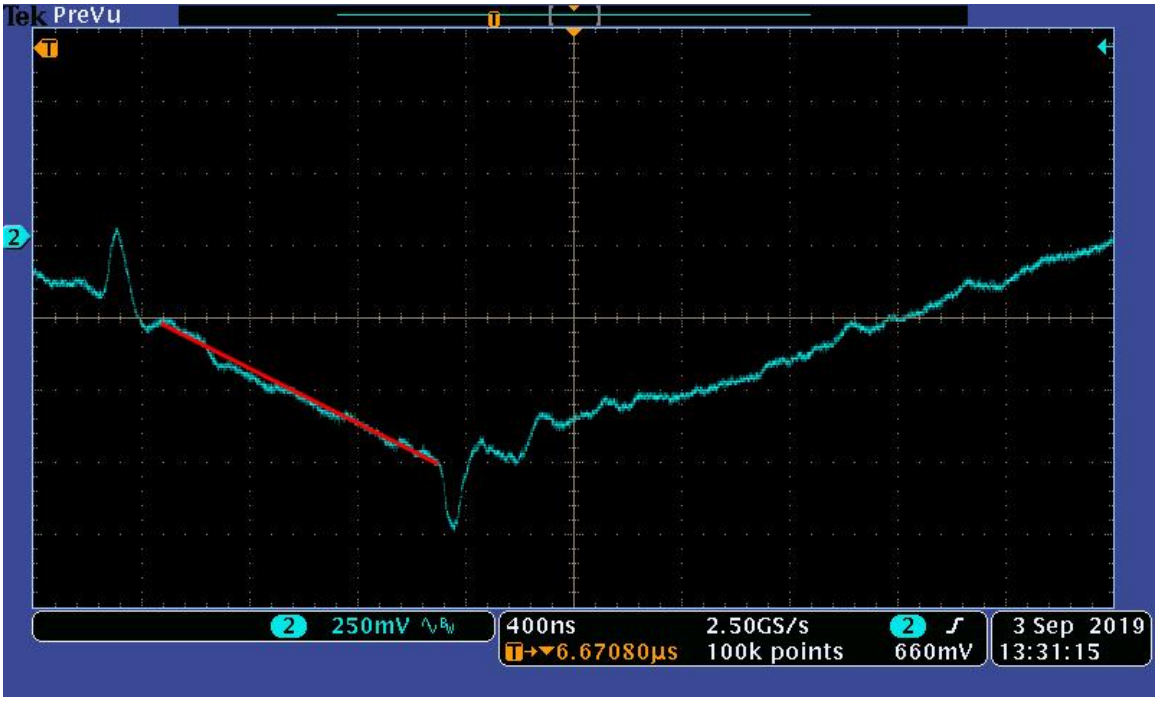

Figure 33: Full load, zoomed-in waveform of flying capacitor C3, used for capacitor measurements

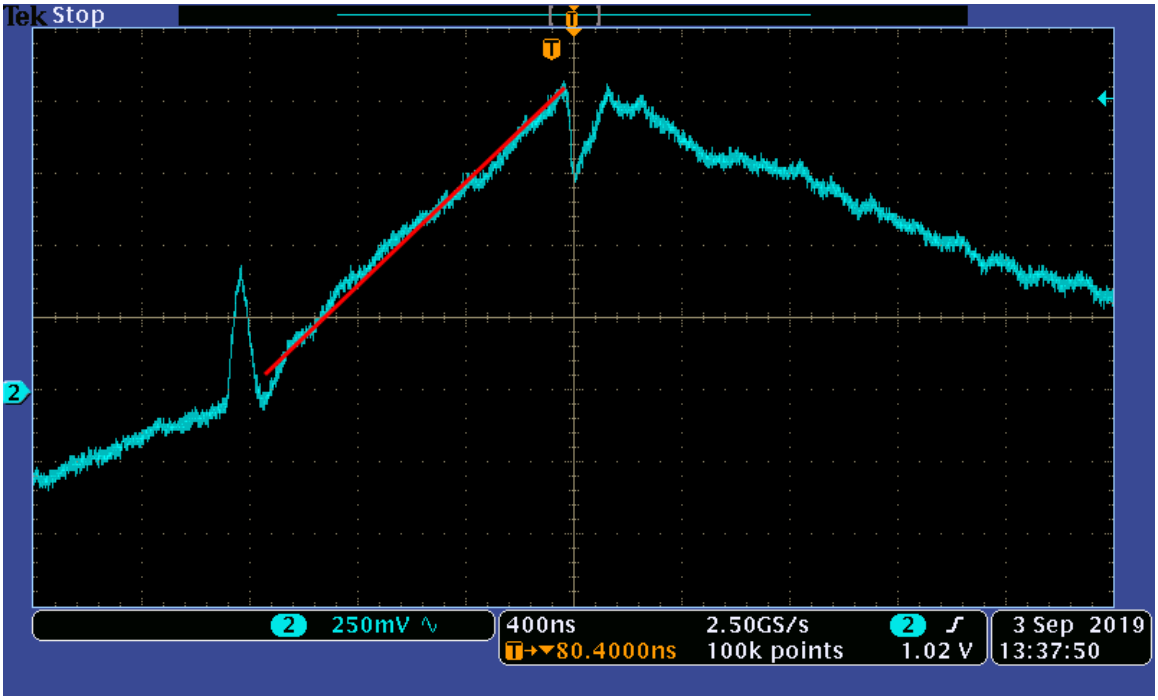

Figure 34: Full load, zoomed-in waveform of flying capacitor C2, used for capacitor measurements

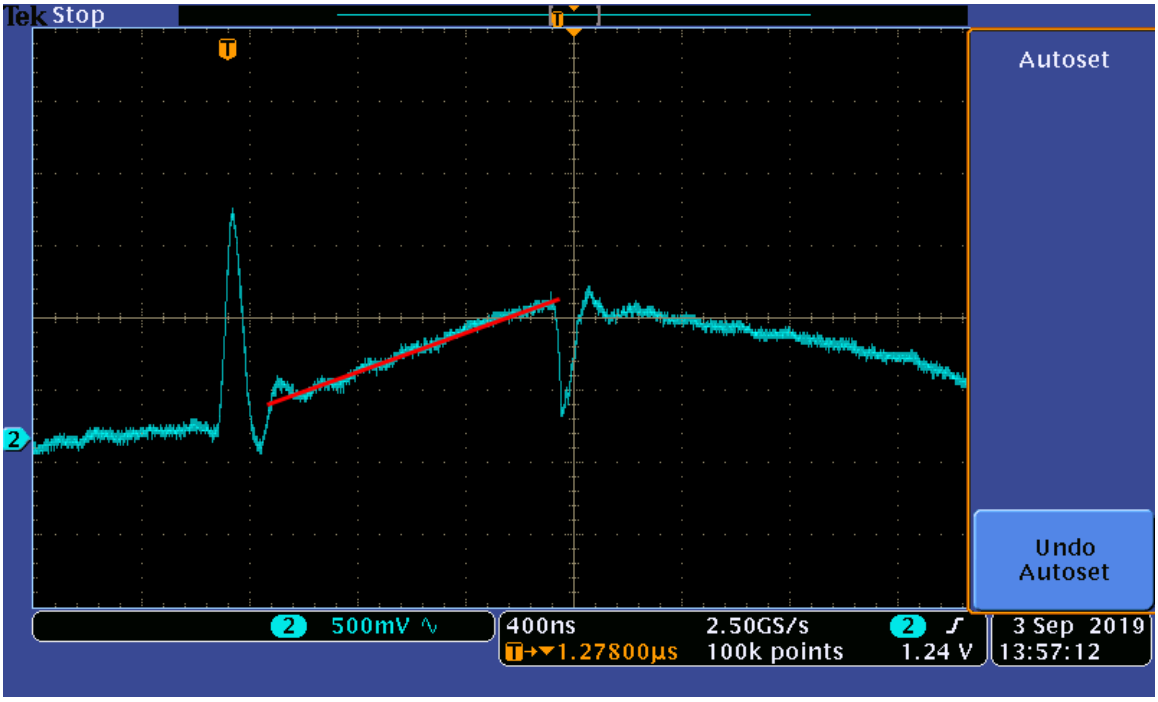

Figure 35: Full load, zoomed-in waveform of flying capacitor C1, used for capacitor measurements

Table 9 shows the flying capacitor values as measured under full load operating conditions via the capacitor measurement method derived in Section 4.1.1, using the three figures presented above.

Table 9: Expected versus measured prototype flying capacitor sizes, full load measurements

Flying Capacitor and total nominal capacitance	Expected voltage de-rating	Expected total capacitance	Real capacitance (Full load measurements)	Actual de-rating
C3=30x4.7µF	-57%	60.6 µF	78.7 µF	-44.2%
C2=10x10 µF	-42%	58 µF	39.2 µF	-60.8%
C1=10x10 µF	-40%	60 µF	54 µF	-46%

The half-load waveforms of flying capacitors C3, C2, and C1, magnified to show the instance where the capacitors carry the full load current, are shown in Figures 36, 37, and 38.

Figure 36: Half load, zoomed-in waveform of flying capacitor C3, used for capacitor measurements

Figure 37: Half load, zoomed-in waveform of flying capacitor C2, used for capacitor measurements

Figure 38: Half load, zoomed-in waveform of flying capacitor C1, used for capacitor measurements

Table 10 shows the flying capacitor values as measured under full load operating conditions via the capacitor measurement method derived in Section 4.1.1, using the three figures presented above.

Table 10: Expected versus measured prototype flying capacitor sizes, half load measurements

Flying Capacitor and total nominal capacitance	Expected voltage de-rating	Expected total capacitance	Real capacitance (Half-load measurements)	Actual de-rating
C3=30x4.7µF	-57%	60.6 µF	78 µF	-44.7%
C2=10x10 µF	-42%	58 µF	40 µF	-60%
C1=10x10 µF	-40%	60 µF	55.4 µF	-44.6%

A comparison between the actual and expected flying capacitor values shown in Tables 9 and 10 shows that, while some flying capacitors experienced less de-rating than expected, others experienced more de-rating than expected. The most significant anomalies between the measured and expected capacitance values were observed in capacitors C3 and C2. The

ceramic capacitors used for C3 were seen to have de-rated by around 44% at 36 V during testing, less than the 57% derating specified from its datasheet [32]. The capacitors used for C2 were seen to have de-rated by around 60% at 24 V during testing, significantly more than the 42% derating specified from its datasheet. The capacitors used for C1 de-rated roughly as expected [33], but its measured capacitance is still a bit different from the expected capacitance. These measurement results exemplify the variances in capacitance that can result from potential inaccuracies in the de-rating curves, as well as manufacturing tolerance.

Regarding the anomaly between the expected and actual de-ratings of the ceramic capacitors used for C2, the de-rating of the flying capacitors used at 24 V (the blocking voltage of C2) listed on the characterization sheet at the time of design was around 42%. The most recent characterization sheet for the ceramic capacitor used for C2 lists the de-rating at 24 V to be around 55% [34]. The most recent figure of de-rating is much closer in value to the actual de-rating observed through the in-circuit measurement method (60%). Therefore, it can be confirmed using the most recent datasheets that an error in the de-rating curve for the capacitors used for C2 was present at the time of design.

The comparison between the expected and measured flying capacitor values shown above confirms that potential inaccuracies in the supplied ceramic capacitor de-rating curves, together with manufacturing tolerances, are the primary sources of flying capacitor mismatch in real-world implementations of the split-phase Dickson SCC. Due to these factors, some fine-tuning may be necessary to improve the performance of the converter. However, it should be noted that, despite the inaccurate de-rating curves and the variations in capacitance due to manufacturing tolerance, the prototype with its flying capacitors

matched solely through referral to the supplied de-rating curves still delivered satisfactory performance.

5.3 Prototype Performance with Tuned Flying Capacitors

It has been previously shown through simulations in Section 3.1.1 that operation with fully matched flying capacitors results in little to no current transients through the capacitors during switching. This corresponds to reduced switching and conduction losses within the split-phase Dickson SCC.

Using the capacitance of flying capacitor C3 as a base value, additional ceramic capacitors were added to both C2 and C1 to increase their capacitances, such that they are aligned with the capacitance of C3, Using the per-unit measured capacitance values for the ceramic capacitors used for C2 and C1 (4 µF per unit at 24 V for C2, and 5.54 µF per unit at 12 V for C1), 9 more ceramic capacitors were added to capacitor C2 (for a total of 19), while 5 more ceramic capacitors were added to capacitor C1 (for a total of 15). The tuned 48 V to 12 V, 35 A split-phase Dickson SCC prototype was tested from light load to full load to analyze its performance relative to its initial configuration with the mismatched flying capacitors. A comparison of efficiency curves resulting from operation with fully matched flying capacitors and operation with the initial mismatched capacitors is shown in Figure 39.

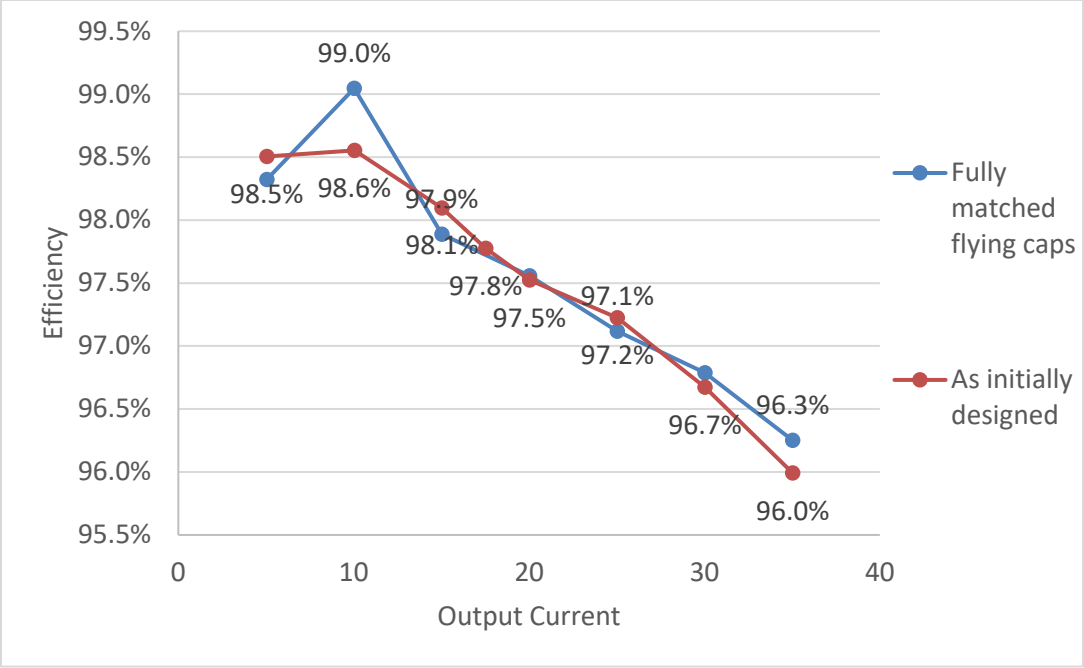

Figure 39: Comparison of efficiency curves for first 48 V to 12 V, 35 A split-phase Dickson SCC prototype. Efficiency curve for prototype with fully matched flying capacitors shown in blue. Initial efficiency curve shown in red.

With fully matched flying capacitors, the prototype's overall efficiency improved by 0.3 to 0.4%, with a peak efficiency of 99% attained at a load of 10 A, and a full load efficiency of 96.3%. The full load efficiency of the tuned split-phase prototype is on par with the two-phase prototype discussed in [27], while the peak efficiency of the tuned split-phase prototype, at 99%, is far higher than the peak efficiency attained by the two-phase prototype in [27], which was 98%.

The power loss reduction between the operation of the tuned prototype and the operation of the prototype with the initial mismatched flying capacitors was around 1 W at full load conditions. The tuned prototype experienced full-load power losses of 15 W, down from 16 W experienced by the untuned prototype. Therefore, the percentage of loss reduction between operation with fully matched flying capacitors and operation with the initial mismatched flying capacitors was 6.25%.

The temperature profile of the tuned prototype has also seen slight improvements, with a maximum temperature of 78.7 °C recorded at full load operation. Figure 40 shows the thermal image of the top side of the tuned prototype during full load conditions.

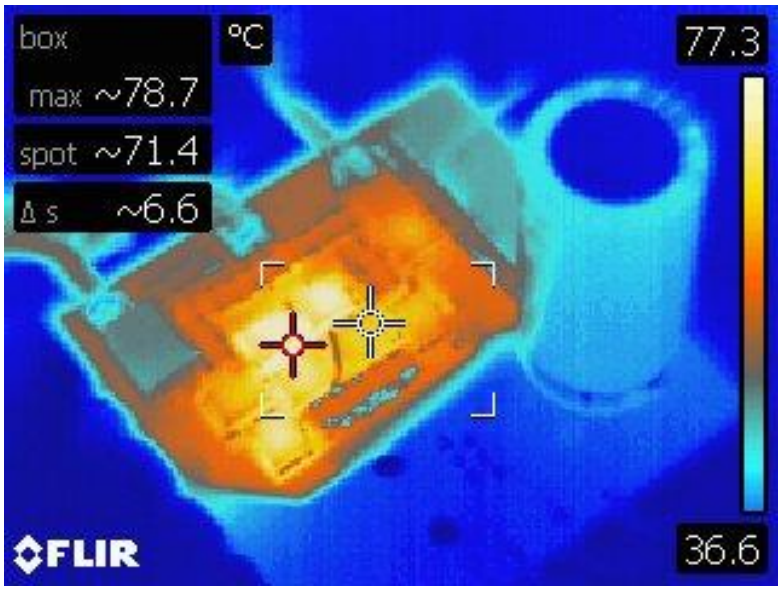

Figure 40: Thermal image of top side of prototype at full load, with fully matched flying capacitors

Therefore, it can be concluded from testing of the tuned prototype that it is important to ensure that the values of the flying capacitors of the split-phase Dickson SCC are matched as closely as possible, giving consideration to the fact that ceramic capacitors de-rate when subjected to a DC voltage bias. Fully matched flying capacitors ensures best performance of the split-phase Dickson SC converter. Due to the possibility of inaccuracies in the supplied de-rating curves, as well as the potential for component variations due to manufacturing tolerances, it may be necessary to tune the flying capacitors to further optimize performance. However, it has also been shown that despite the possibilities of inaccurate de-rating curves and component variations due to manufacturing tolerance, designing the flying capacitors based on the supplied de-rating curves still resulted in a reliably performing prototype.

As previously discussed, the electrolytic input capacitor was a major source of power loss in Prototype 1. Therefore, at the conclusion of testing for this prototype, a method to compensate for the effects of input voltage ripple was developed. The motivation behind developing the compensation method was to allow the use of smaller ceramic capacitors to serve as the input capacitor. This would result in better power efficiency, as well as space savings, on the split-phase Dickson SCC. The derivation and testing of this method through circuit simulation is discussed in the following section of this chapter.

5.4 Proposed Input Voltage Ripple Compensation Method

As discussed in Chapter 3, the operation of the input capacitor at smoothing out the input current causes the input voltage to exhibit ripple. Therefore, some intuitive methods of compensating for input voltage ripple would be to either use a large input capacitor, or to implement voltage sensing circuitry within the circuit, in order to ensure that the switches operate such that the equivalent circuit branch voltages always become matched during switching.

While utilizing large input capacitors does indeed remove the effect of input voltage ripple within the split-phase Dickson SCC, larger capacitors tend to be the electrolytic type, with inherently large equivalent series resistance (ESR) values that result in increased power losses within the circuit. As shown in the loss breakdown chart in Figure 29, the electrolytic capacitor used as the input capacitor for Prototype 1 contributed to around 31% of the total power losses at full load. Furthermore, electrolytic capacitors tend to be physically bulky, therefore space would need to be set aside for them, potentially causing a decrease the circuit's power density.

Implementing voltage sensing circuitry in the circuit would allow an increase in efficiency since the large input capacitor is no longer needed, but along with taking up space, sensing circuits tend to be complicated to implement. One other method, proposed in this subsection, can be theorized from the existing split-phase control theory.

As discussed in Chapter 2, the split-phase control method controls the charging and discharging of the flying capacitors to allow them to satisfy the output node voltage equations before switching takes place (shown in Equations 10 and 11), thereby eliminating charge redistribution.

$$\Delta V_{n\ (Phase\ 1)} = (V_{IN} - V_{C3}) - (V_{C2} - V_{C1}) \tag{10}$$

$$\Delta V_{n\ (Phase\ 2)} = (V_{C3} - V_{C2}) - (V_{C1}) \tag{11}$$

This capacitor voltage control is realized through the imposition of reduced duty cycles on some of the circuit's switches. Therefore, it was hypothesized that, if these switches with reduced duty cycles (referred to as 'split-phase' switches) allow the control of the flying capacitor voltages such that the node voltage equations are satisfied during switching, these same switches could, in theory, further control the charging behaviors of the flying capacitors, such that the additional voltage difference during switching caused by input voltage ripple is compensated for. This would be done by adjusting the duty cycles of these 'split-phase' switches, thereby allowing the flying capacitors to charge and discharge for either a longer or shorter period, potentially reducing the voltage differences during switching caused by input voltage ripple. In practice, this technique would be simple to implement, as the only modification needed to be made on the physical circuit is to slightly adjust the signal pulse length of the microcontroller's PWM output controlling one or more of the 'split-phase' switches. Space for sensing circuitry or large components are

not necessary with this form of compensation, thus potentially offering improvements in power density and efficiency.

As will be shown in the following discussion and analysis, the efficacy of adjusting the duty cycles of the ‘split-phase’ switches to compensate for the effects of input voltage ripple has been confirmed through model analysis, and further verified through circuit simulation. However, due to the ongoing COVID-19 pandemic, prototype testing to verify the efficacy of this method in practice is not possible.

5.4.1 Model Analysis of Duty Cycle Tuning Strategy

First-order models for the flying capacitor voltages were derived using first principles to investigate the effect of tuning duty cycles on reducing equivalent circuit branch voltage differences during switching. The following assumptions were made in deriving the first-order models: (1) that the currents through the flying capacitors were piecewise-constant waveforms, (2) that the average voltages of the flying capacitors have ideal behavior, (3) that the components were ideal (i.e: no ESR) and (4) that there is no transient voltage behavior during switching. Making these assumptions when deriving the flying capacitor voltage models meant that the model could not be used to precisely predict the results of any given ‘split-phase’ duty cycle change, but the results from model analysis provided a general idea on what would occur if the ‘split-phase’ duty cycles were slightly modified. The details of the model derivation can be found in the following subsection.

5.4.1.1 Example of Derivation of Flying Capacitor Voltage Models

The spit-phase Dickson SC converter’s switching pattern is Phase 1-1b-2-2b. In ideal operating conditions, phases 1 and 2 both last for 37.5% of the switching period, while

phases 1b and 2b both last for 12.5% of the switching period. The simplified equivalent circuits of these four phases are shown in Figure 41.

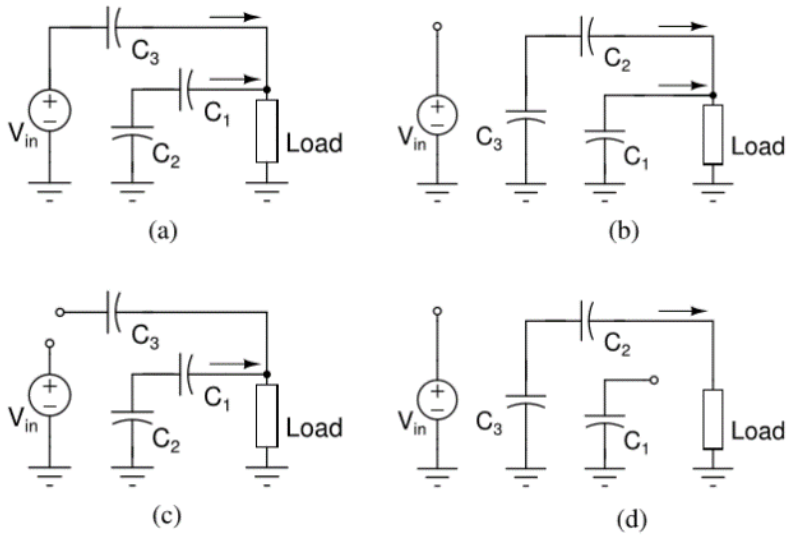

Figure 41: Simplified equivalent circuits for 4-to-1 split-phase Dickson SCC

The equivalent circuits are essentially capacitor dividers. With three flying capacitors in the 4-to-1 configuration of the Dickson converter, each equivalent circuit branch will have either one or two flying capacitors connected in series. During switching phases with two branches conducting (Phases 1 and 2; Figures 41a and 41b), the branch with fewer flying capacitors carries 2/3 of the output current, while the branch with more flying capacitors carries 1/3 of the output current. During switching phases with only one branch conducting current (Phases 1b and 2b; Figures 41c and 41d), that branch carries the full load current throughout the switching phase. The following is the derivation for the voltage model for flying capacitor C3. The voltage models for capacitors C2 and C1 were derived using the same method.

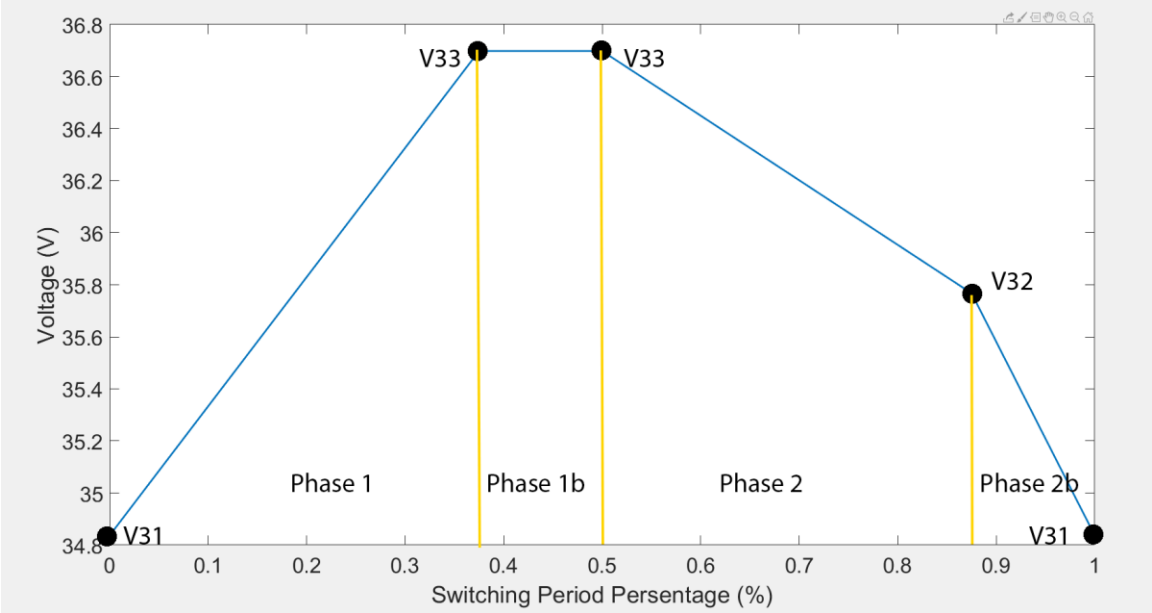

Figure 42: Modelled voltage waveform of Capacitor C3

Figure 42 shows the voltage waveform for one switching period for flying capacitor C3. During phase 1 (the first 37.5 % of the switching period), C3 is connected between the input source and the load; thus, it is being charged by the input source from V_{31} to V_{33}. The other two flying capacitors, C2 and C1, are connected in series between ground and the load, parallel to C3. Therefore, C3 carries 2/3 of the load current in phase 1. In phase 1b, C3 is left floating due to switch Q8 cutting it from the input source; therefore, it does not conduct during this phase, and its voltage stays at V_{33}. In phase 2, C3 and C2 are connected in series, between ground and the load, while C1 is connected between ground and the load, parallel to C3 and C2. During this phase, C3 discharges into C2, while carrying 1/3 of the load current. C3's voltage decreases from V_{33} to V_{32} during phase 2. In phase 2b, with C1 cut off from the circuit due to switch Q8 switching off, C3 (as well as C2) carries the full current load. C3's voltage further decreases from V_{32} to V_{31} during phase 2b.

Throughout the switching period, C3 blocks an average of three times the output voltage.

Superposition was used to derive the flying capacitor voltage models, by first assuming zero DC bias to determine the values of the voltage points V_{31}, V_{33}, and V_{32}. The DC bias voltage was added to those values afterwards to obtain the final flying capacitor voltage model.

From the above inferred voltage waveform, the differences in capacitor voltage between the various points along the waveform can be written as such:

$$V_{33} - V_{31} = \frac{\frac{2}{3} I_O D_8 T}{C_3} \tag{12}$$

$$V_{32} - V_{33} = \frac{-\frac{1}{3} I_O D_5 T}{C_3} \tag{13}$$

$$V_{31} - V_{32} = \frac{-I_O (0.5 - D_5) T}{C_3} \tag{14}$$

Where D_8 and D_5 are the duty cycles of switches Q8 and Q5, respectively, T is the switching period and is the inverse of the switching frequency, and I_o is the output current.

It was also noted that since the average capacitor voltage without DC bias was 0, the integral of the waveform over one switching cycle should thus equal 0. This equation can be written as such:

$$\int_0^{D_8 T} \left(\frac{V_{33} - V_{31}}{D_8 T} t + V_1 \right) dt + \int_0^{(0.5 - D_8)T} V_{33} dt + \int_0^{D_5 T} \left(\frac{V_{32} - V_{33}}{D_5 T} t + V_3 \right) dt + \int_0^{(0.5 - D_5)T} \left(\frac{V_{31} - V_{32}}{(0.5 - D_5) T} t + V_2 \right) dt = 0 \tag{15}$$

Substituting equations 12, 13, and 14 into equation 15, the sum of integrals becomes:

$$\int_0^{D_8 T} \left(\frac{\frac{2}{3} I_O}{C_3} t + V_{31} \right) dt + \int_0^{(0.5 - D_8)T} V_{33} dt + \int_0^{D_5 T} \left(\frac{-\frac{1}{3} I_O}{C_3} t + V_{33} \right) dt + \int_0^{(0.5 - D_5)T} \left(\frac{-I_O}{C_3} t + V_{32} \right) dt = 0 \tag{16}$$

The equation after evaluating the antiderivatives becomes:

$$\left(\frac{\frac{2}{3}I_O}{2C_3}t^2 + V_{31}t\right)\Big\{_{0}^{D_8T} + V_{33}t\Big\{_{0}^{(0.5-D_8)T} + \left(\frac{-\frac{1}{3}I_O}{2C_3}t^2 + V_{33}t\right)\Big\{_{0}^{D_5T}$$
$$+ \left(\frac{-I_O}{2C_3}t^2 + V_{32}t\right)\Big\{_{0}^{(0.5-D_5)T} = 0$$

(17)

Evaluating equation 17 using the bounds gives:

$$\frac{\frac{2}{3}I_O(D_8T)^2}{2C_3} + V_{31}D_8T + V_{33}(0.5-D_8)T + \frac{-\frac{1}{3}I_O(D_5T)^2}{2C_3} + V_{33}D_5T + \frac{-I_OT^2(0.5-D_5)^2}{2C_3}$$
$$+ V_{32}(0.5-D_5)T = 0$$

(18)

The terms V_{31}, V_{32}, and V_{33} can all be written in terms of each other through rearranging of equations 12, 13, and 14. These can thus be substituted into Equation 18 to give the following voltage point equations. Note that these expressions are un-simplified; these expressions were tested in Matlab as is, to verify that the model was accurate compared to PSIM simulation results.

$$V_{31} = \frac{I_OT\left(-\frac{2}{3}D_8^2+\frac{1}{3}D_5^2-(0.5-D_5)^2-\frac{4}{3}D_8(0.5-D_8)-\frac{4}{3}D_8D_5\right)}{2C_3} \quad (19)$$

$$V_{32} = \frac{I_OT\left(-\frac{2}{3}D_8^2-\frac{1}{3}D_5^2+(0.5-D_5)^2+2D_8(0.5-D_5)-\frac{2}{3}D_5(0.5-D_8)\right)}{2C_3} \quad (20)$$

$$V_{33} = \frac{I_OT\left(\frac{2}{3}D_8^2+\frac{1}{3}D_5^2+(0.5-D_5)^2+\frac{2}{3}D_5(0.5-D_5)\right)}{2C_3} \quad (21)$$

Note that the above expressions assume no DC bias on the capacitor. The capacitor voltage waveform points given a DC bias on the capacitor can be calculated by simply adding the expected average DC bias value to the voltage point equations (hence, superposition). For example, to calculate point V_{31} given a DC bias of $3V_o$ on the flying capacitor (as is the case with capacitor C3), one first substitutes in the duty cycle, switching

period, capacitance, and the output current values into Equation 19, then adds the constant $3V_o$ to the calculation result to get the final value.

5.4.1.2 Model Analysis and Discussion

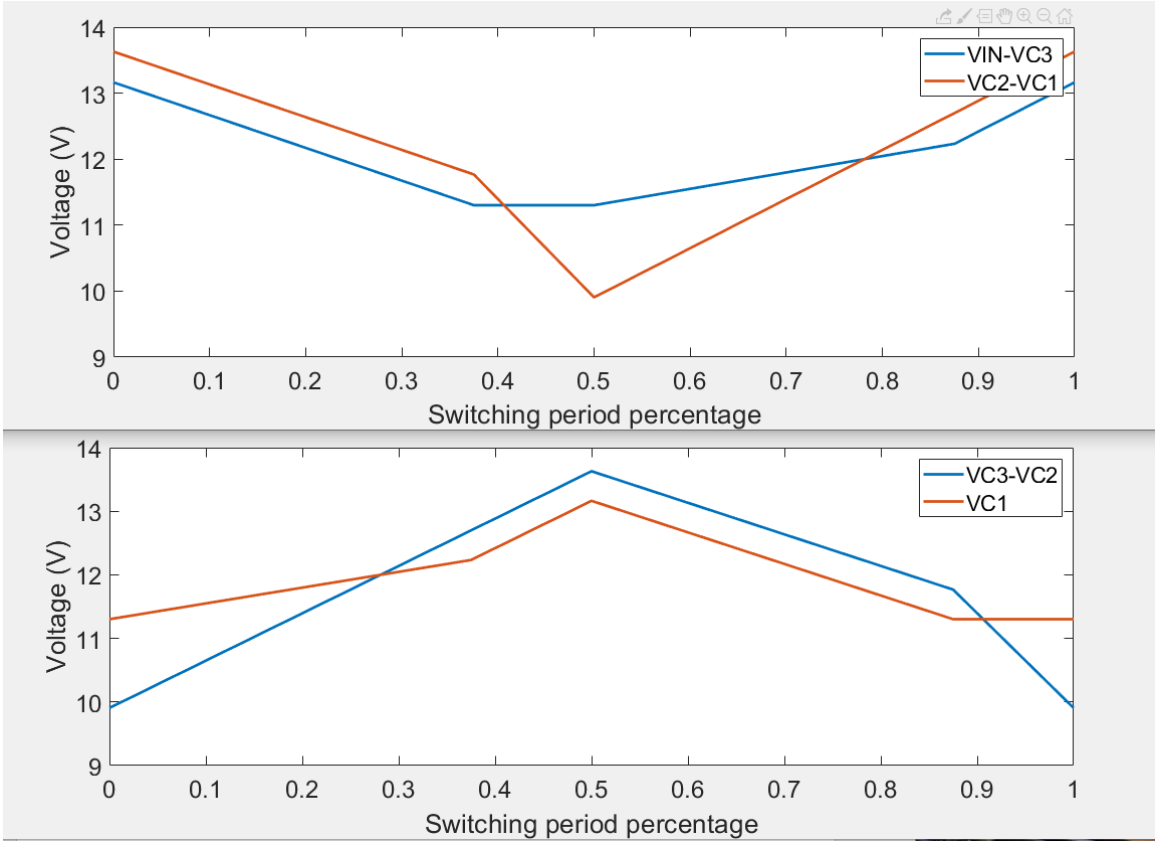

Figure 43: Modelled Phase 1 and Phase 2 equivalent circuit branch voltage waveforms (First order approximation, No input voltage ripple, D5 = D8 = 0.375)

Figure 43 shows the equivalent circuit branch voltages of the 4-to-1 Dickson converter, obtained using the flying capacitor voltage model, when the 'split-phase' duty cycles of both switch Q5 and Q8 (refer to Figure 1) were set to 37.5%, which is the duty cycle value for split-phase operation in ideal conditions, given in [20]. The model output in Figure 42 assumed an ideal input voltage source. The model parameters are the same as listed in the simulation parameters in Table 1. Given that an assumption was made that the average voltages of the flying capacitors have ideal behavior, and since the capacitor ESR values

and the switch on-resistances were not considered in the model, branch voltage differences of around 0.47 V in magnitude are present during switching. In practice, the presence of such nonidealities mean that the 0.47 V branch voltage difference would be absorbed by the resistances and the branch voltages would balance out during switching.

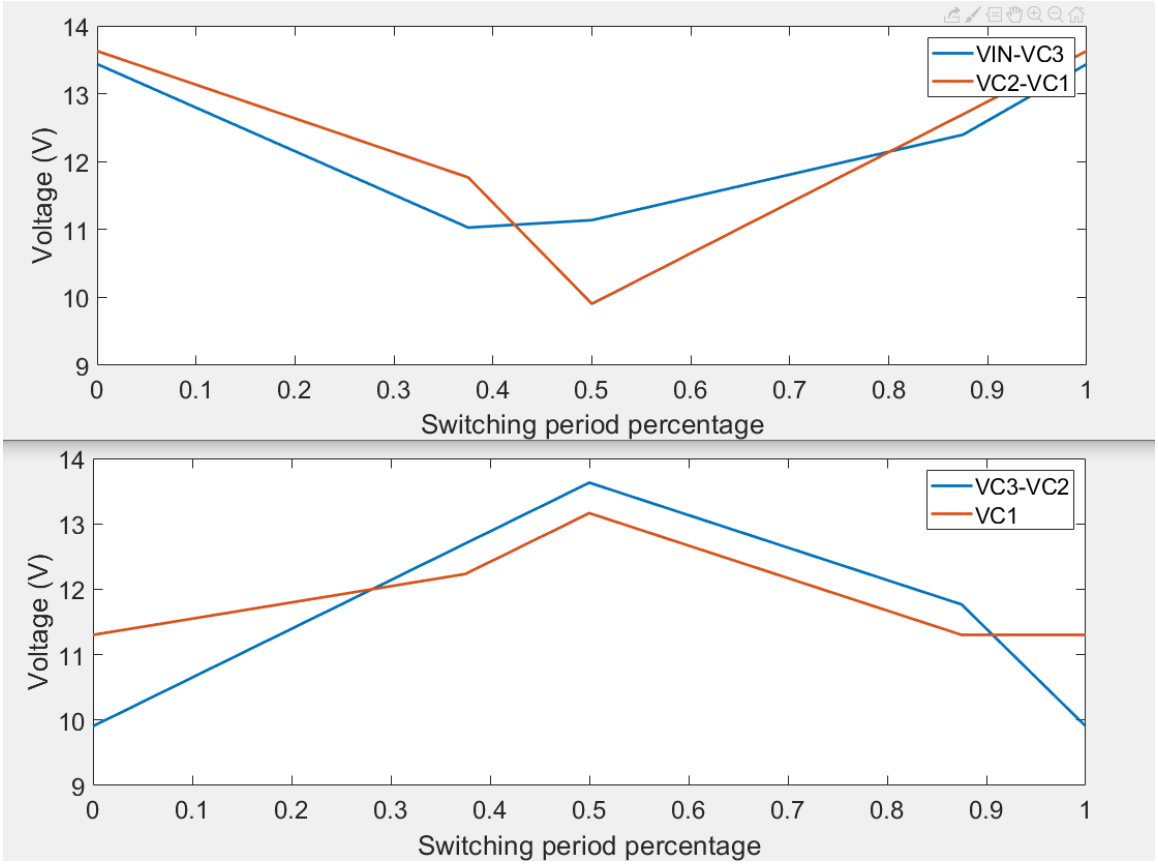

Figure 44: Modelled Phase 1 and Phase 2 equivalent branch voltage waveforms with effect of input voltage ripple considered; D5 = D8 = 0.375

Figure 44 shows the modelled equivalent circuit branch voltage differences with the addition of input voltage ripple generated by a 100 µF input capacitor. The voltage difference between the Phase 1 equivalent circuit branches at t = 0 was around 0.2 V, while the voltage difference between the Phase 2 equivalent circuit branches at t = 0.5T was around 0.5 V. The objective of the model analysis was to observe whether changing the duty cycles of switches Q5 and Q8 (the 'split-phase' switches) would have any effect on

the equivalent circuit branch voltage differences caused by input voltage ripple during switching. If, in adjusting the duty cycles of Q5 and/or Q8, the voltage differences during switching between the equivalent circuit branches can be reduced, then it can be concluded that the method of tuning the duty cycles of the ‘split-phase’ switches will be effective at compensating for the voltage differences during switching because of input voltage ripple.

When the duty cycles of both switch Q5 and Q8 were changed from 37.5% to 40%, the voltage difference between the Phase 1 equivalent circuit branches at t = 0 was reduced to 0.06 V (from 0.19 V), while the voltage difference between the Phase 2 equivalent circuit branches at t = 0.5T was reduced to 0.37 V (from 0.5 V). As shown in Figure 45, the waveforms obtained from the flying capacitor model appear closer together during switching.

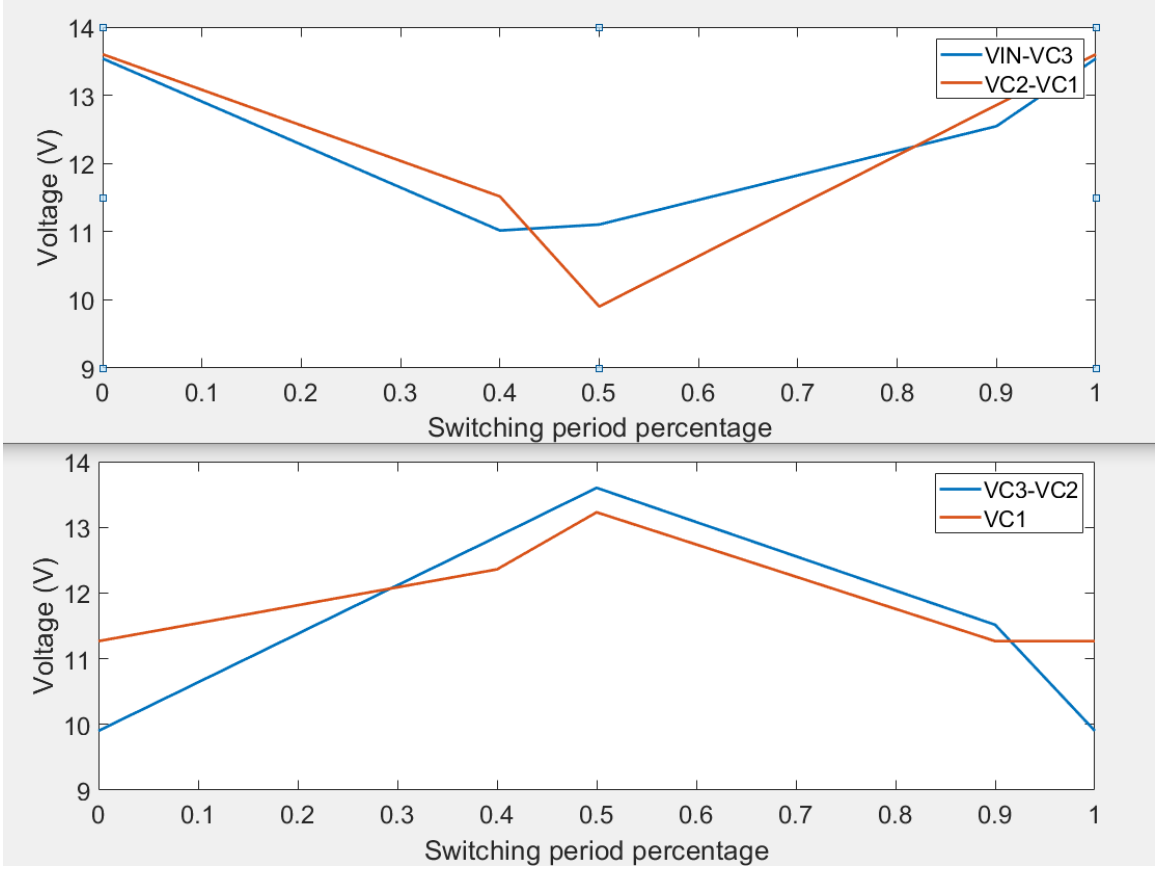

Figure 45: Modelled Phase 1 and Phase 2 equivalent circuit branch voltage waveforms with effect of input voltage ripple considered; D5 = D8 = 0.4

The above results from flying capacitor modelling shows that slightly adjusting the values of the 'split-phase' duty cycles would be able to compensate for equivalent circuit branch voltage differences caused by external sources of voltage ripple. However, as previously mentioned, the flying capacitor voltage models were derived with multiple assumptions of ideal behavior. The derivations assumed piecewise-constant current waveforms and did not consider the interactions that occur between capacitors when capacitive branches with difference voltages are connected. Therefore, the model could only be used to obtain a general understanding on whether changing the 'split-phase' duty cycle values would have any effect of reducing branch voltage differences due to external sources of voltage ripple. To accurately analyze the effects of modifying the 'split-phase'

duty cycle values on branch voltage differences during switching, computer simulations of the circuit were necessary.

5.4.2 Simulation Analysis of Duty Cycle Tuning Strategy

Simulations by PSIM of the split-phase Dickson SCC were performed to determine the effects of tuning 'split-phase' duty cycle values on the magnitudes of the equivalent circuit branch voltages due to input voltage ripple during switching. The simulations were performed using the nominal parameters listed in Table 11.

Table 11: Simulation Parameters used for Duty Cycle Tuning Analysis

SIMULATION PARAMETERS	
V_{IN}	48 V
V_{OUT}	12 V
I_{OUT}	35 A
C3, C2, C1	47 µF
C_{OUT}	47 µF
C_{IN}	100 µF
D_5	0.375
D_8	0.375
$D_{(All\ other\ switches)}$	0.5
L_{OUT}	200 nH
f_{SW}	100 kHz
$R_{DS(on)}$	1 mΩ
R_{ESR}	1 mΩ
$R_{L(winding)}$	0.3 mΩ

Without any form of compensation, with the 'split-phase' duty cycles of both switches Q8 and Q5 set to a value of 37.5%, the voltage difference between the Phase 2 equivalent circuit branches during the transition from Phase 1b to Phase 2 was 0.142 V, while the voltage difference between the Phase 1 equivalent circuit branches during the transition from Phase 2b to Phase 1 was 0.185 V. The maximum current through the flying capacitors occurred in flying capacitor C3, with a current transient measuring 43.95 A. A detailed view of the equivalent circuit branch voltage waveforms during switching, as well as the flying capacitor current waveforms, are presented in Figure 46.

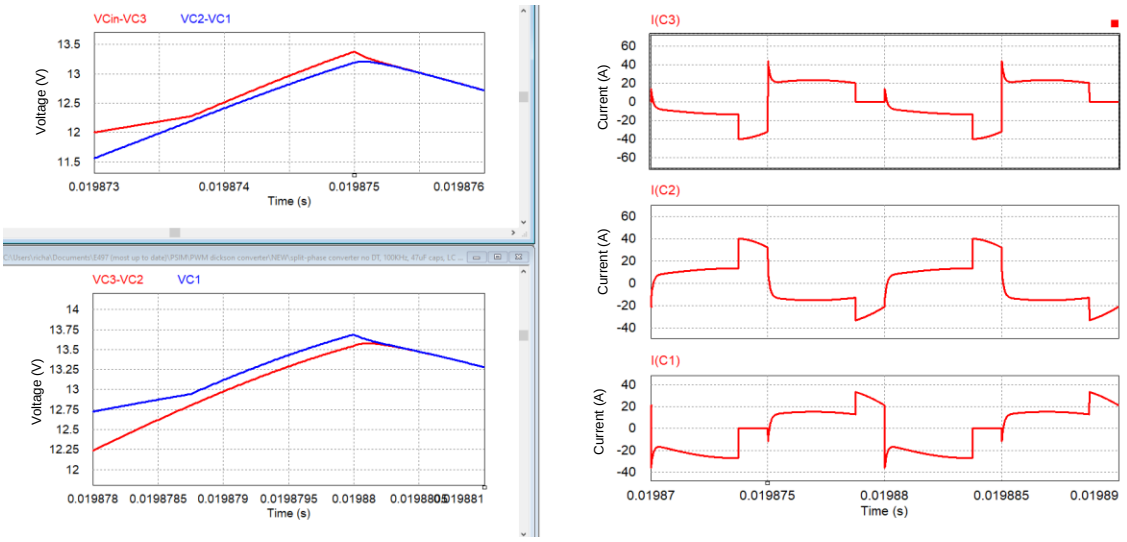

Figure 46: Simulated Phase 1 and Phase 2 equivalent circuit branch voltage waveforms at their times of switching (left) and flying capacitor currents over two switching cycles (right); D5 = D8 = 0.375; 100 µF input capacitor

For this investigation, the duty cycles of the 'split-phase' switches, Q8 and Q5, were first adjusted independently of each other to analyze the effects of changing the duty cycle of an individual 'split-phase' switch. When the duty cycle of switch Q5 was slightly raised from 37.5% to 38%, the voltage difference between the Phase 2 equivalent circuit branches during the transition from Phase 1b to Phase 2 was reduced to 0.10 V, from the previous value of 0.14 V. Similarly, the voltage difference between the Phase 1 circuit branches during the transition from Phase 2b to Phase 1 was reduced to 0.14 V, from the previous value of 0.185 V. Correspondingly, the maximum current through the flying capacitors dropped to 38.87 A, from the previous value of 43.95 A. Detailed views of the equivalent circuit branch voltages during switching, as well as the flying capacitor current waveforms for this operating scenario, are presented in Figure 47.

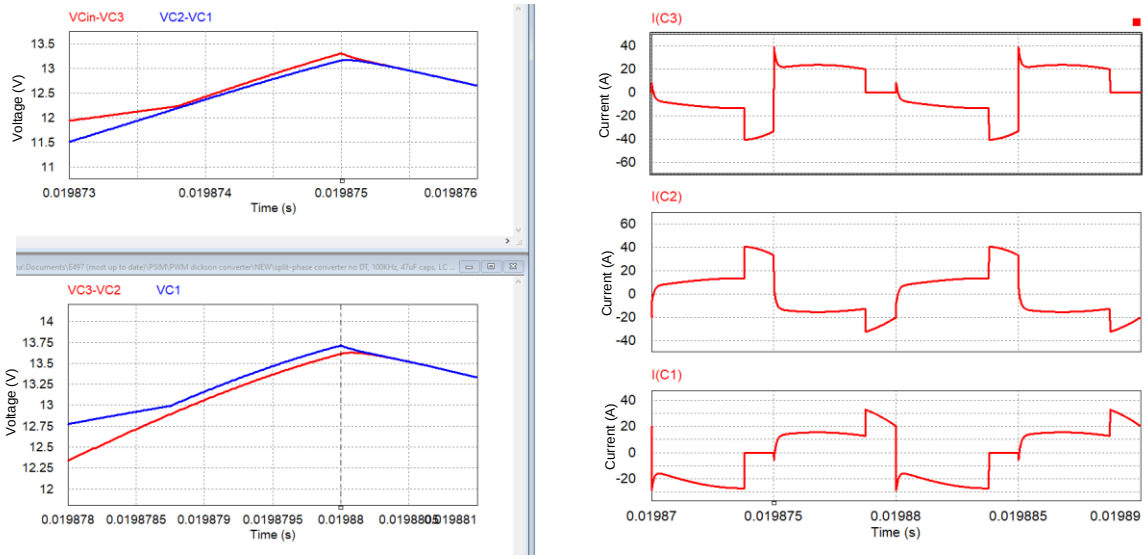

Figure 47: Simulated Phase 1 and Phase 2 equivalent circuit branch voltage waveforms at their times of switching (left) and flying capacitor currents over two switching cycles (right); D5 = 0.38; D8 = 0.375; 100 µF input capacitor

The above simulation results prove that tuning the duty cycle of only one of the 'split-phase' switches was sufficient at reducing the voltage differences between equivalent circuit branches due to input voltage ripple during switching. The duty cycle of switch Q5 was then progressively raised to observe the trend between the duty cycle of Q5 and the voltage differences between the equivalent circuit branches during switching. The plot shown in Figure 48 shows that the magnitudes of the voltage differences during both switching transitions exhibits linear trends as the duty cycle of Q5 increases. Both voltage difference trends cross the horizontal axis when the duty cycle of Q5 was between 0.39 and 0.4. Note that a positive voltage differences between the Phase 1 equivalent circuit branches indicate that the voltage of branch $V_{IN} - V_{C3}$ is larger in magnitude than the voltage of branch $V_{C2} - V_{C1}$ when switching takes place, and that the negative voltage differences between the Phase 2 equivalent circuit branches indicate that the voltage of branch $V_{C3} - V_{C2}$ is smaller than the voltage of branch V_{C1} when switching takes place.

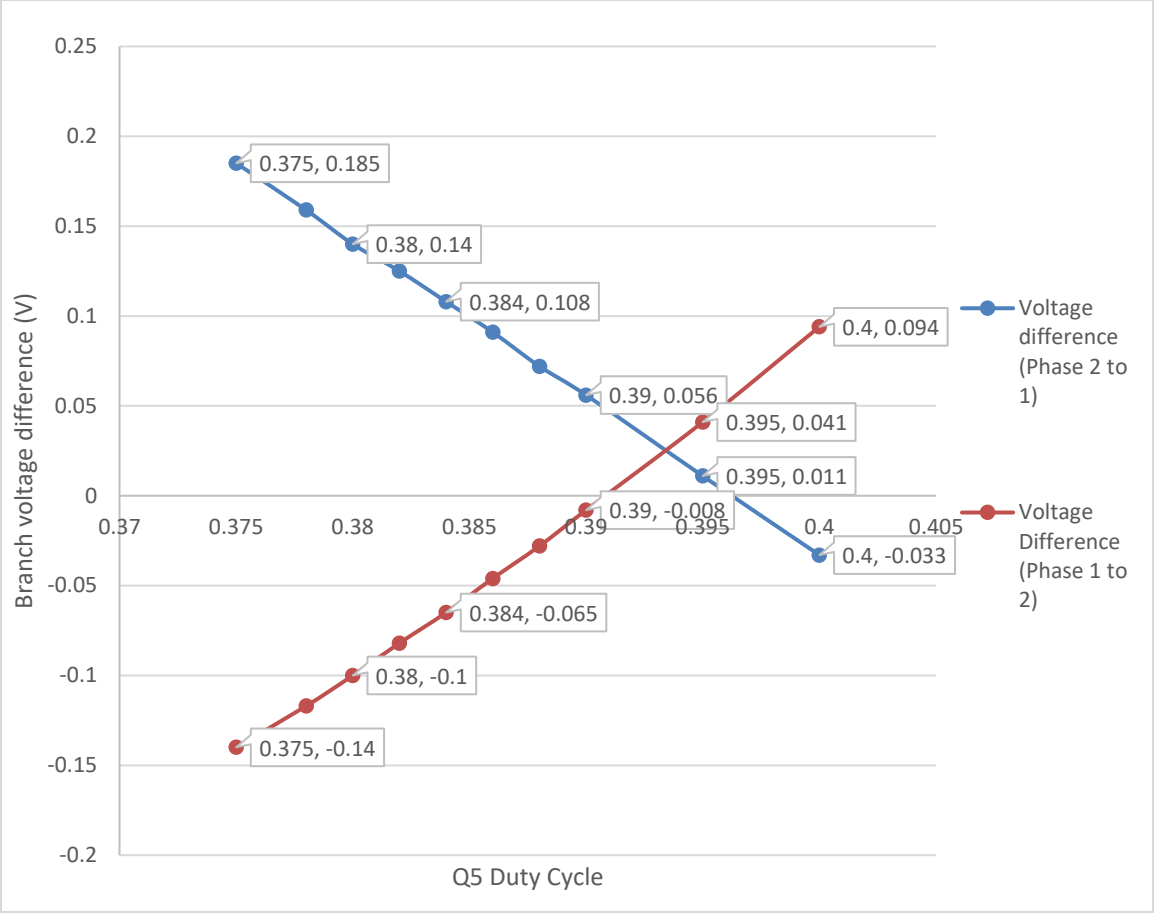

Figure 48: Plot of Phase 1 (V1) and Phase 2 (V2) branch voltage differences versus Q5 duty cycle

When the duty cycle of Q5 was increased to 39%, the voltage differences during switching were reduced to the point where their effect on the flying capacitor currents during switching are insignificant. These simulation results are displayed in Figure 49.

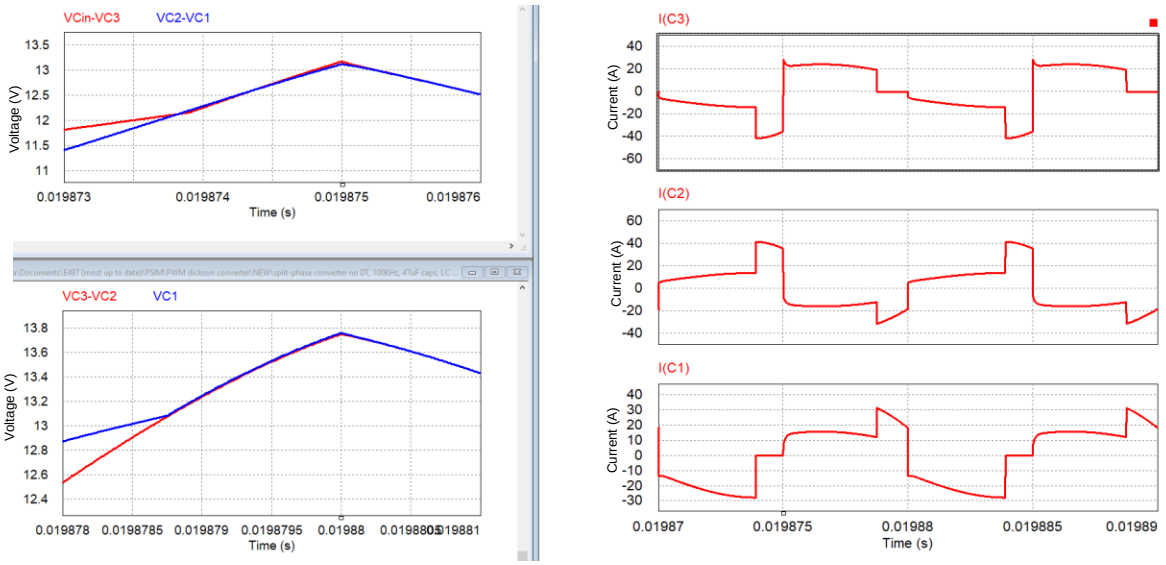

Figure 49: Simulated Phase 1 and Phase 2 equivalent circuit branch voltage waveforms at their times of switching (left) and flying capacitor currents over two switching cycles (right); D5 = 0.39; D8 = 0.375; 100 µF input capacitor

Further simulations were performed on the circuit to analyze whether changing the duty cycle of Q5 would effectively compensate for voltage differences during switching caused through usage of input capacitors with values smaller than 100 µF. The values of the flying capacitors were fixed at 47 µF throughout these simulations. As shown in the plot in Figure 50, tuning the duty cycle of Q5 could successfully compensate for voltage differences during switching in scenarios with an input capacitor as small as 40 µF, although it should be noted that in scenarios with smaller input capacitors, larger increases in the duty cycle of Q5 were necessary.

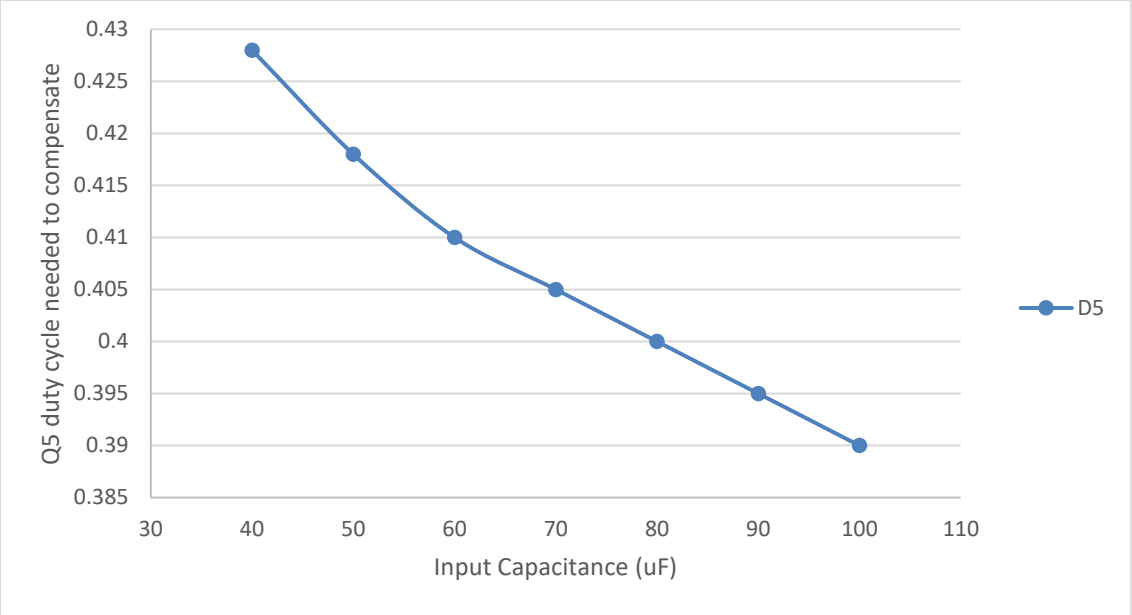

Figure 50: Required Q5 duty cycle to compensate for effect of input voltage ripple, versus value of input capacitor

Simulations were also performed using different values of flying capacitors to evaluate whether different values of duty cycle for Q5 would be needed to compensate for input voltage ripple in these configurations. A 100 µF input capacitor was used throughout these simulations. As shown in the plot in Figure 51, the required duty cycle of Q5 required to compensate for the input voltage ripple increases as the values of the flying capacitors increased. This result was expected because larger flying capacitors experience less voltage ripple, and therefore would need slightly longer charging times to be able to make up for the voltage differences caused by input voltage ripple during switching, given a constant input capacitor value, and thus a constant peak-to-peak input voltage ripple, over a range of flying capacitor values.

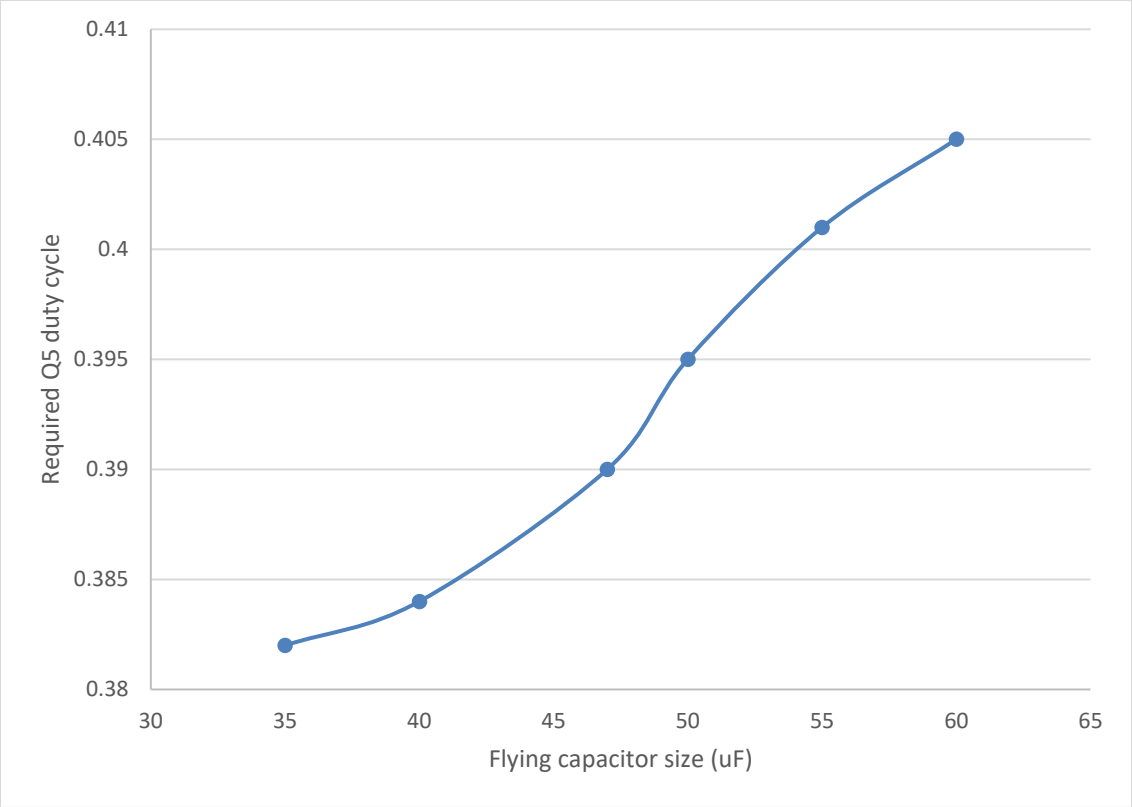

Figure 51: Required Q5 duty cycle to compensate for effect of input voltage ripple, versus flying capacitor value

However, as the values of the flying capacitors increases, the decreased voltage ripple of the flying capacitors results in the duty cycle tuning strategy becoming less effective at compensating for input voltage ripple. The simulation results shown in Figure 52 were obtained using 60 µF flying capacitors and a duty cycle of 0.405 on switch Q5. The compensation resulted in a maximum voltage difference of 0.11 V during switching. Other duty cycle values that were tested for this scenario were less effective because they tend to greatly reduce the voltage difference during the transition to Phase 1, but greatly increase the voltage difference during the transition to Phase 2, or vice versa.

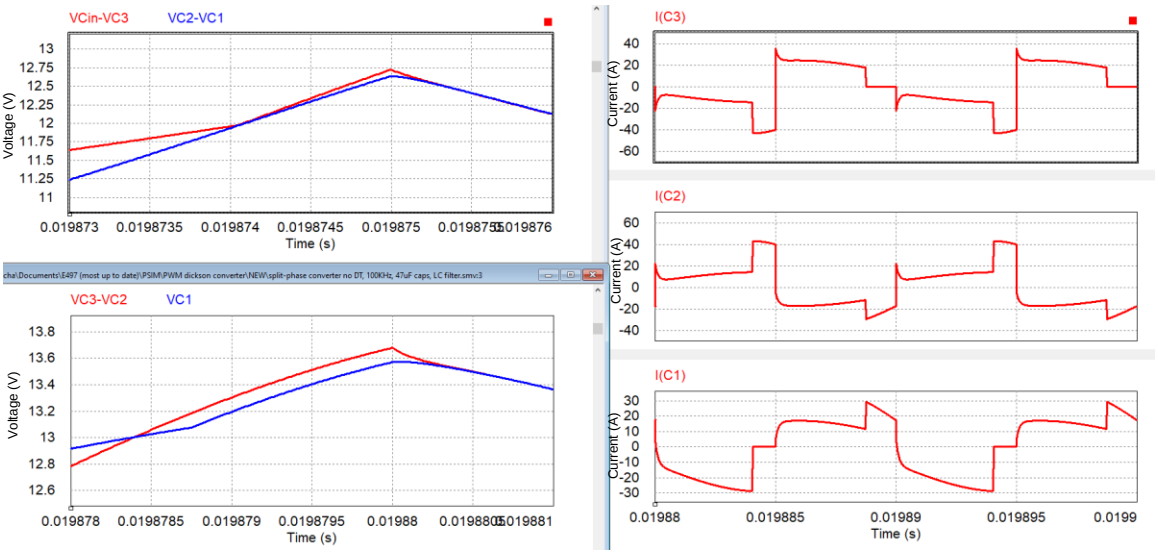

Figure 52: Simulated Phase 1 and Phase 2 equivalent circuit branch voltage waveforms at their times of switching (left) and flying capacitor currents over two switching cycles (right); D5 = 0.405; D8 = 0.375; 100 µF input capacitor; 60 µF flying capacitors

Finally, simulations to simulate a 'power-up' scenario were performed, again using the 100 µF input capacitor and with the duty cycle of Q5 set to 39%. The split-phase Dickson SCC was first simulated with a load of 5 A (to represent a low-power setting), then with a load of 15 A (to represent a medium power setting with respect to the full load of 35 A), to investigate whether the tuned duty cycle of switch Q5 would be effective at compensating for voltage differences due to input voltage ripple in a wide range of loading scenarios. For the 5 A load scenario, a small amount of voltage difference during switching was observed, however the current spikes resulting from these voltage differences were mostly insignificant compared to the maximum non-transient currents through the flying capacitors. The simulation results for the 5 A load scenario are presented in Figure 53.

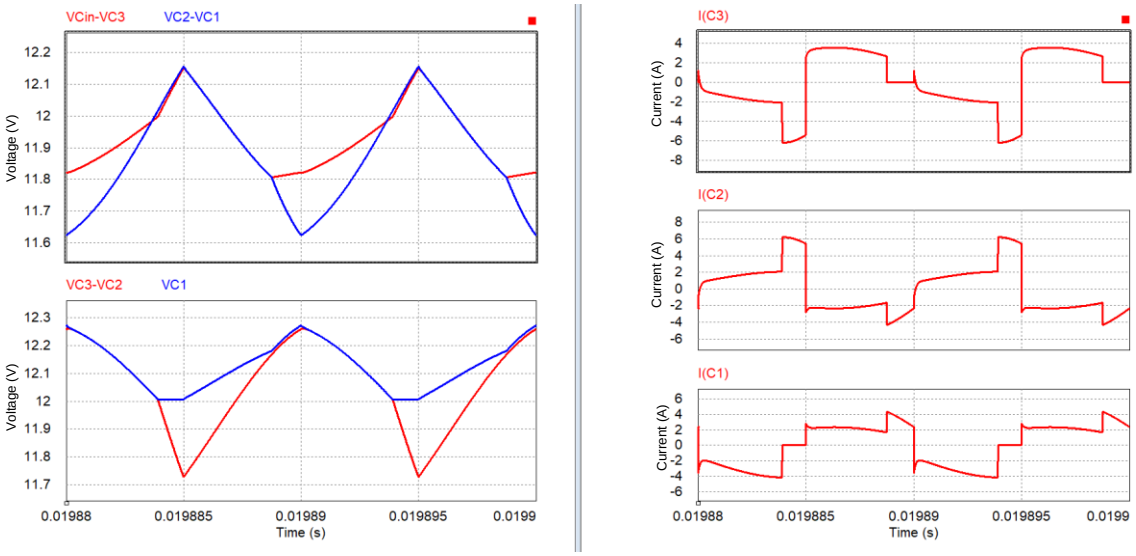

Figure 53: Simulated Phase 1 and Phase 2 equivalent circuit branch voltage waveforms (left) and flying capacitor currents (right); D5 = 0.39; D8 = 0.375; 100 µF input capacitor; 5A output current

When the circuit was simulated with a 15 A load, the equivalent circuit branch voltage waveforms behaved similarly to the full load waveforms shown in Figure 49, in that the voltage differences during switching were reduced to the point where they became insignificant. The simulation results for the 15 A load scenario are presented in Figure 54.

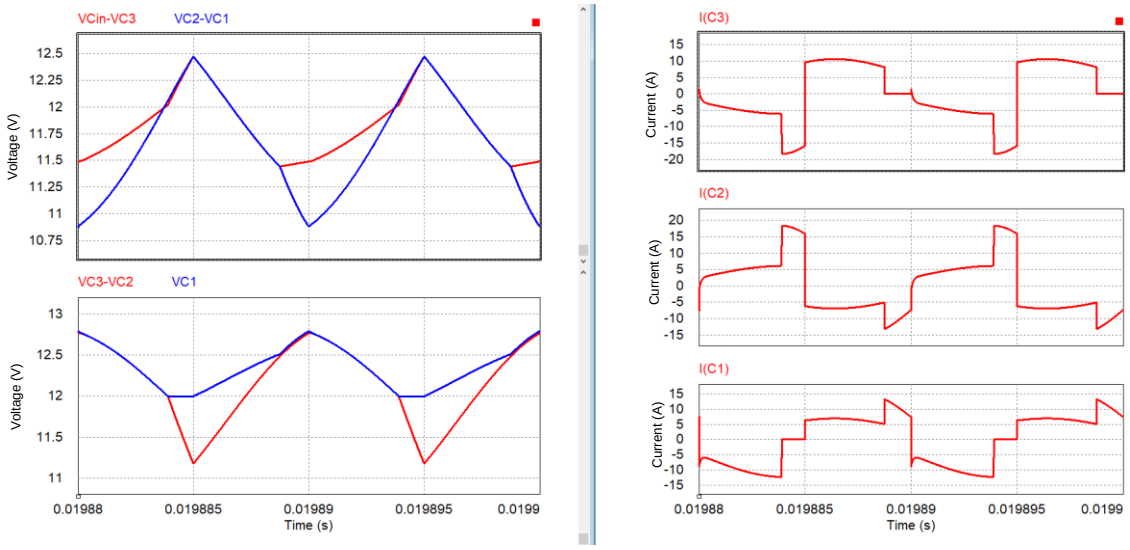

Figure 54: Simulated Phase 1 and Phase 2 equivalent circuit branch voltage waveforms (left) and flying capacitor currents (right); D5 = 0.39; D8 = 0.375; 100 µF input capacitor; 15A output current

It should be noted that the above simulations were performed with an output capacitor which ensures that the output voltage ripple is less than 5% of the output voltage. When the output voltage experiences little ripple, the magnitudes of the voltage difference during the Phase 1 and Phase 2 switching transitions caused by input voltage ripple are roughly equal. Through additional simulations, it was found that larger amounts of output voltage ripple (>5% of the output voltage) indirectly resulted in the voltage differences caused by input voltage ripple only appearing during one switching transition per switching cycle. This was because larger output voltage ripple values caused the average voltages of the flying capacitors to decrease, thereby indirectly causing the branch voltages during one of the switching transitions to equalize. Figure 55 shows the simulated equivalent circuit branch voltage waveforms obtained from simulation of the 4-to-1 split-phase Dickson SCC using the nominal parameters shown in Table 11, with untuned duty cycles, but with a 23.5 µF output capacitor (thus ensuring a large output voltage ripple).

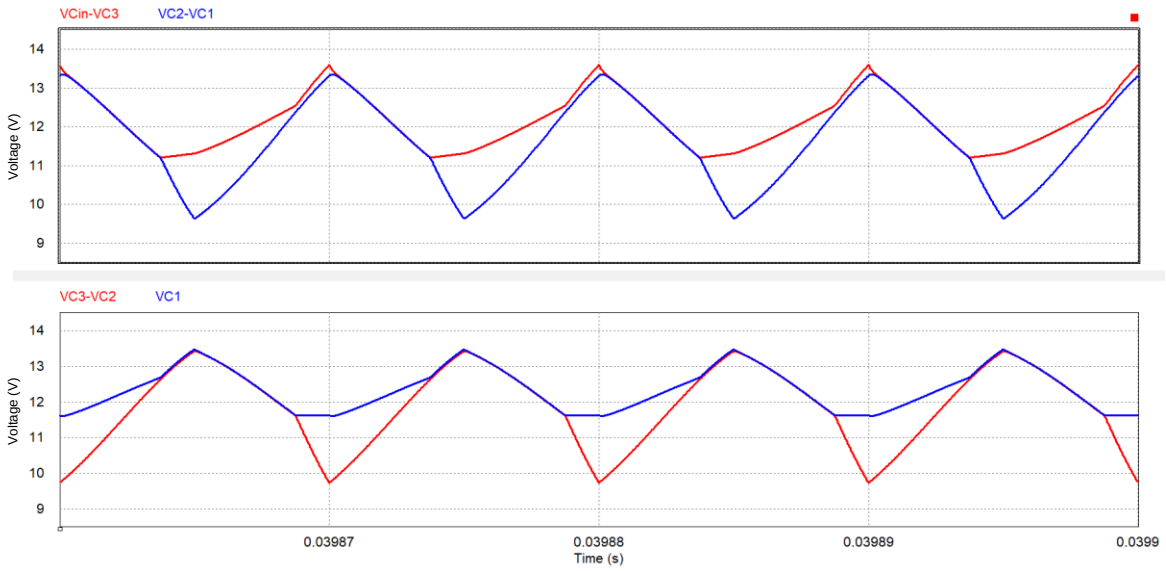

Figure 55: Simulated Phase 1 and Phase 2 equivalent circuit branch voltage waveforms of 48 V to 12 V, 35 A split-phase Dickson SCC; Cout= 23.5 µF

As shown in Figure 55, the voltage differences due to input voltage ripple only appears during the transition from Phase 2 to Phase 1, due to the indirect effect of the increased output voltage ripple. Due to the one-sided nature of the voltage differences during switching in this scenario, the duty cycle tuning strategy would not be effective at compensating for the effects of input voltage ripple. Changing the duty cycle of Q5 in this scenario would cause voltage differences during Phase 1 transition to decrease but would cause voltage differences during Phase 2 transition to increase. Therefore, it can also be concluded that input voltage ripple compensation through duty cycle tuning would require the output voltage ripple to exhibit low ripple to be effective.

The above investigations prove that for a given size of input capacitor, tuning the duty cycle of just one of the ‘split-phase’ switches would be sufficient to compensate for the voltage differences during switching due to the input voltage ripple resulting from the use of that size of input capacitor. Furthermore, the tuned value of the ‘split-phase’ switch does not need to be changed to adapt to different load levels. This method of tuning the ‘split-

phase' switches to compensate for voltage differences during switching due to the effects of input voltage ripple would allow the use of smaller input capacitors, while at the same time dispensing with the requirement for sensing circuitry. It is also simple to implement in practice, as it would only require adjusting the pulse width of the microcontroller output that controls the 'split-phase' switch. However, the values of duty cycle required to compensate for input voltage ripple are dependent on the values of the flying capacitors used in the split-phase Dickson SCC, with larger flying capacitors requiring a larger duty cycle on the 'split-phase' switch to compensate for the input voltage ripple. Furthermore, high output voltage ripple may result in the duty cycle tuning method becoming ineffective at compensating for input voltage ripple, since output voltage ripple indirectly causes the voltage differences during switching caused by input voltage ripple to appear during only one switching transition per switching cycle. It should also be noted that parasitic properties of passive and active components, such as MOSFET on-resistance and capacitor ESR, may, in practice, require the use of duty cycle values different to the values obtained through simulation.

5.5 Simulation Testing of 10-switch Split-Phase Dickson SCC

As previously discussed, due to the onset of the COVID-19 pandemic, it was not possible to perform prototype testing on the 10-switch 48 V to 12 V, 35 A split-phase Dickson SCC prototype. Therefore, it was decided that the performance of this configuration would be analyzed through circuit simulation.

The 10-switch configuration of the 48 V to 12 V, 35 A split-phase Dickson SCC was simulated using 47 µF flying capacitors and a 100 µF input capacitor. As with previous simulations and prototype testing, the switching frequency was set to 100 kHz.

Assumptions made during these simulations include: (1) that the flying capacitor values are perfectly matched at 47 µF, (2) that the equivalent series resistance (ESR) of all capacitors in the circuit are 1 mΩ, and (3) that the switches in the circuit have on-resistances of 1 mΩ and diode forward voltages of 0.7 V. The full list of simulation parameters is shown in Table 12.

Table 12: Simulation Parameters for 10-switch 4-to-1 Dickson SCC Analysis

SIMULATION PARAMETERS	
V_{IN}	48 V
V_{OUT}	12 V
I_{OUT}	35 A
C3, C2, C1	47 µF
C_{OUT}	47 µF
C_{IN}	100 µF
D_5	0.39
D_8	0.375
$D_{(All\ other\ switches)}$	0.5
L_{OUT}	200 nH
L_{IN}	10 µH
f_{SW}	100 kHz
$R_{DS(on)}$	1 mΩ
R_{ESR} (All capacitors)	1 mΩ
$R_{L(winding)}$	0.3 mΩ
$V_{Fwd\ Diode}$	0.7 V

5.5.1 Single Circuit Phase Configuration Simulation Results

The compensatory method of tuning the 'split-phase' switches, as described in Section 5.4, was implemented in the 10-switch circuit for the single-stage analysis. A duty cycle of 0.39 was imposed on switch Q5 to compensate for the input voltage ripple caused by the operation of the 100 µF input capacitor.

The equivalent circuit branch voltage waveforms of the 10-switch 48 V to 12 V, 35 A split-phase Dickson SCC circuit, obtained from circuit simulation, are shown in Figure 56. The implementation of the compensatory method meant that the maximum voltage

difference recorded between the equivalent circuit branches during switching being 0.054 V.

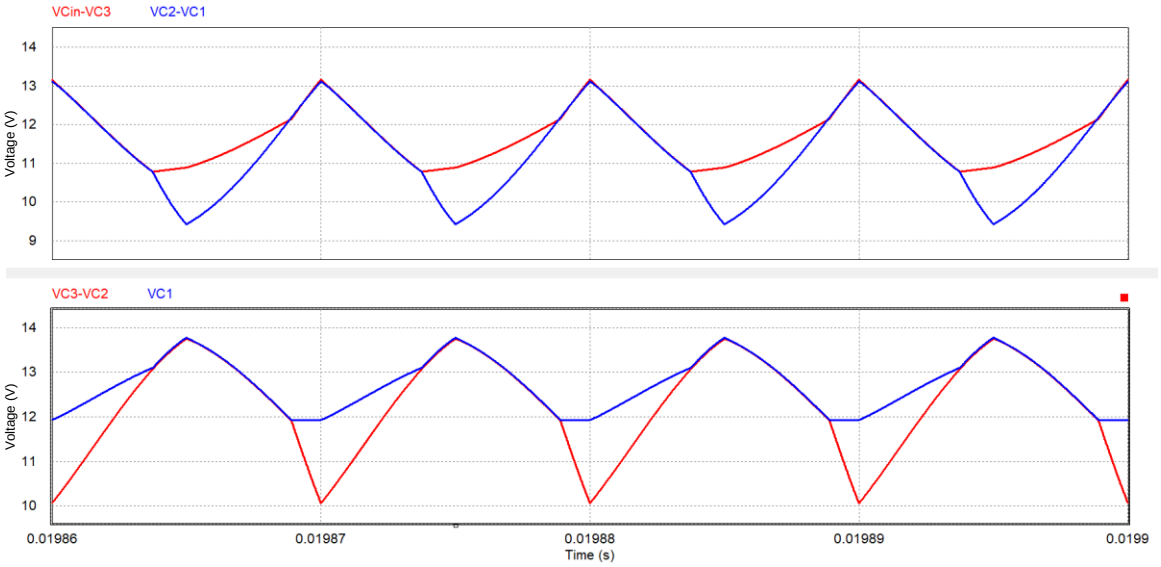

Figure 56: Equivalent Circuit Branch Voltage waveforms of simulated single circuit phase 10-switch 48 V to 12 V, 35 A split-phase Dickson SCC (with duty cycle compensation)

Figure 57 shows the current waveforms of the 10-switch split-phase Dickson SCC's flying capacitors, obtained from simulations. Due to the implementation of the compensatory method, the flying capacitors experience transient behaviors of very small magnitudes.

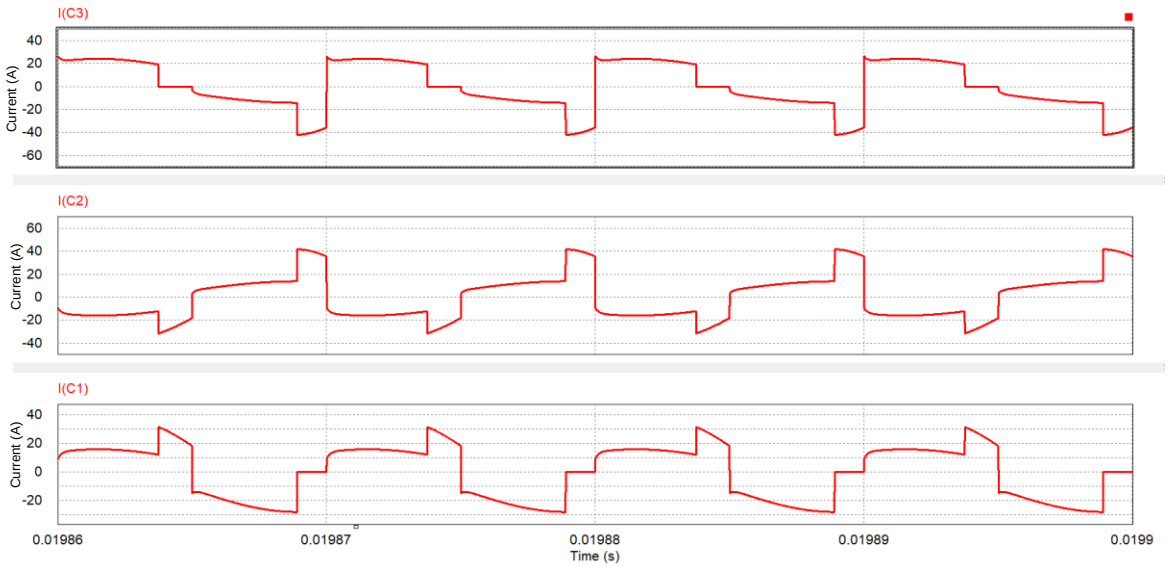

Figure 57: Simulated flying capacitor current waveforms of single circuit phase 10-switch 48 V to 12 V, 35 A split-phase Dickson SCC

The ability to use smaller input capacitors in combination with duty cycle tuning to eliminate the effects of the resultant input voltage ripple within the split-phase Dickson SCC, will lead to increased efficiency of the circuit in practice.

The input capacitor and the output load voltage waveforms are shown in Figure 58, while the input current and output current waveforms are shown in Figure 59.

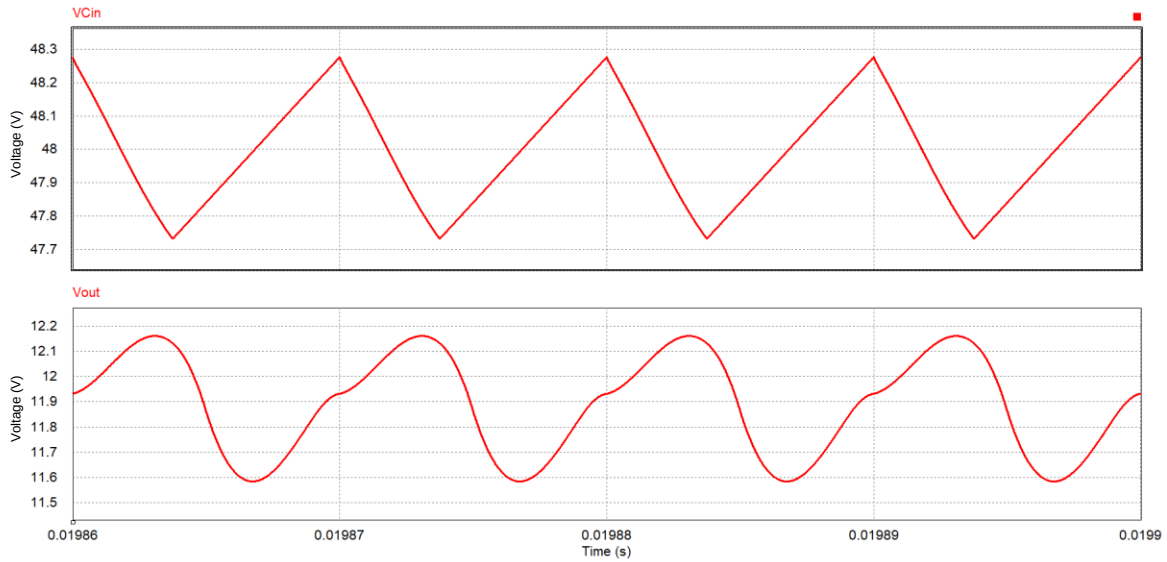

Figure 58: Simulated input and output voltage waveforms of single circuit phase 10-switch 48 V to 12 V, 35 A split-phase Dickson SCC

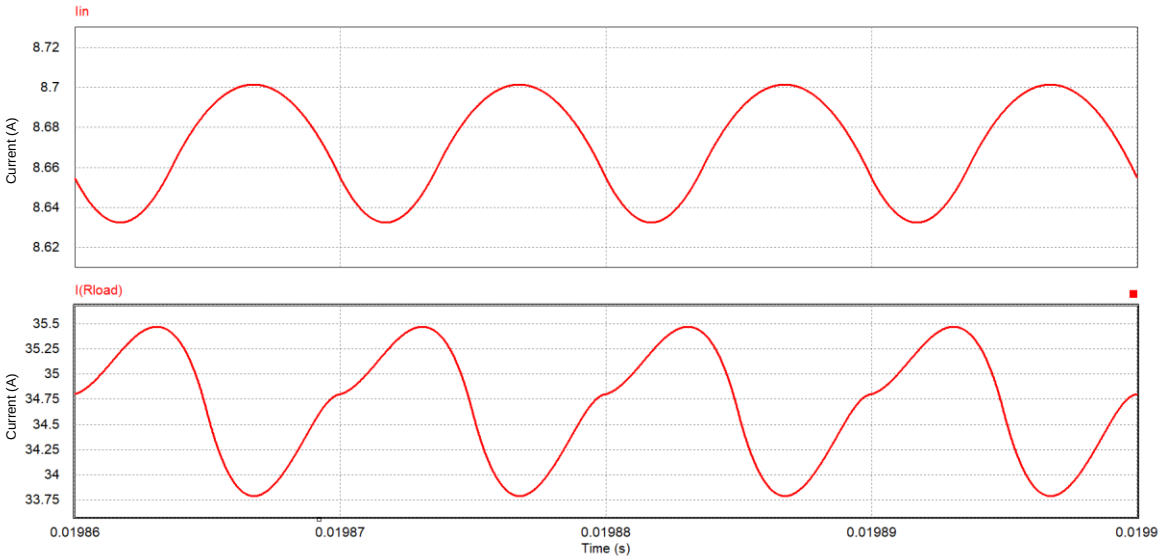

Figure 59: Simulated input and output current waveforms of single circuit phase 10-switch 48 V to 12 V, 35 A split-phase Dickson SCC

Using the waveforms in Figures 58 and 59, the peak-to-peak input voltage ripple was 0.543 V, and the peak-to-peak output voltage ripple was 0.577 V. The peak-to-peak input current ripple was 0.069 A, while the peak-to-peak output current ripple was 1.681 A.

5.5.2 Simulation Results of Two-Phase Interleaved Configuration

As discussed in Chapter 4, the 10-switch prototype was designed with interleaving in mind. As such, simulations were performed on a two-phase interleaved configuration of the 10-switch 48 V to 12 V split-phase Dickson SCC converter. The interleaved configuration places two power stages in parallel. The two stages share an input source and an output load, consequently supplying a combined output current of 70 A to the load if each individual stage supplies 35 A. The switching cycles of the two power stages are exactly half of a switching period (or 180 degrees) apart. This results in decreases in the input and output voltage and current ripples; the interleaving of phases this way causes the ripple frequencies at the input and output to essentially double.

Note that in this context, the term 'phase' refers to a single power circuit of an interleaved configuration, instead of a circuit state within a switching cycle. 'Two-phase' interleaved therefore refers to two power stage circuits connected in parallel with each other. The circuits operate with split-phase control.

The circuit schematic of the two-phase interleaved, 10-switch 4-to-1 Dickson SCC topology is shown in Figure 60.

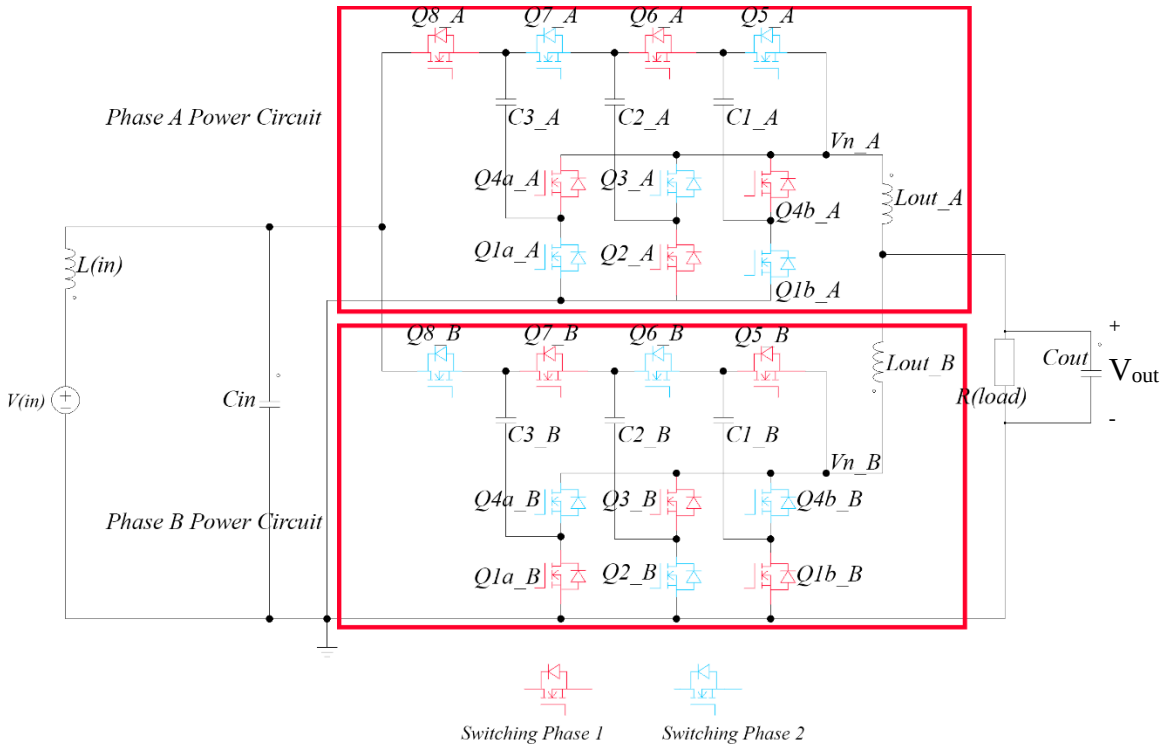

Figure 60: Circuit schematic of two-phase interleaved, 10-switch 4-to-1 split-phase Dickson SCC topology

To evaluate the current sharing capabilities between the two individual power stages, the simulations were performed with Phase A using 47 µF flying capacitors, and Phase B using 51 µF flying capacitors. Furthermore, to ensure a low output voltage ripple, the value of the output capacitor was doubled to 94 µF. The remaining simulation parameters are identical to those listed in Table 12.

The two-phase interleaved circuit was initially simulated without the compensatory measures introduced in Section 5.4, to observe the impact of input voltage ripple on the interleaved operation of the split-phase Dickson SCC.

The equivalent circuit branch voltage waveforms obtained from simulation of the two-phase interleaved, 10-switch split-phase Dickson SCC circuit are shown in Figure 61.

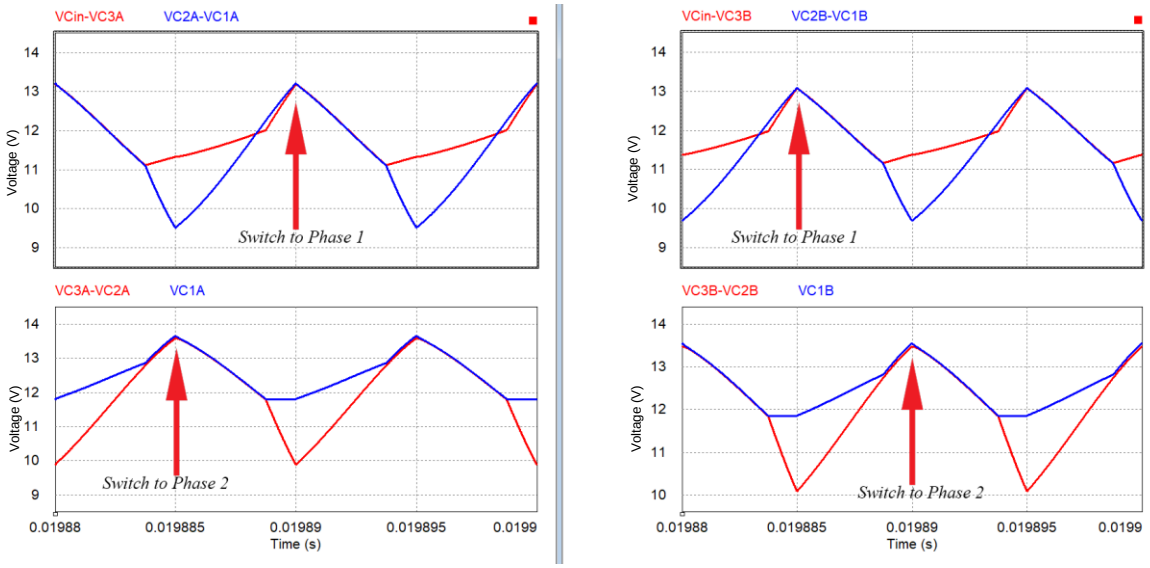

Figure 61: Equivalent Circuit Branch Voltage waveforms of simulated two-phase interleaved, 10-switch 48 V to 12 V, 70 A split-phase Dickson SCC

The waveforms in the figure above show that the voltage differences are only present during the transition to Switching Phase 1 for both stages of the two-stage split-phase Dickson SCC. The maximum voltage difference recorded during switching was 0.07 V. The small voltage differences during both switching transitions resulted in the flying capacitors exhibiting current transients of insignificant magnitudes, as shown in the flying capacitor current waveforms in Figure 62.

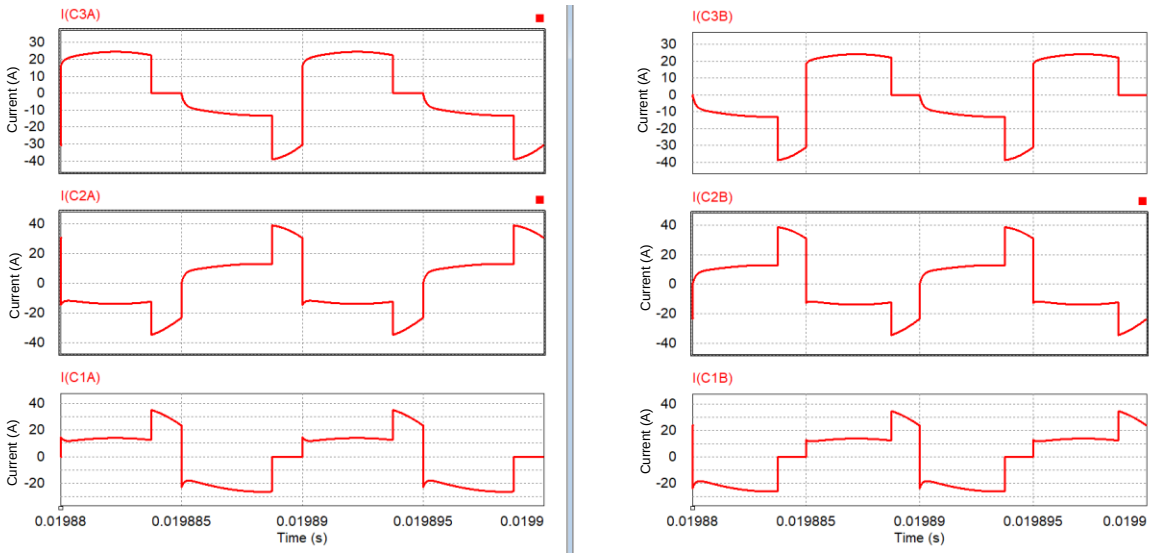

Figure 62: Simulated flying capacitor current waveforms of two-phase interleaved, 10-switch 48 V to 12 V, 70 A split-phase Dickson SCC

Compared to the simulation results from the uncompensated single-phase 48 V to 12 V split-phase Dickson SCC, shown in Figure 46, the uncompensated two-stage interleaved 48 V to 12 V split-phase Dickson SCC configuration experiences far less voltage differences during transition due to input voltage ripple, and correspondingly, the flying capacitors only experience current transients of insignificant magnitudes. This is because the interleaving of two power circuits, each operating exactly half a switching period apart from each other, effectively doubles the frequency of the ripple experienced by components at the both the input and the output. In particular, the input voltage ripple was reduced by more than half to 0.22 V peak-to-peak, compared with 0.54 V peak-to-peak as obtained from the single stage 48 V to 12 V, 35 A simulations performed previously. Due to the heavily reduced input voltage ripple, the voltage differences generated during switching within the two-phase interleaved, 48 V to 12 V, 70 A split-phase Dickson SCC are small enough that compensation is of reduced necessity.

5.5.2.1 Other waveforms and performance discussion

The input and output current waveforms are shown in Figure 63, while the input and output voltage ripple waveforms are shown in Figure 64.

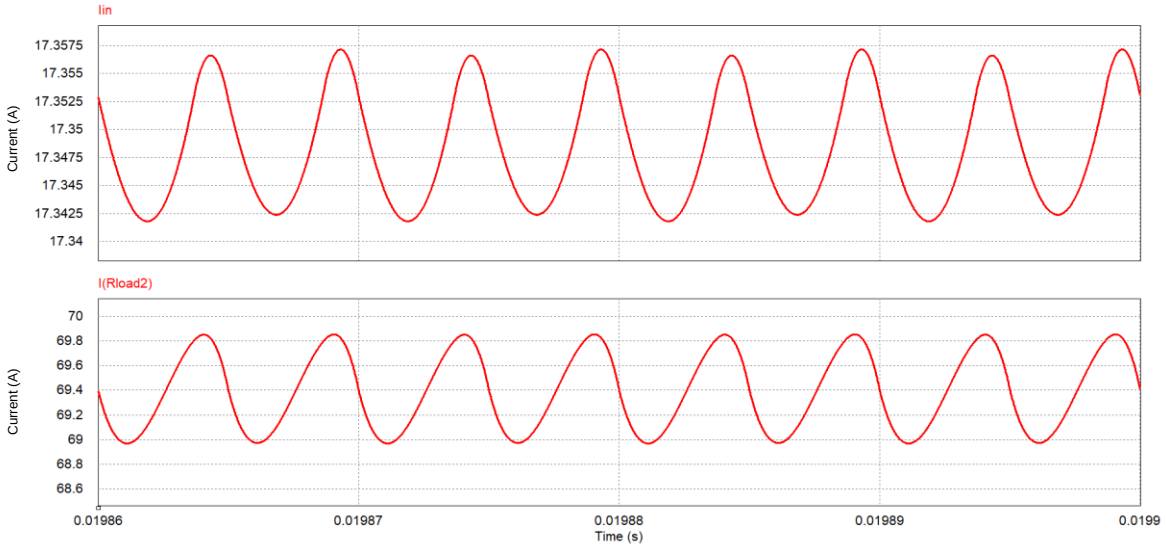

Figure 63: Simulated input and output current waveforms of two-phase interleaved 10-switch 48 V to 12 V, 70 A split-phase Dickson SCC

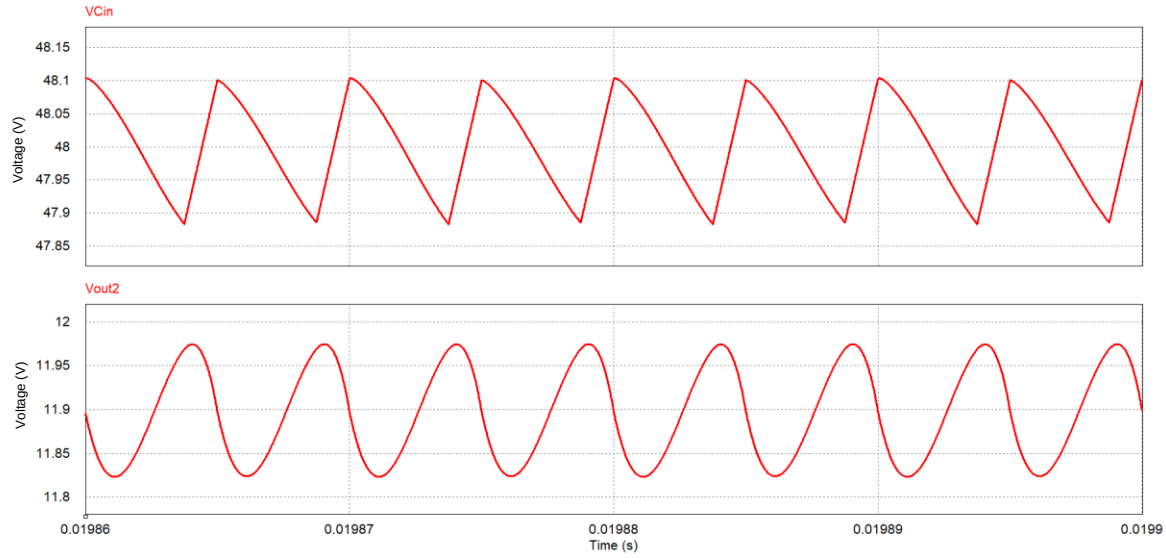

Figure 64: Simulated input and output voltage waveforms of two-phase interleaved 10-switch 48 V to 12 V, 35 A split-phase Dickson SCC

Using the waveforms in Figures 62 and 63, the peak-to-peak input voltage ripple was 0.22 V, and the peak-to-peak output voltage ripple was 0.15 V. The peak-to-peak input current ripple was 0.02 A, while the peak-to-peak output current ripple was 0.88 A. Comparing the voltage and current ripples obtained from the interleaved circuit simulations, to those obtained from the single-stage simulations performed in the previous section, these results confirm that configuring two stages of the split-phase Dickson SCC in an interleaved configuration leads to overall decreased voltage and current ripple at the input and output.

5.5.2.2 Current Sharing Behavior of Interleaved Split-Phase Dickson SCC Configuration

In the current two-phase interleaved configuration with component and simulation parameters listed in Table 12, with Phase A operating with 47 µF flying capacitors and Phase B operating with 51 µF flying capacitors, Phase A supplied an average of 34.79 A of current to the load, while Phase B supplied an average of 34.61 A of current to the load. The current sharing is thus 50.1% for Phase A and 49.9% for Phase B, indicating almost perfect current sharing between the two interleaved power circuits.

When the equivalent resistances of the circuit branches are different between the interleaved power circuits, the current sharing is not expected to be equal. To evaluate the current sharing behavior between the two power circuits when one of them uses components with different parasitic values, the MOSFET on-resistance and ESR values of the components were increased by 10% in Phase B. This change resulted in Phase A (the power stage with unchanged parasitic values) supplying an average current of 36.18 A to the output, while Phase B (the power stage with increased parasitic values) supplying an average current of 33.19 A to the output. The current sharing is therefore 52.2% for Phase

A, and 47.8% for Phase B, confirming that the current sharing between two interleaved phases of the split-phase Dickson SCC is dependent on the values of the parasitic resistances of the components used in the individual power circuits, relative to each other.

5.6 Conclusion

This chapter provided a discussion regarding the practical test results of a 48 V t o12 V, 35 A split-phase Dickson SC converter prototype. Verification of the flying capacitor values using the in-circuit measurement method confirmed that component tolerance and inaccuracies in the ceramic capacitor datasheets are the main contributors to flying capacitor mismatch. The split-phase Dickson SCC was found to function reliably even with significantly mismatched flying capacitors. However, by tuning the flying capacitors according to their actual de-rating values obtained through measurement, such that their values are matched, the efficiency of the split-phase Dickson SCC saw an overall increase.

A method to compensate for the effects of input voltage ripple on the operation of the split-phase Dickson SCC was developed and tested through simulation. This method was developed to allow the use of smaller input capacitors, thus allowing improvements in power efficiency. By tuning the duty cycles of the ‘split-phase’ switches of the circuit based on the flying capacitor values and the expected voltage ripple, the voltages of the flying capacitors are controlled to the point that the additional voltage differences that appear during switching as a result of input voltage ripple are reduced. When this compensation method was simulated on the 10-switch, 48 V to 12 V, 35 A split-phase Dickson SCC, the full-load efficiency attained by the simulated circuit was far higher than the full-load efficiency attained by the previously tested prototype.

Finally, a two-phase 10-switch, 48 V to 12 V, 70 A split-phase Dickson SCC converter in interleaved configuration was simulated to analyze the operation of multi-stage converters. The simulation results show that, by essentially doubling the ripple frequency at the input and output of the circuit, the overall input and output voltage and current ripples are decreased. This results in a reduced need to compensate for the effects of input voltage ripple, since the magnitude of the input voltage ripple is reduced in interleaved configurations. The current sharing between power stages in an interleaved configuration were found to be dependent on the component parasitic properties of each power circuit, relative to one another, with matched parasitic properties resulting in better current sharing among the power circuits.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

With the ever-growing power demands of data centers and development of better performing power architectures, the focus on denser, more efficient power converters for bridging the gap between the new power architectures and existing infrastructure is increasing. Traditional PWM-based power converters, due to the high stress their components experience, tend to be bulky and lacking in performance. The switched-capacitor converter's advantages of low component stress, and therefore its ability to utilize overall smaller components, increase power density, and improve efficiency, makes it an ideal power converter topology to improve the performance and efficiency within data centers. With the addition of more complex control architectures such as split-phase control to eliminate the problem of charge redistribution, the efficiency, performance, and power density of the Dickson-type switched-capacitor converter could be further improved.

Since the split-phase Dickson SCC has never been implemented in high current applications, such as 12 V and 35 A output, the research presented in this thesis mainly focuses on the effects of practical limitations and factors that could negatively impact the performance of the split-phase Dickson SCC, as well as the design considerations stemming from the effects of these practical factors. Shortcomings in performance due to practical factors, while typically not a concern in low-power applications, could be significant when concerning high-power, high-current applications.

The first contribution presented in this thesis focuses on the sensitivity of the split-phase Dickson SCC to mismatch between the values of the circuit's flying capacitors. The

original theory behind split-phase control was derived with the assumption that all the flying capacitor values were matched. If the flying capacitor values in the split-phase Dickson SCC are mismatched, their different charging and discharging rates results in the split-phase control method not fully compensating for charge redistribution. Simulations performed on the circuit with mismatched capacitors showed that significant current transients would be present whenever switching took place, thereby causing increases in conduction and switching losses within the circuit. It is therefore crucial that the flying capacitors of the split-phase Dickson SCC be matched as closely as possible. Switched-capacitor converters are generally implemented using ceramic capacitors. These capacitors will lose capacitance when subjected to DC voltages, which, combined with typical component tolerances, makes matching the flying capacitors of the split-phase Dickson SCC difficult in practice. Prototype testing has shown that variations in capacitance due to manufacturing tolerance, as well as the possibility of inaccuracies in the supplied capacitor de-rating curves, may require the capacitors of the split-phase Dickson SCC to be tuned to improve their performance.

The second contribution presented in this thesis focuses on the effects of input voltage ripple on the performance of the split-phase Dickson SCC. Since the flying capacitors are not isolated from the input source, any input voltage ripple superimposes itself onto the flying capacitors' voltage waveforms. Circuit simulations have shown that input voltage ripple cascading into the flying capacitors causes differing voltages between the equivalent circuit branches, thereby resulting in the split-phase control method not fully compensating for charge redistribution. Input voltage ripple is primarily caused by the operation of the input capacitor, which charges and discharges continually to ensure the input source

supplies a purely DC current. Intuitive methods to compensate for input voltage ripple include large input capacitors or sensing circuitry, however these methods are typically space-intensive, and result in either efficiency reduction or added design complexity. A method of compensation for input voltage ripple is introduced in this thesis. Developed from the existing split-phase control framework, it was found that slightly tuning the duty cycles of the 'split-phase' switches was an effective means of compensating for the effects of input voltage ripple originating from specific sizes of input capacitor. Compared to the standard methods of utilizing large input capacitors or implementing sensing circuitry, the method proposed in this thesis will not compromise on power density or efficiency and is simple to implement. Utilizing computer simulation, the efficacy of the method of compensating for the effects of input voltage ripple was verified.

6.2 Future Work

The work presented in this thesis represent the first implementation of the split-phase Dickson switched-capacitor converter in a high-current (48 V to 12 V, 35 A output) application. Therefore, further research in the topic of high power switched-capacitor converters could focus on further optimizing the components and control methods of the SCC for high power applications.

Regarding the issue of flying capacitor matching in the split-phase Dickson switched-capacitor converter, the effectiveness of implementing switch control and duty cycle tuning, similar to those developed in this thesis to compensate for the effect of input voltage ripple, could be investigated as a means to compensate for the different charging and discharging rates caused by mismatched flying capacitors. Alternatively, research could shift towards the utilization of more precise types of capacitors, or those that experience

less de-rating due to DC bias voltage, for constructing the flying capacitors of the split-phase Dickson SCC. Utilizing more precise capacitors to construct the flying capacitors would reduce the chance of mismatch between the flying capacitors in operation.

With regards to the sensitivity of the split-phase Dickson SCC to input voltage ripple, future research could focus on further optimizing the duty cycle tuning strategy. Alternatively, research could shift towards the application of using different types of input filters, such as active filters, to reduce input voltage ripple and thus, improve the performance of the split-phase Dickson switched-capacitor converter.

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Appendix A: Switch Control Code for Prototype 1

```
/*
 * File:   main.c
 * Author: Richard Y. Sun
 *
 * Created on June 10, 2019, 12:37 PM
 */

#include <stdio.h>
#include <stdlib.h>

#include "xc.h"
#include <libpic30.h>

//Oscillator Values
#define M 65
#define N1 2
#define N2 2

#define PLL_FREQ 7370000
#define FOSC (PLL_FREQ*M)/(N1*N2)
#define FCY (FOSC/2)
#define ACLK 117920000
#define ACLK_KHz 117920

//Duty Cycles
#define D1 0.5
#define D2 0.375
#define DT_NS 75
#define DT_MT 70 //Deadtime in Counter Values
#define D1_MT 4716 //D = 0.5 in Counter Values
#define D2_MT (D1_MT * 0.75) //D = 0.375 in Counter Values

//Setup
#pragma config FNOSC = FRC

#pragma config POSCMD = XT
#pragma config FCKSM = CSECMD
#pragma config OSCIOFNC = OFF

#pragma config ICS = PGD2
#pragma config JTAGEN = OFF

#pragma config WDTEN = OFF

#pragma config IOL1WAY = OFF

#pragma config PWMLOCK = OFF

void InitOscillator(void);
void InitPWM(void);

int main(int argc, char** argv) {
    RCONbits.SWDTEN = 0;
    InitOscillator();
```

```
    InitPWM();
    while(1);
    return 0;
}

void InitOscillator (void)
{
    PLLFBD = 0b000110000;                 // M = 65
    CLKDIVbits.PLLPOST = 0;     // N2 = 2
    CLKDIVbits.PLLPRE = 0;      // N1 = 2
    OSCTUN = 0;

    __builtin_write_OSCCONH(0x01);
    __builtin_write_OSCCONL(0x01);
    while(OSCCONbits.COSC != 0b001);
    while(OSCCONbits.LOCK!=1){};

    ACLKCONbits.FRCSEL = 1;
    ACLKCONbits.SELACLK = 1;
    ACLKCONbits.APSTSCLR = 7;
    ACLKCONbits.ENAPLL =1;
    while(ACLKCONbits.APLLCK != 1);
}

void InitPWM (void)
{
    PTCONbits.PTEN = 0;
    PTCONbits.EIPU = 1;
    PTCON2bits.PCLKDIV = 0;
    PTCON2 = 0;
    PTPER = 9433;  //100 KHz

    //Configure PWM2
    PWMCON2bits.MTBS = 0;
    PWMCON2bits.ITB = 0; //PTPER provides PWM time period value
    PWMCON2bits.MDCS = 0;
    IOCON2bits.PENH = 1;
    IOCON2bits.PENL = 1;
    IOCON2bits.PMOD = 3;
    FCLCON2bits.FLTMOD = 3;
    FCLCON2bits.CLMOD = 1;
    PHASE2 = 0; //Switch 1 PS
    SPHASE2 = 4716; //Switch 8 PS
    PDC2 = (D1_MT - DT_MT); //Switch 1 DC
    SDC2 = (D2_MT - DT_MT); //Switch 8 DC

    //Configure PWM3
    PWMCON3bits.MTBS = 0;
    PWMCON3bits.ITB = 0;
    PWMCON3bits.MDCS = 0;
    IOCON3bits.PENH = 1;
    IOCON3bits.PENL = 1;
    IOCON3bits.PMOD = 3;
    FCLCON3bits.FLTMOD = 3;
    FCLCON3bits.CLMOD = 1;
    PHASE3 = 4716; //Switch 2 PS
    SPHASE3 = 0; //Switch 7 PS
```

```
    PDC3 = (D1_MT - DT_MT); //Switch 2 DC
    SDC3 = (D1_MT - DT_MT); //Switch 7 DC

    //Configure PWM4
    PWMCON4bits.MTBS = 0;
    PWMCON4bits.ITB = 0; //PTPER provides PWM time period value
    PWMCON4bits.MDCS = 0;
    IOCON4bits.PENH = 1;
    IOCON4bits.PENL = 1;
    IOCON4bits.PMOD = 3;
    FCLCON4bits.FLTMOD = 3;
    FCLCON4bits.CLMOD = 1;
    PHASE4 = 4716; //Switch 4 PS
    SPHASE4 = 0; //Switch 3 PS
    PDC4 = (D1_MT - DT_MT); //Switch 4 DC
    SDC4 = (D1_MT - DT_MT); //Switch 3 DC

    //Configure PWM5
    PWMCON5bits.MTBS = 0;
    PWMCON5bits.ITB = 0;
    PWMCON5bits.MDCS = 0;
    IOCON5bits.PENH = 1;
    IOCON5bits.PENL = 1;
    IOCON5bits.PMOD = 3;
    FCLCON5bits.FLTMOD = 3;
    FCLCON5bits.CLMOD = 1;
    PHASE5 = 4716; //Switch 6 PS
    SPHASE5 = 0; //Switch 5 PS
    PDC5 = (D1_MT - DT_MT); //Switch 6 DC
    SDC5 = (D2_MT - DT_MT); //Switch 5 DC

    PTCONbits.PTEN = 1;
    //Remapping pins
    int x = OSCCONbits.IOLOCK;

    __builtin_write_OSCCONL(OSCCON & 0xDF);
    x = OSCCONbits.IOLOCK;

    ANSELB = 0;
    RPOR3bits.RP39R = 0b110100; //set pin 18 as PWM4L
    RPOR3bits.RP38R = 0b110011; //Set pin 17 as PWM4H
    RPOR2bits.RP37R = 0b110110; //set pin 16 as PWM5L
    RPOR7bits.RP47R = 0b110101; //Set pin 15 as PWM5H
    __builtin_write_OSCCONL(0x46);
    __builtin_write_OSCCONL(0x57);
    OSCCONbits.IOLOCK = 1;
    //__builtin_write_OSCCONL(OSCCON | (1<<6));

}
```