

**MOSFET CURRENT SOURCE GATE DRIVERS, SWITCHING
LOSS MODELING AND FREQUENCY DITHERING CONTROL
FOR MHZ SWITCHING FREQUENCY DC-DC CONVERTERS**

by

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Abstract

The power density of a switching converter is dependent on the size of the power circuit components. Converters are operated in the hundreds of kHz to achieve high power density since the size of the converter reactive components decrease as frequency increases. Most present day low power (<200W) DC-DC converters operate at switching frequencies up to 500kHz. Some research has been conducted on converters that can operate above 500kHz up to 4MHz. In the near future, most DC-DC switching converters for communications and computers will operate at switching frequencies of 1-10MHz in order to achieve greater power density and improved transient response. To meet the next generation requirements of these applications, four new ideas are proposed in this thesis.

The first contribution is a new current source gate drive circuit for power MOSFETs. The circuit provides a nearly constant gate current to reduce switching transition times and therefore switching loss in power MOSFETs. In addition, it can recover a portion of the gate energy normally dissipated in a conventional driver. Demonstrated loss reduction of 24.8% at 10V/5A load are presented in comparison to a conventional voltage source driver for a boost converter switching at 1MHz.

The second contribution is a new high efficiency 1MHz synchronous buck voltage regulator using an improved current source driver. The proposed circuit achieves short rise and fall times to reduce switching loss in the buck HS MOSFET. It also recovers a portion of the SR gate energy, enabling a loss reduction of 24% at 1.3V/30A load in comparison to a conventional driver.

In the third contribution, a new switching loss model is proposed for synchronous buck voltage regulators. The model uses simple closed form equations to calculate the rise and fall times and piecewise linear approximations of the HS MOSFET voltage and current waveforms to

allow quick and accurate calculation of switching loss.

The final contribution is a new variable frequency digital control method for resonant converters, which is suitable for future applications switching at 10MHz. The proposed method uses frequency dithering to reduce the clock frequency demands of the digital controller.

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For Jennifer

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List of Symbols

$B_{ac\ pk}$	Magnetic core peak AC flux density
C	Capacitor
C_b	Bootstrap capacitance
C_{dsi}	MOSFET parasitic drain-to-source capacitance, where i corresponds to the MOSFET number
C_f	Converter powertrain output filter capacitance
C_g	MOSFET total parasitic gate capacitance
C_{gdi}	MOSFET parasitic gate-to-drain capacitance, where i corresponds to the MOSFET number
C_{gsi}	MOSFET parasitic gate-to-source capacitance, where i corresponds to the MOSFET number
C_{issi}	MOSFET parasitic input capacitance, where i corresponds to the MOSFET number
C_{issi_spec}	MOSFET parasitic input capacitance datasheet specification value, where i corresponds to the MOSFET number
C_m	Magnetic core loss constant
C_{ossi}	MOSFET parasitic output capacitance, where i corresponds to the MOSFET number
C_{ossi_spec}	MOSFET parasitic output capacitance datasheet specification value, where i corresponds to the MOSFET number
C_p	Resonant converter parallel capacitance
C_{res}	Resonant capacitance
C_{rssi_spec}	MOSFET parasitic gate-to-drain capacitance datasheet specification value, where i corresponds to the MOSFET number
C_s	Resonant converter series capacitance
d	MOSFET drain terminal
d_i	MOSFET drain terminal, where i corresponds to the MOSFET number
d_i'	MOSFET drain terminal including parasitic inductance, where i corresponds to

	the MOSFET number
D	Duty cycle
D_i	Diode, where i corresponds to the Diode number
D_b	Bootstrap diode
D_{C1}	Dither sequence steady-state duty cycle
D_{C2}	Dither sequence steady-state duty cycle plus one LSB dither
f	Frequency
f_{clock}	Clock frequency
f_{min}	Minimum steady-state frequency
f_r	Resonant frequency
f_s	Switching frequency
g_i	MOSFET gate terminal, where i corresponds to the MOSFET number
g_{fs}	MOSFET transconductance
i_d	MOSFET drain current
i_{dsi}	MOSFET drain current, where i corresponds to the MOSFET number drain current, ($i=1,2,3,\dots$)
i_{dsRMS}	RMS value of the MOSFET current
i_{D2}	Current through diode, D_2
i_g	Gate drive current
i_{Li}	i th inductor current, ($i=1,2,3,\dots$)
i_{Lf}	Output filter inductor current
i_{LM}	Magnetizing inductor current
i_{Lon}	Inductor current during turn on
i_{Lpre}	Inductor current during pre-charge
i_{Vcc}	Line current
i_{VccAVG}	Average line current

$i_{V_{ce}RMS}$	RMS line current
I_{ds}	Peak drain current
I_g	Average gate current
I_{g1f}	Average gate current during T_{1f}
I_{g2f}	Average gate current during T_{2f}
I_{g1r}	Average gate current during T_{1r}
I_{g2r}	Average gate current during T_{2r}
I_o	Load current
I_{off}	Current at turn off
I_{on}	Current at turn on
I_{onpk}	MOSFET turn on current
I_{onRMS}	RMS current during turn on
I_{pl_off}	Instantaneous plateau current during turn off
I_{pl_on}	Instantaneous plateau current during turn on
I_{preRMS}	RMS current during pre-charge
I_{rr}	Reverse recovery current
I_{rr_spec}	Datasheet specification values for the reverse recovery current
I_s	Series resonant current
I_{th_off}	Instantaneous gate threshold current at turn off
I_{th_on}	Instantaneous gate threshold current at turn on
$I_{V_{cc}RMS}$	RMS current during energy return interval
j	Imaginary $j = \sqrt{-1}$
K	Constant
L_i	Inductor, where ($i=1,2,3,\dots$) is the inductor number
L_f	Output filter inductor
L_{loop}	Inductance of the switching loop in a synchronous buck

L_m	Magnetizing inductance
L_{si}	i th series inductance, ($i=1,2,3,\dots$)
M_i	i th power MOSFET, ($i=1,2,3,\dots$)
n	Number of turns
N_{ADC}	Number of bits required for an ADC
N_{DFM}	Number of bits required for a DFM
N_{DPWM}	Number of bits required for an DPWM
$N_{DPWMeff}$	Effective DPWM resolution
N_p	Transformer primary turns
N_s	Transformer secondary turns
N_{stages}	Number of stages required for a ring oscillator
p_i	i th pole, ($i=1,2,3,\dots$)
P_{core}	Core loss
P_{cond}	Total conduction loss
P_g	MOSFET gate loss
P_{M1}	Loss in MOSFET M_1
P_{off}	Turn off loss
P_{off_conv}	Turn off switching loss for a conventional voltage source gate driver
P_{on}	Turn on loss
P_{on_conv}	Turn on switching loss for a conventional voltage source gate driver
P_{out}	Output power
P_{pre}	Power dissipation during pre-charge
P_{sw}	Total switching loss
P_{tot}	Total loss
P_{tot_sw}	Total turn on and turn off switching loss
P_{Vcc}	Power dissipated during energy return interval

Q	Quality factor of the load
Q_{FL}	Full load quality factor
Q_{gi}	i th MOSFET total gate charge, ($i=1,2,3,\dots$)
Q_{gd}	MOSFET gate-to-drain charge
Q_{NL}	No load quality factor
Q_{pl}	MOSFET total gate charge at the beginning of the plateau
Q_{rr}	Reverse recovery charge
Q_{rr_spec}	Datasheet specification values for the reverse recovery charge
Q_{th}	MOSFET total gate charge at the threshold
R_i	i th resistor, ($i=1,2,3,\dots$)
R_{ac}	AC resistance
R_{dc}	DC resistance
R_{ds}	MOSFET on resistance
R_{dson}	MOSFET on resistance
R_{ext}	External gate resistance
R_f	Fall time resistance
R_g	MOSFET internal gate resistance
R_{hi}	Resistance of the driver switch
R_{lo}	Driver low side switch resistance
R_L	Inductor copper loss
R_N	Sink impedance
R_O	Output resistance
R_{on}	On resistance
R_p	Source impedance
R_{pre}	Pre-charge resistance
R_r	Total series resistance in the gate drive path

$R_{V_{cc}}$	Energy return resistance
s	MOSFET source terminal [†]
s_i	MOSFET source, where ($i=1,2,3,\dots$) is the MOSFET number
s'	MOSFET source terminal including common source inductance
s'_i	MOSFET source terminal including common source inductance, where ($i=1,2,3,\dots$) is the MOSFET number
S_i	i th logic level control MOSFET, ($i=1,2,3,\dots$)
S_N	N-channel logic control level MOSFET
S_P	P-channel logic control level MOSFET
t	time
T_{1f}	Fall time interval 1
T_{1r}	Rise time interval 1
T_{2f}	Fall time interval 2
T_{2r}	Rise time interval 2
T_f	Fall time
T_{on}	Turn on time
T_{pre}	Inductor pre-charge interval (ns)
T_r	Rise time
T_{rr}	Total reverse recovery time
T_s	Switching period
$T_{V_{cc}}$	Energy return time
v_{Cres}	Resonant capacitor voltage
v_{ds}	Drain-to-source-voltage
v'_{ds}	Drain-to-source voltage
v_{gs}	MOSFET gate-to-source voltage

[†] In Chapter 3, Section 3.4.1.2, s denotes the Laplace transform variable.

v_{gsi}	MOSFET gate-to-source voltage, where ($i=1,2,3,\dots$) is the MOSFET number
v_{Ldi}	Voltage across parasitic drain inductance
v_{Lsi}	Voltage across parasitic source inductance
v_o	Output voltage
v_p	Transformer primary winding voltage
V_{cb}	Blocking capacitor voltage
V_{cc}	MOSFET driver supply voltage
V_{core}	Volume of the core
V_{dd}	Logic supply voltage
V_{ds}	Drain-to-source voltage
V_{ds_spec}	Datasheet voltage specification
V_F	Diode forward voltage drop
V_{gs1r}	Average gate voltage during T_{2f}
V_{in}	Input voltage
V_{inv}	Inverter output voltage
$V_{IN\ min}$	Minimum input voltage
V_O	Output voltage
V_{o_FL}	Full load output voltage
V_{o_NL}	No load output voltage
V_p	Peak overshoot voltage
V_{pl}	MOSFET plateau voltage
V_{pl_off}	MOSFET plateau voltage at turn off
V_{pl_on}	MOSFET plateau voltage at turn on
V_{th}	MOSFET threshold voltage
V_{ref}	Reference voltage
x	Core loss switching frequency parameter

γ	Core loss peak flux density parameter
α	Neper frequency
τ_{pre}	Inductor pre-charge interval time constant
τ_{Vcc}	Inductor energy return interval time constant
ω_o	Resonant frequency

Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuits
BJT	Bipolar Junction Transistor
CSD	Current Source Driver
DC	Direct Current
DFM	Discrete Frequency Modulation
DPWM	Discrete Pulse Width Modulation
DSP	Digital Signal Processors
IC	Integrated Circuits
EMI	Electrical Magnetic Interference
HS	High Side
LCC	Inductor Capacitor Capacitor
LSB	Least Significant Bit
MOSFET	Metal Oxide Silicon Field Effect Transistor
PCB	Printed Circuit Board
PSFB	Phase Shift Full-Bridge
PWM	Pulse Width Modulation
RLC	Resistance Inductor Capacitor
RMS	Root Mean Square
SR	Synchronous Rectifier
VCO	Voltage Controlled Oscillator
VR	Voltage Regulator

ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Prefixes for SI Units

p	Pico (10^{-12})
n	Nano (10^{-9})
μ	Micro (10^{-6})
m	Milli (10^{-3})
k	Kilo (10^3)
M	Mega (10^6)
G	Giga (10^9)

SI Units

A	Amperes
C	Coulombs
F	Farads
H	Henries
Hz	Hertz
s	seconds
V	Volts
W	Watts
°	Degrees
Ω	Ohms

Chapter 1

Introduction

1.1 Introduction

This section gives a general introduction to power electronics, power conversion and recent trends in power conversion. It lays the groundwork for the material presented in Chapters 2-6, which focus on gate drivers, switching loss models and control techniques for high switching frequency converters.

Power electronics is a field of electrical engineering concerned with the processing of electrical power between several forms using converters. Power electronic converters are used in nearly all electrical devices that we use in our daily lives. Applications include computers, consumer electronics, transportation electronics, telecommunications equipment, medical equipment, industrial electronics and many more.

Power electronic converters are classified in four categories:

- 1) DC-DC converters
- 2) DC-AC converters (inverters)
- 3) AC-AC converters
- 4) AC-DC converters (rectifiers)

The application requirements, efficiency, reliability, size and cost are the most important requirements an engineer must consider when designing a converter.

In the last twenty-five years, there has been rapid growth in the semiconductor industry. Integrated Circuits (ICs) are now used in most consumer and industrial electronic devices. These ICs usually require power to be delivered at low DC voltages, e.g. 5V, 3.3V, 2.5V, 1V etc. Since power consumption is proportional to frequency and to supply voltage squared, current trends

have IC supply voltages dropping to 1V and below to allow operating frequencies to increase. In addition, these low voltage loads require much higher current, faster transient response, tighter voltage regulation and lower voltage ripple. In telecommunications and computing applications, the bus voltages are higher DC voltages (e.g. 48V, 24V, 12V), so DC-DC converters are required to step down the bus voltages to meet the IC requirements. For this reason, there has been tremendous growth and research conducted in the area of DC-DC converters.

Historically, the linear regulator was the primary method used to create a regulated output voltage [1],[2]. However, the efficiency of converters using linear regulation suffers due to the large voltage drop across the series pass power device. The efficiency of a linear regulator is typically only 30-50%. Therefore heat sinks are usually required, which makes them uneconomical above 10W.

To meet power density and cost requirements, present day DC-DC converters are switching converters, which utilize MOSFETs as switches and diodes, or MOSFETs, for rectification. The switches and rectifiers are operated in the on or off state. Switching converters can be isolated, or non-isolated. Converters that include control are referred to as power supplies, or switching power supplies. There are many known converter topologies and perhaps hundreds of variations of these topologies. Furthermore, there are two principle classes of topologies: Pulse Width Modulation (PWM) mode and resonant mode.

In modern applications, the power density of power supplies is of critical importance. It is dependent on the size of all of the power circuit components, control and any heat sink devices. The size of the semiconductor switches is proportional to their power handling capability, which relates to the losses associated with the switches and ultimately the efficiency of the power supply. In addition, converters are operated at high frequencies to achieve high power density since the size of the converters reactive components decreases as frequency increases. Most

present day, low power ($< 200\text{W}$) DC-DC power supplies operate at switching frequencies between 200kHz and 500kHz. Some research has been conducted on converters that can operate above 500kHz up to about 4MHz and there are now commercial products available operating above 1MHz [3].

1.2 Research Motivation and Objectives

In modern computing applications, the power density of switching converters is of critical importance. As switching frequencies increase, power density can be improved by reducing converter size, since the size of the magnetic components and bulk storage capacitors decrease. Furthermore, operating at high frequency improves dynamic performance since higher switching frequencies allow for the design of wider bandwidth control loops.

This thesis addresses three areas related to high frequency operation: 1) reducing switching loss and gate loss, 2) quickly and accurately modeling switching loss, and 3) control for high frequency resonant converters.

1.2.1 Reducing Switching Loss and Gate Loss

Traditionally, the principle barrier to high frequency operation above 1MHz has been switching loss, which increases proportionally to switching frequency. Resonant and soft switching PWM topologies have been proposed and have demonstrated excellent ability to reduce or eliminate turn on switching loss. However, soft switching PWM topologies typically operate with high turn off switching loss and tend to operate with turn on switching loss at light load and/or maximum input voltage conditions. With the addition of snubber capacitors, resonant converters can minimize turn off switching loss, however the additional large and lossy magnetic components and their inherently high conduction loss make them poor candidates for many low cost computing applications. In these applications, the buck and boost converter topologies are

preferred due to their low component count and associated low cost, however both of these topologies have significant switching loss at high frequencies.

A second and less significant barrier to high frequency operation above 1MHz is gate drive loss. Solutions have been proposed to solve the gate loss problem [4]-[18], however there are inherent drawbacks in all of the proposed methods. All of the previously proposed methods suffer from at least one of several drawbacks, large magnetics, slow turn on/turn off of the switch being driven, high conduction loss in the driver switches and a lack of noise immunity in the circuit to prevent false triggering.

The main objective of the work presented in Chapters 3 and 4 is to present new current source gate drive circuits that can reduce switching loss and recover gate energy. In contrast to the traditional approach of eliminating switching loss by allowing the current or voltage to go to zero before the switching transition, the proposed circuits minimize switching loss by minimizing the switching transition times. As an added benefit, the small inductors in the proposed circuits store gate energy and then return it to the driver supply to recover some of the gate energy otherwise lost in conventional drivers.

1.2.2 Quick and Accurate Modeling of Switching Loss

In order to optimally design a high frequency switching converter, engineers and researchers begin their design by estimating the losses in a design file that is typically created using a spreadsheet, or other mathematical software. Device data sheet values and analytical models are used to calculate the losses. Using the loss models, many design parameters and components are compared to achieve a design with the optimal combination of efficiency and cost. At high switching frequencies approaching 1MHz and beyond, switching loss becomes a significant proportion of total losses, e.g. 50%, so accurate characterization of switching loss becomes

important for optimal design.

The conventional model proposed in [19] enables simple and rapid estimation of switching loss, however, the main drawback is that it neglects the switching loss dependences due to common source inductance and other circuit inductances. Comprehensive analytical models have been proposed in [20] and [21]. The basic idea of these models is to derive the current and voltage equations using the equivalent circuit of the power MOSFET during switching transitions, which is complex due to the high order differential equations required to obtain the model solution.

The objective of Chapter 5 is to present a new model that solves the complexity problem of the models in [20] and [21] while maintaining the main benefit of simplicity in the conventional model of [19]. The proposed model includes the common source inductance and other parasitic inductances to enable simple and accurate switching loss calculations.

1.2.3 Control for High Frequency Resonant Converters

As discussed in section 1.2.1, resonant converters are good candidate topologies for very high frequency operation in the MHz range due to their inherently low switching loss. Traditionally, computing and telecommunications applications have required constant frequency power conversion so that individual converters could be synchronized with the system. In order to operate at constant frequency, the asymmetrical pulse width modulation (PWM) technique and the phase shift technique [22]-[24] were proposed for resonant converters, but the adoption rate for the application of these techniques for resonant power conversion has not been very high. Recently, industry standards have changed with the proliferation of digital circuits, so that telecom networks have essentially become datacom networks, which don't require synchronization of the power converters, thereby permitting the use of variable switching

frequencies. In addition, the control problem has become more complicated as switching frequencies have increased, and will continue to increase in the future, with targets approaching 10MHz in the next ten years.

Given the problems outlined for future high frequency operation of DC-DC converters in the 1-10MHz range, the objective of Chapter 6 is to present a new digital control method to enable resonant converter operation in the 5-10MHz switching frequency range.

1.3 Thesis Organization

This thesis consists of seven chapters. Chapter 1 introduces the subject of DC-DC power converters with particular focus on the issues relevant to MHz switching frequency operation. This chapter establishes motivation and sets objectives for the research contributions presented in Chapters 3-6. A literature review on gate drivers, resonant gate drivers, switching loss models and control techniques are presented in Chapter 2. Chapter 3 proposes a new current source gate driver for ground referenced power MOSFET switches driven at logic level supply voltages. The boost converter topology is used to demonstrate the advantages of the proposed driver. The driver loss analysis, design procedure, logic implementation and experimental results are presented. An alternate implementation of the driver is also included. Chapter 4 introduces a new current source gate driver for a 1MHz synchronous buck converter. The driver loss analysis, design with optimization, logic and level shift implementations and experimental results are presented. A new practical and accurate analytical switching loss model for conventional voltage source gate drivers and current source gate drivers is presented in Chapter 5. Simulation and experimental results are presented to verify the model. Chapter 6 introduces a new digital control method for variable frequency resonant converters. Simulation results are presented to verify the control method. Chapter 7 summarizes the contributions of the research presented in this thesis

and gives recommendations for future work.

1.4 Thesis Publications

This thesis contains three chapters that present results that have been published in the form of IEEE refereed papers. The complete citations for these papers and the chapters in which they appear are provided as follows:

Chapter 3 - A Current Source Driver Achieving Switching Loss Reduction and Gate Energy Recovery at 1MHz:

[1] **W. Eberle**, Z. Zhang, Y.F. Liu and P.C. Sen, "A Current Source Gate Driver Achieving Switching Loss Savings and Gate Energy Recovery at 1-MHz," IEEE Trans. Power Electron., in press, TPEL-2007-05-0257.

[2] **W. Eberle**, Y.F. Liu and P.C. Sen, "A Novel High Efficiency Resonant Gate Driver with Efficient Energy Recovery and Low Circulating Current" IEEE Trans. Industrial Electron., in press, TIE00485-2005.

[3] **W. Eberle**, Y.F. Liu and P.C. Sen, "A Resonant Gate Drive Circuit with Reduced MOSFET Switching and Gate Losses", in proc. IEEE Industrial Electronics Society Conf. (IECON), Nov. 2006, pp. 1745-1750.

[4] **W. Eberle**, P.C. Sen and Y.F. Liu, "A Novel High Performance Resonant Gate Drive Circuit with Low Circulating Current", in proc. IEEE Applied Power Electronics Conf. (APEC), Mar. 2006, pp. 324-330.

[5] **W. Eberle**, P.C. Sen and Y.F. Liu, "A New Resonant Gate Drive Circuit with Efficient Energy Recovery and Low Conduction Loss", in proc. IEEE Industrial Electronics Society Conf. (IECON), Nov. 2005, pp. 650-655.

Chapter 4 - A High Efficiency MHz Synchronous Buck Voltage Regulator with Current Source Gate Driver:

[1] **W. Eberle**, Z. Zhang, Y.F. Liu and P.C. Sen, "A High Efficiency MHz Synchronous Buck Voltage Regulator with Current Source Gate Driver," IEEE Trans. Power Electron., submitted, TPEL-2008-02-0067.

[2] **W. Eberle**, Z. Zhang, Y.F. Liu, and P.C. Sen, "A High Efficiency Synchronous Buck VRM with Current Source Gate Driver," in proc. IEEE Power Electronics Specialists Conf. (PESC), Jun. 2007, pp. 21-27.

Chapter 5 – A Practical and Accurate Switching Loss Model for Buck Voltage Regulators:

[1] **W. Eberle**, Z. Zhang, Y.F. Liu and P.C. Sen, "A Practical Switching Loss Model for Buck Voltage Regulators," IEEE Trans. Power Electron., submitted, TPEL-2008-02-0070.

[2] **W. Eberle**, Z. Zhang, Y.F. Liu and P.C. Sen, "A Simple Switching Loss Model for Buck Voltage Regulators with Current Source Drive," in proc. IEEE Power Electronics Specialists Conf. (PESC), Jun. 2008, in press.

[3] **W. Eberle**, Z. Zhang, Y.F. Liu and P.C. Sen, "A Simple Analytical Switching Loss Model for Buck Voltage Regulators," in proc. IEEE Applied Power Electronics Conf. (APEC), Feb. 2008, pp. 36-42.

Chapter 2

Literature Review

2.1 Introduction

In this chapter a critical review of literature relevant to the three main thesis topics is presented. The three main thesis topics are all related to low power, high frequency DC-DC converters. They include: 1) MOSFET gate drive including switching and gate driving loss, 2) modeling of switching loss, 3) control for MHz switching frequency resonant converters.

In section 2.2, an overview of DC-DC converters is presented. Loss mechanisms in DC-DC converters are discussed in section 2.3. A review of MOSFET gate drive techniques is presented in section 2.4, followed by a review of switching loss models in section 2.5. Reviews of analog and digital converter control techniques are presented in sections 2.6 and 2.7, respectively. The conclusions are presented in section 2.8.

2.2 DC-DC Converter Types

The majority of DC-DC converters are either pulse width modulated (PWM) DC-DC converters, or resonant mode DC-DC converters. These two types of converters are described in the following sub-sections.

2.2.1 PWM DC-DC Converters

PWM DC-DC converters are the most common class of DC-DC converters in telecommunications and computing applications. A block diagram of a switch mode DC-DC converter is illustrated in Figure 2.1. Most PWM DC-DC converters consist of an inverter, a rectifier, a filter and a transformer for isolation if required. The inverter creates a high frequency square wave voltage which is rectified and then filtered to produce a DC output voltage.

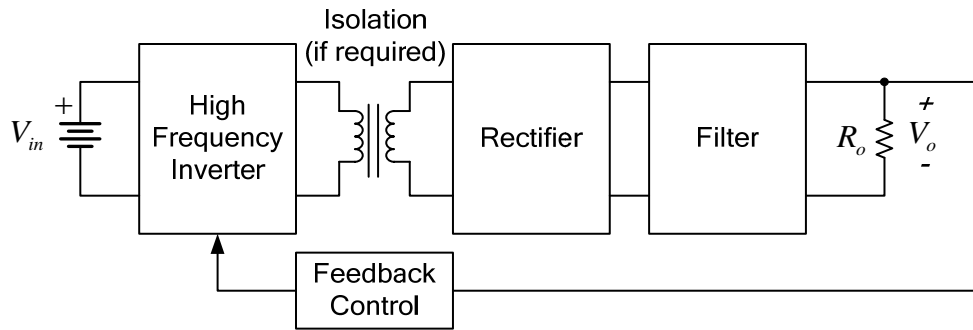


Figure 2.1 Block diagram of a switch mode DC-DC converter

2.2.2 Resonant Mode DC-DC Converters

Resonant mode DC-DC converters are the second class of DC-DC converters used in telecommunications and computing applications. A block diagram of a resonant mode DC-DC converter is illustrated in Figure 2.2. All resonant DC-DC converters consist of an inverter, a resonant circuit, a rectifier, a filter and a transformer for isolation if required. The inverter creates a high frequency square wave voltage which is then filtered by the resonant circuit, rectified and then filtered to produce a DC output voltage.

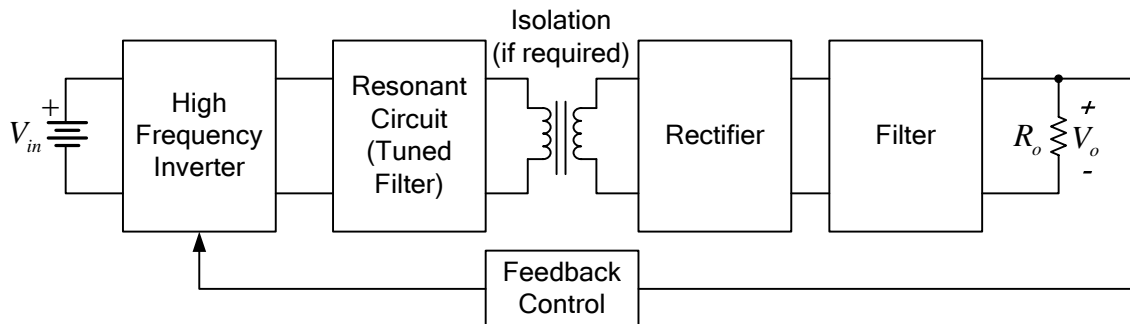


Figure 2.2 Block diagram of a resonant DC-DC converter

The resonant circuit can be considered as a tuned filter that allows frequency signals near the resonant frequency to pass through while filtering out all other harmonics. Therefore, the resonant circuit behaves as a sinusoidal source. Typically, the resonant circuit is tuned close to the switching frequency. It can be demonstrated that resonant converters can achieve zero current

switching (ZCS) if operated below the resonant frequency (leading current), or they can achieve zero voltage switching (ZVS) if operated above the resonant frequency (lagging current). However, since low power DC-DC converters use power MOSFETs as the switches, operation above resonant frequency is preferred to eliminate the losses associated with the MOSFET output capacitance.

The advantages of resonant converters in comparison to PWM converters are lower switching losses and reduced electromagnetic interference (EMI) due to the sinusoidal nature of the voltages and/or currents. The disadvantages are increased conduction losses and high component stress for the resonant components.

2.3 Review of Losses in Switching Power Converters

The purpose of DC-DC converters is to increase or decrease the output voltage with respect to the input. The efficiency of a converter is a measure of the ratio of the output power supplied to the load with respect to the input power. The input power is equal to the load power plus the converter losses. Converters have losses in their control circuits and magnetics, however, the greatest sources of loss are in the converter switching power MOSFETs. These losses are briefly discussed in the following sub-sections.

2.3.1 MOSFET Frequency Dependent Losses

MOSFETs exhibit three types of frequency dependent loss: 1) Gate Loss, 2) Switching Loss, and 3) Output Loss. The MOSFET equivalent circuit is shown in Figure 2.3. The terminal labeled d is the drain. The terminal labeled s is the source and the terminal labeled g is the gate. The MOSFET equivalent circuit includes a body diode, which is due to the physical structure of the device. In addition, it includes effective terminal capacitances, which are device parasitics due to the physical structure.

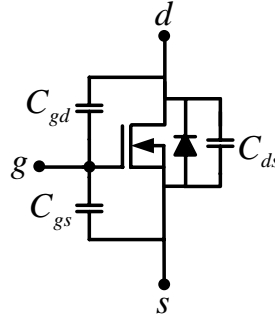


Figure 2.3 MOSFET equivalent circuit including the body diode and parasitic terminal capacitances

2.3.1.1 Gate Loss

Energy is required in order to charge and discharge the MOSFET parasitic gate capacitances, C_{gs} and C_{gd} , each switching period. This energy is usually dissipated through resistance in series with the gate within the gate drive circuit. MOSFET gate loss, P_g , is given by (2.1), where Q_g is the total gate charge, f_s is the switching frequency and V_{cc} is the driver supply voltage.

$$P_g = Q_g V_{cc} f_s \quad (2.1)$$

For typical low power DC-DC switching converters, Q_g is approximately 10-100nC and V_{cc} is 5-10V. The total gate loss for a converter is the sum of the gate loss for each switch. For most converters, the gate energy losses become a concern at switching frequencies beyond 1MHz.

2.3.1.2 Switching Loss and Output Loss

The second and third frequency dependent components of switch device loss in converters are closely related - they are switching loss and output loss due to the switch output capacitance, C_{ds} . Switching loss, P_{sw} , occurs during switching transitions and is due to a positive volt-ampere product of the switch current and drain-to-source voltage as given by (2.2). The constant K , is typically between 1/6 and 1/2. The MOSFET rise and fall times, T_r and T_f can be obtained from data sheets. The output loss, P_{out} , is energy lost when the switch output drain-to-source capacitance is discharged during turn on as given by (2.3).

$$P_{sw} = K(T_r + T_f)V_{ds}I_{ds}f_s \quad (2.2)$$

$$P_{out} = \frac{1}{2}C_{ds}V_{ds}^2f_s \quad (2.3)$$

Converter device switching transitions can generally be classified as hard-switching, or soft-switching.

Typical piecewise linear hard-switching waveforms are illustrated in Figure 2.4. In Figure 2.4, v_{gs} is the MOSFET gate-to-source voltage, i_{ds} represents the MOSFET current and v_{ds} represents the voltage across the drain-to-source. P_{sw} is the product of v_{ds} and i_{ds} . Switching loss occurs at turn on when v_{gs} transitions from V_{th} to V_{pl} (when $v_{ds}=0$) and at turn off when v_{gs} transitions from V_{pl} (when v_{ds} begins to ramp up) down to V_{th} . Another problem that arises from hard-switching is EMI due to the high dv/dt and di/dt during the transitions.

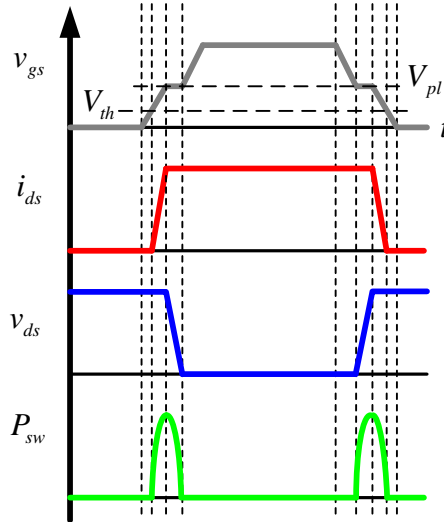


Figure 2.4 Typical piecewise linear hard-switching MOSFET waveforms with switching times exaggerated

Soft-switching transitions can be further classified as ZVS, or ZCS. The goal of soft-switching is to eliminate these switching loss components in (2.2) and (2.3) for a converter and thereby recover the energy that would otherwise be lost. Soft-switching techniques can be used in switch mode circuits to reduce, or eliminate turn on loss. For resonant converters, soft-

switching is inherent due to the sinusoidal nature of the waveforms. Additional parallel external snubbing capacitance can minimize turn off loss for switch mode and resonant mode converters by slowing down the rise time of the drain-to-source voltage during turn off. ZVS is the preferred soft-switching method for MOSFETs because it eliminates the losses associated with the output capacitance – this energy is discharged to the source or load during the high-to-low voltage transition. This energy is not recovered in the ZCS case.

2.3.2 MOSFET Non-Frequency Dependent Losses

Neglecting the skin effect in the leads, MOSFET conduction loss is essentially non-frequency dependent. MOSFET conduction loss is usually the largest non-frequency dependent loss in a converter operating below 500kHz. In the on state, MOSFETs do not behave as an ideal switch with zero impedance, but they behave like a small resistance. This resistance is typically called the R_{ds} , or R_{dson} of the MOSFET. Typical values of R_{ds} for present day MOSFETs range from about 1-100m Ω for MOSFETs with an off state voltage stress rating of 200V. The conduction loss of a MOSFET, P_{cond} , is given by (2.4), where i_{dsRMS} is the RMS value of the MOSFET current.

$$P_{cond} = i_{dsRMS}^2 R_{ds} \quad (2.4)$$

Synchronous rectification is the use of a MOSFET instead of a diode rectifier. In recent years, the use of MOSFETs as synchronous rectifiers (SRs) has become essential for high current low output voltage applications because rectifier conduction losses can be significantly reduced. The main drawbacks of synchronous rectification are the requirement of control circuitry to control the timing of the on-state of the SR and the addition of gate loss not present in diode rectifiers. In addition, since the MOSFET is a bi-directional switch, if a MOSFET SR is not properly controlled, “shoot-through” current can result.

2.3.3 Other Sources of Loss in Power Converters

There are three other main sources of loss in power converters: 1) copper loss, 2) control loss and 3) core loss. Copper loss is generally distributed among the various printed circuit board (PCB) traces on a converter, however since magnetic components typically require multiple turns around the magnetic cores, copper losses associated with magnetics can be significantly higher than those attributed to PCB traces. It is common to assume that resistance is non-frequency dependent, so $R_{dc}=R_{ac}$. However, due to the skin effect, this assumption can become inaccurate as frequencies and/or harmonic content increase.

Control losses are usually small (typically < 0.5-1W). They are attributed to the control ICs and any external biasing circuits.

Core loss, consisting of hysteric loss and eddy current loss, occurs in all magnetic components. All DC-DC converters utilize at least one filter inductor, or inductance as energy storage in a transformer. All isolated DC-DC converters require a transformer to achieve isolation. Core loss, P_{core} , can be estimated using (2.5), where C_m , x and y are constants related to the magnetic material, f_s is the switching frequency, $B_{ac\ pk}$ is the peak AC flux density and V_{core} is the volume of the core [25]. Typical values for C_m , x and y are $C_m=2*10^{-2}$, $x=1.8$ and $y=2.5$ for Ferroxcube 3F3 material, which is popular for switching converters operating in the 300-500kHz switching frequency range.

$$P_{core} = C_m f_s^x B_{ac\ pk}^y V_{core} \quad (2.5)$$

2.4 Review of Gate Drive Techniques

Gate drive circuits are circuits designed to provide current sourcing and sinking capability in order to charge and discharge the power MOSFET parasitic capacitances during switching. Traditionally, the conventional voltage source gate drive circuit discussed in sub-section 2.4.1 has

been used. Since the early 1990s, resonant gate drive circuits have been proposed as a drive circuit option to recover a portion of the gate loss given by (2.1). Sub-section 2.4.2 reviews many of the recent resonant gate drive circuits.

2.4.1 Conventional Voltage Source Gate Drive

A conventional gate drive circuit is illustrated in Figure 2.5 to drive a power MOSFET, M . Its associated waveforms are given in Figure 2.6. With these drivers, all of the power MOSFET gate energy is dissipated. Energy is absorbed from the line source, V_{cc} , during the turn on of M and then dumped to ground during turn off. Examining Figure 2.6, it is clear that the line current, $i_{V_{cc}}$ only contains a positive component. Since there is no negative component, no energy is returned to the line.

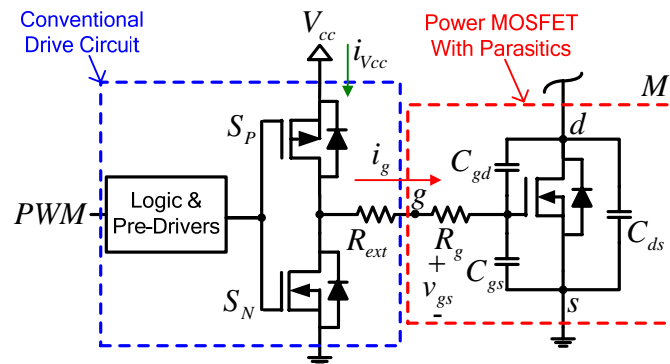


Figure 2.5 Conventional gate drive circuit with power MOSFET and its associated parasitics

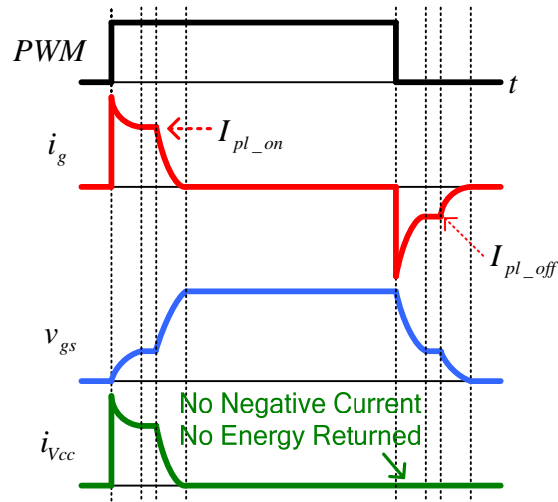


Figure 2.6 Power MOSFET gate drive waveforms with conventional gate drive

For the conventional driver, the gate energy loss due to charging and discharging the gate capacitance of M is given by (2.1). The gate energy is dissipated as RMS loss in: 1) the driver switches S_N and S_P , 2) the external resistance, R_{ext} , and 3) the MOSFET internal gate mesh resistance, R_g , of M . This loss component is well understood and is often called the QV gate loss, representing the product of the total gate charge, Q_g and driver supply voltage, V_{cc} . In addition to the QV loss, conventional gate drivers exhibit switching loss, shoot-through loss and gate loss in their switches. These losses are often neglected by engineers, providing an underestimate of the total drive loss. It was demonstrated in [26] that the power MOSFET QV RMS loss is approximately only 66.7% of the total gate drive circuit loss. The additional components of the gate drive circuit loss include approximately 17.6% for switching loss and 15.7% for gate loss in the driver switches. As illustrated in Figure 2.7, normalized with respect to the QV RMS gate loss, these components are significant. An additional 26% of loss can be attributed to hard switching in the driver switches and 24% to gate loss in the driver switches. Neglecting these components yields an under estimate of gate loss that neglects an additional 50% of the total gate circuit loss.

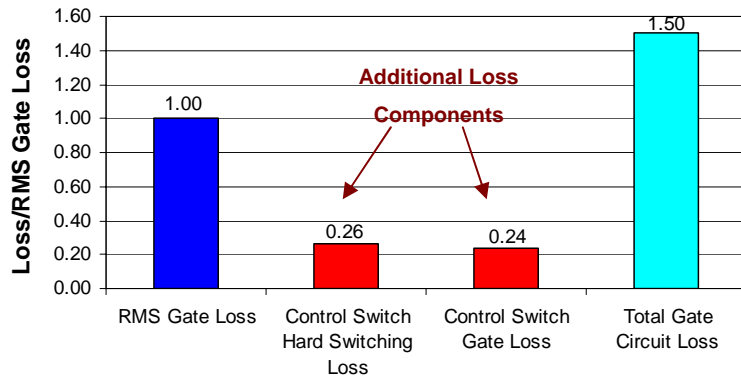


Figure 2.7 Conventional gate drive circuit loss normalized with respect the power MOSFET RMS gate loss

The problems of the conventional gate driver extend beyond the gate drive circuit loss of (2.1). There are two other significant problems:

1) Since these drivers operate with voltage source RC type charging and discharging, switching speed is limited. The MOSFET gate current is limited to a value significantly less than the peak driver current during the turn on and turn off times which occur during the plateau and threshold regions of the MOSFET gate-to-source voltage. This effect is clearly illustrated in Figure 2.6, where the drive current at turn on and turn off decays significantly. During the turn on switching time from the threshold to the end of the Miller plateau, the gate current decays to I_{pl_on} . During the turn off switching time, the problem is even more severe since the gate current decays to I_{pl_off} . Some conventional drivers attempt to overcome this problem with bipolar junction transistor (BJT) driver switches operating as current sources in the active region, however, due to the limited gains of the devices, they do not behave as ideal current sources.

2) A second significant problem is that these drivers typically have a large source impedance (e.g. several Ω s), so the gate drive voltage often does not reach the driver supply voltage, V_{cc} when the MOSFET is turned on. This leads to greater conduction loss since the MOSFET R_{dson} decreases with increasing gate voltage. This effect is illustrated in Figure 2.8, where it is clear

that the MOSFET gate voltage never reaches the driver supply voltage of 5V. Furthermore, the very large source impedance leads to very slow turn on and therefore high turn on switching loss.

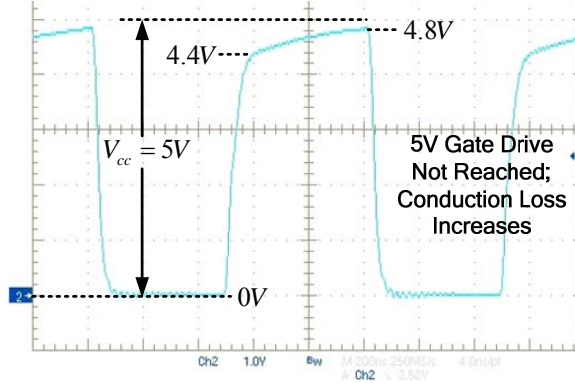


Figure 2.8 Typical MOSFET gate voltage waveform illustrating that the gate voltage amplitude does not reach the control voltage of 5V; UCC37322 driving IRF6618 at 1MHz (Y-axis: 1V/div, X-axis: 200ns/div)

For these two reasons, conventional gate drivers are not optimized to minimize switching loss or conduction loss.

2.4.2 Resonant Gate Drivers

In order to recover a portion of the gate energy otherwise lost in conventional drivers, several papers have been published since the early 1990s proposing resonant gate drive techniques. Several of the proposed drivers are critically reviewed in this sub-section. Following the review, a brief summary is presented highlighting the drawbacks of the existing circuits.

One of the first resonant gate drive circuits was proposed in [4]. The circuit and its associated waveforms are given in Figure 2.9. In Figure 2.9, S_1 and S_2 represent the gating waveforms for MOSFETS S_1 and S_2 , v_{gs} represents the gate-to-source voltage of power MOSFET, M , i_L represents the inductor current and i_g represents the gate current. This circuit uses an auxiliary inductor, L , which operates in continuous conduction mode and a resonant capacitor, C_{res} , along with two control switches, S_1 and S_2 , to recover a portion of the gate energy. There are two significant advantages of this technique. First, the switch being driven, M , is

driven by an essentially constant current source during its transitions, so its associated turn on and turn off times can be quick. In addition, switches S_1 and S_2 clamp the gate high and low during the on and off states, respectively, thereby eliminating false triggering of the MOSFET gate. The disadvantage of this technique is the existence of significant circulating current during the on and off states of M , so the control switches must be selected with relatively low R_{ds} ratings and therefore high gate charge. In addition, the inductor required is relatively large since the current is continuous. The circuit in [4] achieved a 3% efficiency improvement for a 20W converter operating at 2MHz in comparison to a conventional driver.

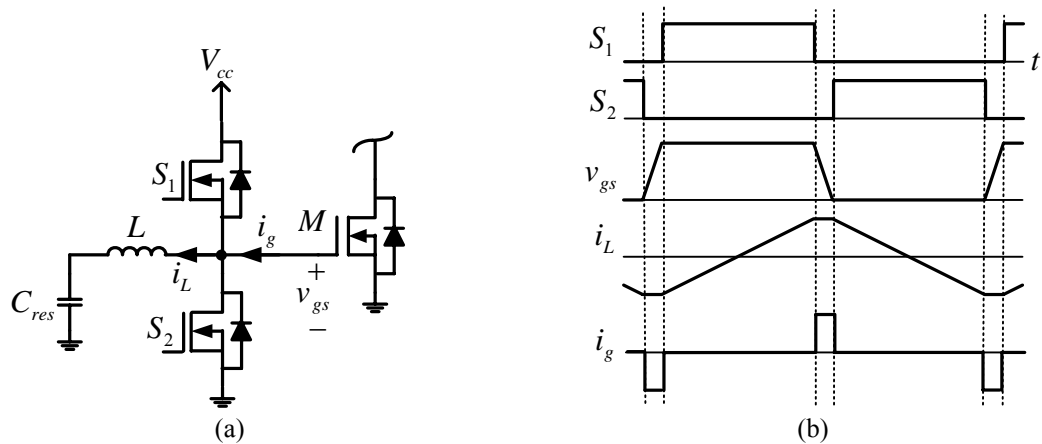


Figure 2.9 Resonant transition gate driver [4]; (a) circuit and (b) waveforms

Following the resonant transition technique, the resonant pulse technique was proposed in [5]. The circuit and its associated waveforms are illustrated in Figure 2.10. In Figure 2.10, S_1 , S_2 and S_3 represent the gating waveforms for MOSFETS S_1 , S_2 and S_3 , v_{gs} represents the gate-to-source voltage of power MOSFET, M , i_L represents the transformer and gate current and $v_{C_{res}}$ represents the voltage across the resonant capacitor, C_{res} . The leakage inductance of the transformer is used to resonate with C_{res} to form the energy recovery circuit. Switch S_3 is gated simultaneously with S_1 to reset the resonant capacitor. The advantages of the resonant transition technique are low conduction losses and gate drive isolation. The disadvantage is slow turn on

and turn off since the power MOSFET gate must be charged and discharged through the leakage inductance with initially zero current. Furthermore, the power MOSFET gate is driven without a DC component, so there is excess negative charge energy.

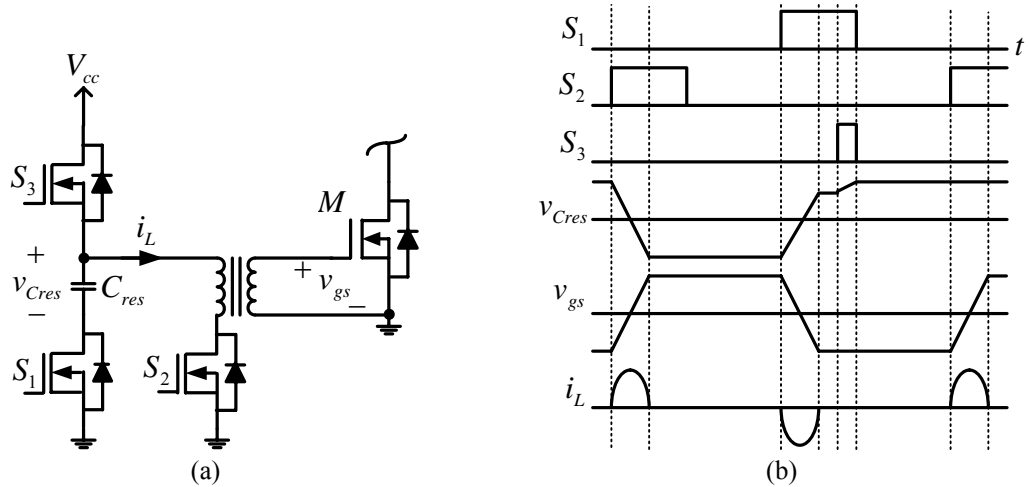


Figure 2.10 Resonant pulse gate driver [5]; (a) circuit and (b) waveforms

In 1993, a resonant gate driver was proposed utilizing a coupled inductor in series with two control switches to eliminate cross conduction and reduce linear operation losses in the control switches in addition to providing partial gate energy recovery [6]. The circuit and waveforms are illustrated in Figure 2.11. In Figure 2.11, S_1 and S_2 represent the gating waveforms for MOSFETS S_1 and S_2 , v_{gs} represents the gate-to-source voltage of power MOSFET, M , and i_g represents gate current. The diodes provide clamping for the gate voltage to prevent over voltage and negative voltage conditions at the gate. However, the diodes do not provide a low impedance path to eliminate spontaneous turn on due to noise spikes. The most significant drawback of this circuit is the inherent slow turn on and turn off since the gate must be charged and discharged through the inductance with zero initial current.

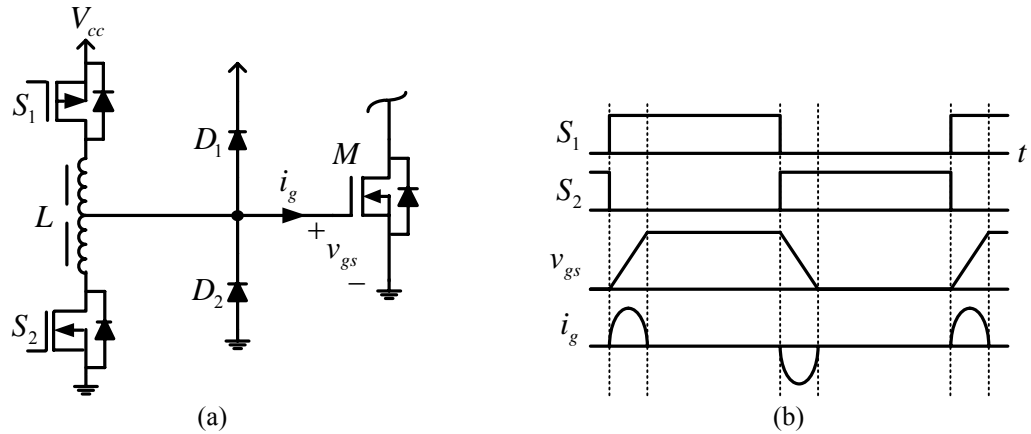


Figure 2.11 Coupled inductor resonant gate driver [6]; (a) circuit and (b) waveforms

A dual high-side/low-side resonant gate driver was proposed [7]. The circuit and its associated waveforms are illustrated in Figure 2.12. In Figure 2.12, S_1 - S_5 represent the gating signals for MOSFETS S_1 - S_5 , i_{L1} and i_{L2} represent the coupled inductor currents and v_{gs1} and v_{gs2} represent the gate-to-source voltages of M_1 and M_2 , respectively. The circuit promises low conduction losses since the inductor current is discontinuous. Only one core is used to form the coupled inductor pair, which helps to reduce the size of the circuit. In addition, control switch S_5 actively clamps the gate of the bottom switch, M_2 , low during its off time, thereby eliminating spontaneous turn on of M_2 caused by Cdv/dt after it is normally turned off. The disadvantages of the proposed method are slow turn off of the top and bottom switches in addition to the complexity of the logic required to generate the control switch gating signals. The circuit in [7] achieved a 3% efficiency improvement at full load for a 20W synchronous buck converter operating at 1MHz in comparison to a conventional driver.

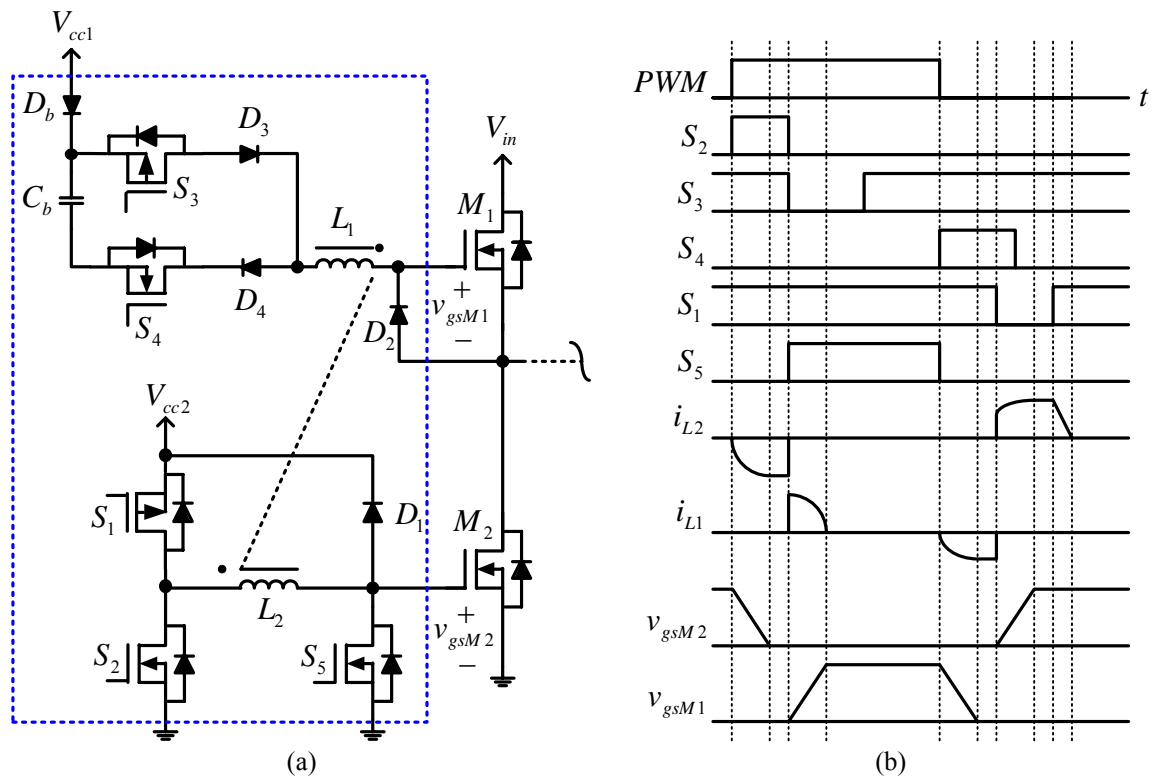


Figure 2.12 High/Low coupled inductor resonant gate driver [7]; (a) circuit and (b) waveforms

Yet another resonant gate drive circuit was proposed in [8]. The circuit and its waveforms are given in Figure 2.13. In Figure 2.13, S_1 - S_3 represent the gating waveforms for MOSFETS S_1 - S_3 , i_L represents the inductor current, i_{D2} represents the diode current in D_2 and v_{gs} represents the gate-to-source voltage of power MOSFET, M . Control switches S_1 and S_2 actively clamp the gate of M , high and low during its respective on and off times. The circuit only recovers the gate energy during turn off and it does so with a slow transition. The turn on gate loss is the same as a conventional gate driver.

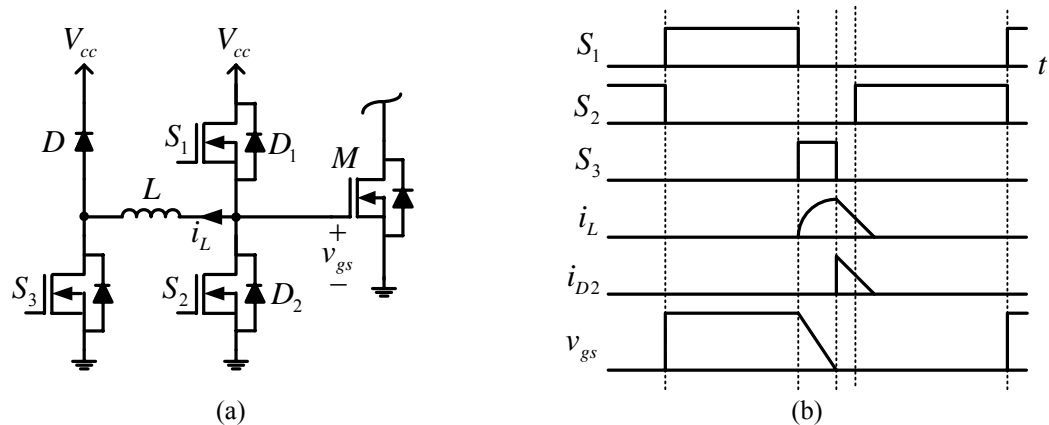


Figure 2.13 Resonant gate driver proposed in [8]; (a) circuit and (b) waveforms

In addition to [4]-[8], in order to recover a portion of the gate energy otherwise lost in conventional drivers, several other papers have been published since the early 1990s proposing resonant gate drive techniques [9]-[18]. In most of these techniques, the inductance is used to resonate with the gate capacitance for charging, so switching speed is limited. Of the methods previously proposed, all of them suffer from at least one of seven problems:

- 1) High circulating current in the driver switches during the power MOSFET on and off states resulting in excessive conduction loss [4],[11]-[14].
- 2) Peak driver current dependent on duty cycle, or switching frequency resulting in switching times that vary with the operating point [4],[11]-[14].
- 3) High transient current in the driver switches during transients due to the DC energy storage in the blocking capacitance [4],[11]-[14].
- 4) Large inductance [4],[11]-[12], bulky transformer, or coupled inductor [6],[10],[13]-[14],[16].
- 5) Slow turn on and/or turn off transition times, which increases both conduction and switching losses in the power MOSFET due to charging the power MOSFET gate beginning at zero inductor current [5]-[10],[15]-[18].

- 6) The inability to actively clamp the power MOSFET gate to the line during the on time and/or to ground during the off time, which can lead to undesired false triggering of the power MOSFET gate, i.e. lack of Cdv/dt immunity [5]-[6],[9]-[10],[16]-[18].
- 7) Only low side, ground referenced drive [4]-[6],[11],[14]-[18].

To solve the problems inherent to conventional drivers, the problems above for existing resonant drivers and to reduce switching loss, new current source gate drive circuits are proposed in Chapters 3 and 4. Both drivers achieve the two main requirements of a good driver cited in the conclusion of [27], namely current source drive during transitions to achieve high speed drive and operate as a low impedance voltage source during the on and off states to minimize false triggering.

2.5 Review of Switching Loss Models

In order to optimally design a high frequency switching converter, engineers and researchers begin their design by estimating the losses in a design file that is typically created using a spreadsheet, or other mathematical software. Device data sheet values and analytical models are used to calculate the losses. Using the loss models, many design parameters and components are compared to achieve a design with the optimal combination of efficiency and cost.

Many models have been proposed to achieve accuracy in loss modeling. These models can generally be classified in one of three categories: 1) physics based models, 2) behaviour models, and 3) analytical models.

The physics based model uses the device parameters including geometry and doping as input for device simulation to do finite element analysis. In general, the results can be very accurate, however the simulations are very slow (e.g. several days for one data set). Another significant drawback is that the semiconductor parameters are not always known, or available from the

semiconductor manufacturers. Furthermore, the modeling results are data points and not closed form mathematical expressions that can be easily used in a design file by an engineer. For these reasons, this model is rarely used by engineers.

Behaviour models also rely on circuit simulation, however, they provide a good tradeoff between accuracy and simulation time. Simulations are conducted typically in seconds, or minutes using Spice based simulators, or SABER, with models provided by semiconductor manufacturers. These models have the same drawback as the physics based model in that the results are produced as data points and not closed form expressions that can be used to produce optimization curves.

Analytical models are math based. Most often, piecewise linear turn on and turn off waveforms are used, or simplified equivalent circuits are used to derive switching loss equations. These methods yield closed form mathematical expressions that can be easily used to produce optimization curves within a design file, however the challenge is to improve accuracy while minimizing complexity.

One of the most popular analytical models is the piecewise linear model presented in [19]. This model is referred to as the conventional model and is used as a benchmark later for comparison purposes with the proposed model in Chapter 5. In the proposed model, an estimate of the MOSFET switching loss is calculated using simplified piecewise linear approximations of the gate drive current, i_g , drain current, i_{ds} , and drain voltage, v_{ds} , waveforms during periods T_2 and T_3 of the switching transitions. The equivalent circuit during turn on and its associated waveforms are illustrated in Figure 2.14. In Figure 2.14, R_{hi} represents the source impedance of the driver, V_{th} represents the MOSFET threshold voltage, and V_{pl} represents the MOSFET plateau voltage.

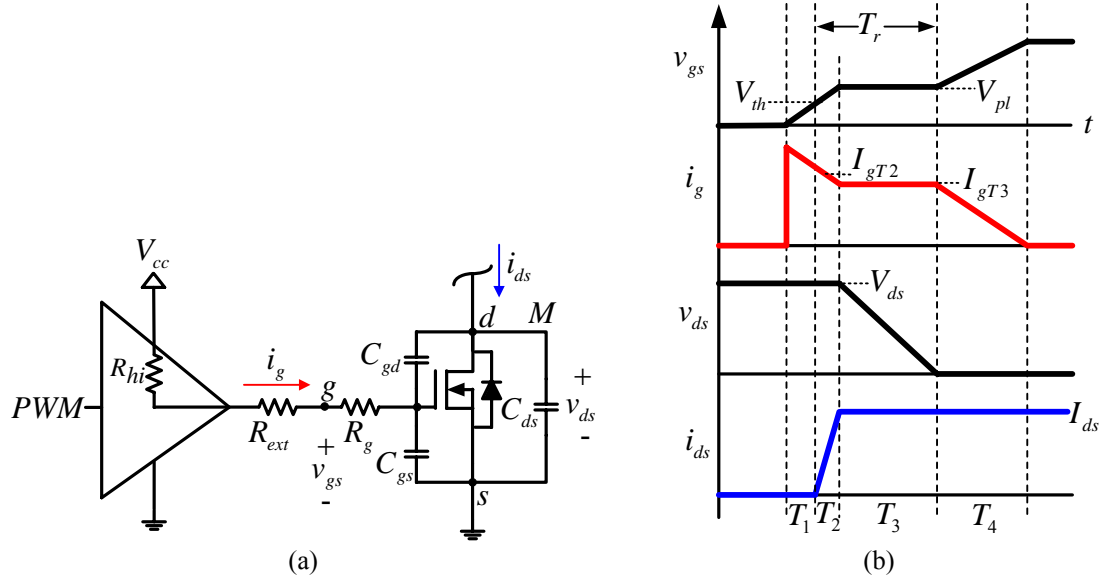


Figure 2.14 Power MOSFET turn on model proposed in [19]; (a) circuit and (b) waveforms

The average gate drive currents during T_2 and T_3 , I_{gT2} and I_{gT3} , are given by (2.6) and (2.7).

$$I_{gT2} = \frac{V_{cc} - 0.5(V_{pl} + V_{th})}{R_{hi} + R_{ext} + R_g} \quad (2.6)$$

$$I_{gT3} = \frac{V_{cc} - V_{pl}}{R_{hi} + R_{ext} + R_g} \quad (2.7)$$

Assuming that I_{gT2} charges the input capacitors of the MOSFET from V_{th} to V_{pl} and I_{gT3} is the discharge current of the C_{gd} capacitor while the drain voltage changes from V_{ds} to 0V, the approximate switching times are given by (2.8) and (2.9). The rise time, T_r is the sum of T_2 and T_3 as given by (2.10).

$$T_2 = (C_{gs} + C_{gd}) \frac{V_{pl} - V_{th}}{I_{gT2}} \quad (2.8)$$

$$T_3 = C_{gd} \frac{V_{ds}}{I_{gT3}} \quad (2.9)$$

$$T_r = T_2 + T_3 \quad (2.10)$$

During T_2 , the drain voltage is V_{ds} and the current is ramping from 0A to the load current, I_{ds} . During T_3 , the drain voltage is falling from V_{ds} to 0V. Using linear approximations of the

waveforms, the power loss components for the respective intervals are estimated by (2.11) and (2.12), where T_s is the switching period. The total turn on switching loss is the sum of the two components, yielding (2.13).

$$P_2 = \frac{T_2}{T_s} V_{ds} \frac{I_{ds}}{2} \quad (2.11)$$

$$P_3 = \frac{T_3}{T_s} \frac{V_{ds}}{2} I_{ds} \quad (2.12)$$

$$P_{on} = \frac{1}{2} V_{ds} I_{ds} T_r f_s \quad (2.13)$$

The equivalent circuit during turn off and its associated waveforms are illustrated in Figure 2.15. In Figure 2.15, R_{lo} represents the sink impedance of the driver

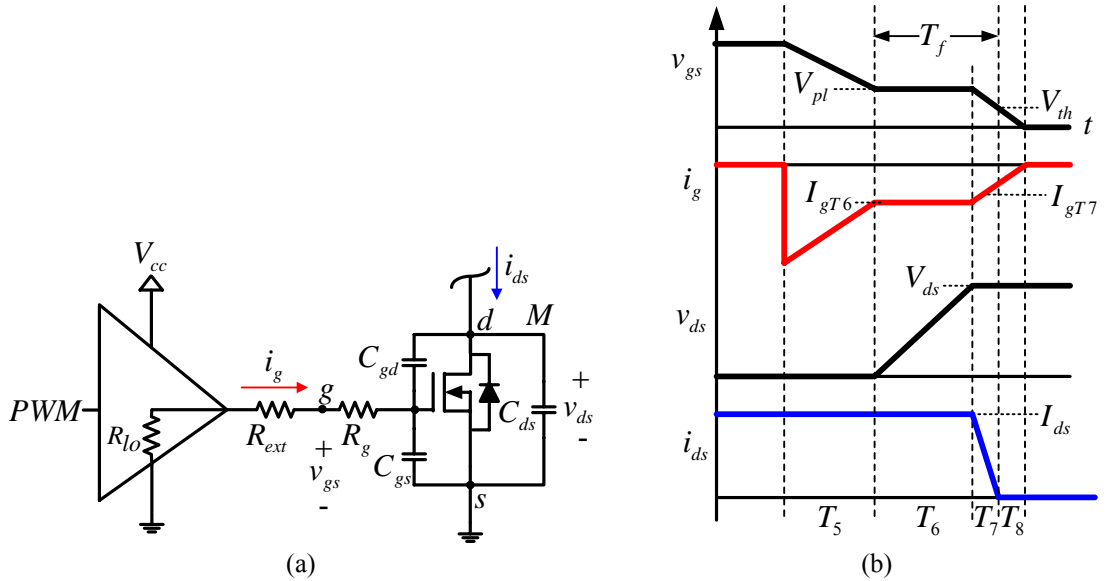


Figure 2.15 Power MOSFET turn off model proposed in [19]; (a) circuit and (b) waveforms

The average gate drive currents during T_6 and T_7 , I_{gT6} and I_{gT7} , are given by (2.14) and (2.15).

$$I_{gT6} = \left| \frac{-V_{pl}}{R_{lo} + R_{ext} + R_g} \right| \quad (2.14)$$

$$I_{gT7} = \left| \frac{-0.5(V_{pl} + V_{th})}{R_{lo} + R_{ext} + R_g} \right| \quad (2.15)$$

Assuming that I_{gT6} is the charge current of the C_{gd} capacitor while the drain voltage changes from 0V to V_{ds} and I_{gT7} discharges the input capacitors of the MOSFET from V_{pl} to V_{th} , the approximate switching times are given by (2.16) and (2.17). The fall time, T_f is the sum of T_6 and T_7 as given in (2.18).

$$T_6 = C_{gd} \frac{V_{ds}}{I_{gT6}} \quad (2.16)$$

$$T_7 = (C_{gs} + C_{gd}) \frac{V_{pl} - V_{th}}{I_{gT7}} \quad (2.17)$$

$$T_f = T_6 + T_7 \quad (2.18)$$

During T_6 , the drain voltage is rising from 0V to V_{ds} . During T_7 , the drain voltage is 0V and the current is ramping from the load current, I_{ds} to 0A. Using linear approximations of the waveforms, the power loss components for the respective intervals are estimated by (2.19) and (2.20), where T_s is the switching period. The total turn on switching loss is the sum of the two components, yielding (2.21).

$$P_6 = \frac{T_6}{T_s} \frac{V_{ds}}{2} I_{ds} \quad (2.19)$$

$$P_7 = \frac{T_7}{T_s} V_{ds} \frac{I_{ds}}{2} \quad (2.20)$$

$$P_{off} = \frac{1}{2} V_{ds} I_{ds} T_f f_s \quad (2.21)$$

The total switching loss, using the conventional model is the sum of the turn on loss, P_{on} and turn off loss, P_{off} and is given by (2.22) as P_{sw} .

$$P_{sw} = \frac{1}{2} V_{ds} I_{ds} (T_r + T_f) f_s \quad (2.22)$$

The conventional model enables simple and rapid estimation of switching loss, however, the main drawback is that it neglects the switching loss dependences due to common source inductance and other circuit inductances. Typically, this model predicts that turn on and turn off

loss are nearly equal. However, in a real converter operating at a high switching frequency, the model is highly inaccurate since turn off loss is much greater than turn on loss.

A comprehensive analytical model is presented in [20]. An extension of this model is presented in [21], which includes ringing loss and characterization of the non-linear capacitances C_{gs} , C_{gd} and C_{ds} . The basic idea of these models is to solve the equivalent circuit illustrated in Figure 2.16 during turn on (R_{lo} open circuit) and turn off (R_{hi} open circuit) to derive the current and voltage equations of the power MOSFET during switching transitions. The advantage of these models is that they provide accurate characterization of switching loss when common source, L_s , and drain, L_d , inductances are included. The main drawback of these models is their complexity due to the high order differential equations required to obtain the model solution.

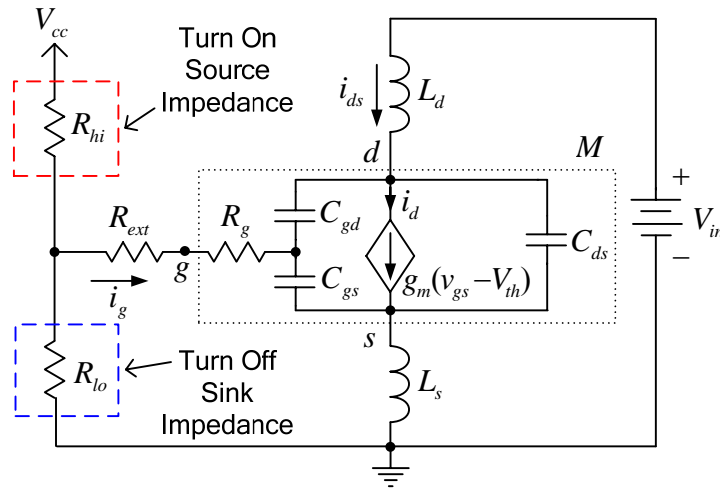


Figure 2.16 Equivalent switching transition circuit used in switching loss models [20] and [21]

To solve the complexity problem of the models in [20] and [21] while maintaining the main benefit of simplicity in the conventional model of [19], a new piecewise linear switching loss model is presented in Chapter 5 for synchronous buck converters. The proposed model includes the common source inductance and other parasitic inductances to enable simple and accurate switching loss calculations.

2.6 Review of DC-DC Converter Analog Control Techniques

Converter systems invariably require constant output voltages regardless of changes in the input voltage, or load current. The only way the output voltage can be kept constant is through the use of feedback. Feedback circuits must vary the converter control input, i.e. the pulse width, or the switching frequency, such that the output voltage is regulated to track a desired reference voltage. In addition, converters must be stable and achieve a good dynamic response.

In low power DC-DC applications, two types of converters are used: PWM converters and resonant converters. PWM converters are controlled by varying the pulse width of the gating signals of the primary side switches. Resonant converters are most commonly controlled by varying the switching frequency of the primary side switches. Resonant converters operate with a tuned filter to ideally allow only the fundamental switching frequency component to pass. The converter output is then controlled by varying the switching frequency near the resonant frequency, which varies the impedance of the resonant tank.

This section will briefly review the most common conventional analog PWM and resonant control methods for DC-DC converters, with the objective of analyzing their suitability for future high switching frequency applications operating at 10MHz.

2.6.1 PWM Converter Analog Control Techniques

There are three common types of PWM converter control techniques: 1) duty cycle control, 2) asymmetrical control, and 3) phase shift control. These techniques are discussed in the following sub-sections.

2.6.1.1 Duty Cycle Control

Duty cycle control is used in simple non-isolated PWM converters such as the buck and boost converters. It is also used for single switch isolated converters including the forward and

flyback converters. In these techniques, the duty cycle of the control switch controls the output voltage. Since most converters controlled by duty cycle control are hard-switched, they are not suitable for future very high switching frequency converters in the MHz range.

2.6.1.2 Asymmetrical Control

The asymmetrical control technique [28]-[30] has been proposed to reduce switching loss in half-bridge converters. In this control technique, the output voltage is controlled by varying the duty cycle of one switch, while the other switch conducts during the remainder of the switching period. Since this technique does not guarantee lossless switching for both switches for most line and load conditions, it is also not suitable for future very high switching converters.

2.6.1.3 Phase Shift Control

In the late 1980s, the phase shift control technique, illustrated in Figure 2.17, was proposed to reduce, or eliminate the primary side turn on switching losses [31]-[34]. The full-bridge converter utilizing this control technique is commonly referred to as the Phase Shift Full-Bridge (PSFB).

In the phase shift control technique, each switch conducts for 180 degrees and the right bridge leg is phase shifted with respect to the left bridge leg. This control technique is not considered a conventional PWM technique by some since the pulse width of the control switches are not controlled. Instead, the phase shifting of the bridge legs yields a variable pulse width voltage at the transformer primary as shown by v_p in Figure 2.17. When this control technique is used for PWM type converters, one of the bridge legs tends to lose ZVS, so switching losses can be very high as switching frequencies approach the MHz range. For this reason, this technique is also not suitable for next generation very high switching frequency converters.

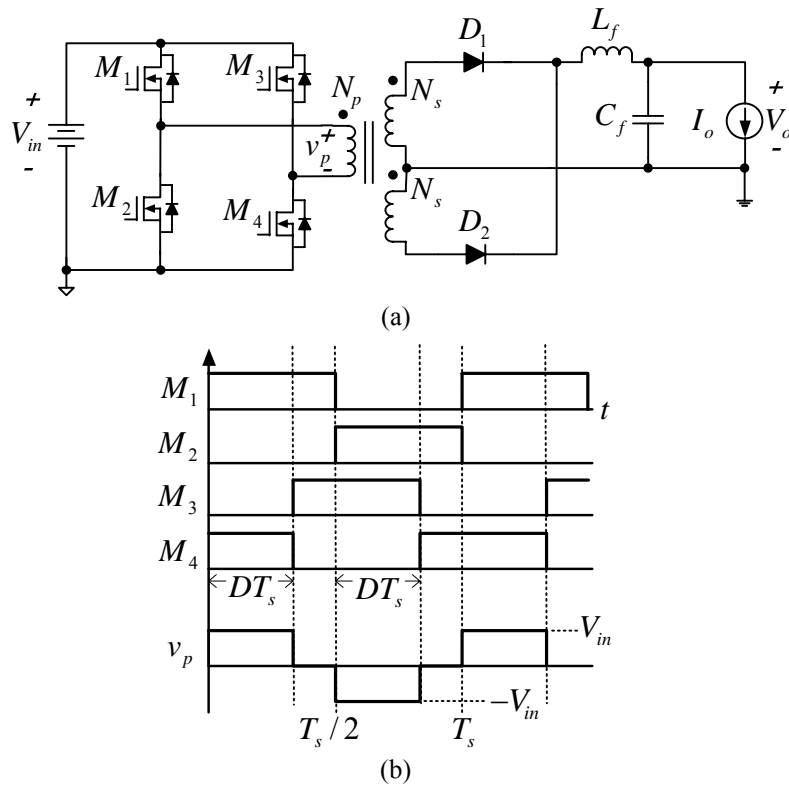


Figure 2.17 (a) Phase shift full-bridge converter and (b) its associated waveforms

2.6.2 Resonant Converter Analog Control Techniques

Traditionally, resonant converters have been controlled by varying the switching frequency near the resonant frequency, so that the impedance of the resonant tank varies to allow a variable portion of the fundamental frequency only to pass to the output rectifier and filter. However, more recently, constant frequency control techniques have been proposed for resonant converters, including the asymmetrical and phase shift techniques. These two techniques are briefly reviewed in the following sub-sections. The techniques themselves are generally suitable for 10MHz switching frequency operation, however implementation of a low cost comparator in the controller integrated circuit is a problem.

2.6.2.1 Variable Frequency Control

Analog variable frequency controllers are not very common since variable frequency control has not been widely used for at least the last fifteen years. The block diagram of a simple variable frequency controller is illustrated in Figure 2.18. The output voltage is compared to a reference and the difference error voltage is amplified using a compensator. The output of the compensator is a predominately DC signal which feeds a voltage controlled oscillator (VCO) which generates the PWM signal.

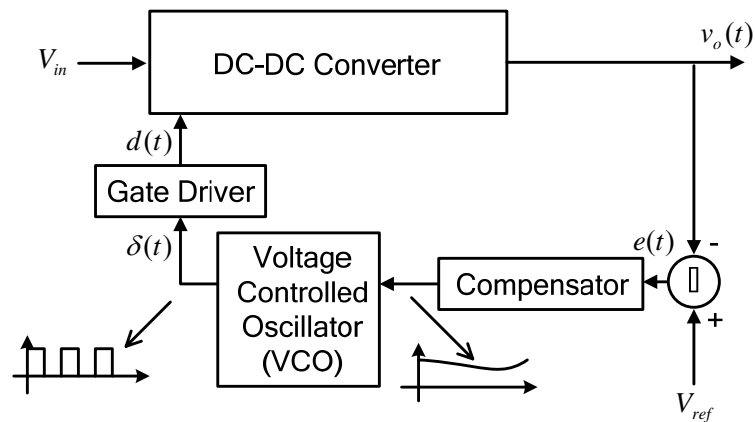


Figure 2.18 Variable frequency control block diagram

Variable frequency constant on-time, or constant off-time controllers have been proposed with oscillator frequencies approaching 10MHz [35].

2.6.2.2 Asymmetrical Control and Phase Shift Control

The asymmetrical and phase shift control techniques have been proposed to allow half-bridge and full-bridge resonant converters to operate at constant switching frequency with ideally no turn on switching loss [22]-[24]. Since these techniques allow resonant converters to be controlled with very low switching loss, depending on the pulse width generation method used, they can be suitable for next generation very high switching frequency converters.

2.6.3 Additional Drawbacks of Conventional Analog Control Techniques

As power systems become more advanced, end users are demanding a greater variety of features for advanced power management. The most significant drawback for future high frequency switching at 10MHz is the implementation of a low cost comparator in the controller integrated circuit. In addition, conventional analog control techniques do not easily interface with other systems, so achieving advanced integration of system components is a problem. Furthermore, the availability of control algorithms is quite limited (i.e. the choices of control algorithms are essentially limited to the four basic algorithms given in this sub-section). Other drawbacks of analog control techniques include relatively high sensitivity to parameter and process variations, high component counts and the lack of ability to make low cost and rapid changes to the controllers.

2.6.4 Summary of Analog Control Techniques

A tree diagram is presented in Figure 2.19 in order to summarize the applicability of control techniques summarized in the preceding sections.

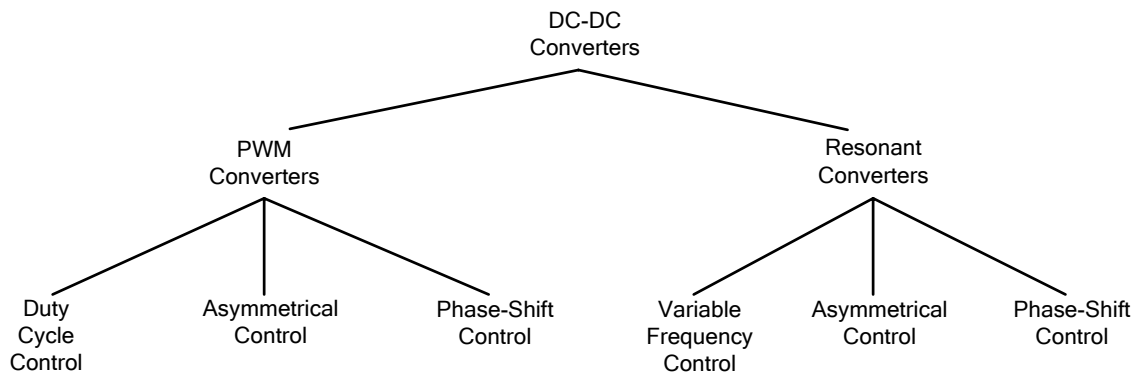


Figure 2.19 Tree diagram summarizing applicability of analog control techniques for DC-DC converters

2.7 Review of DC-DC Converter Digital Control Techniques

Since the late 1990s, there has been rapid growth in interest of applying digital control

techniques for switching power converters. Numerous papers have been published, including [36]-[43], touting the benefits of digital control techniques. In general, these benefits solve all of the problems of analog control mentioned in section 2.6.3.

Digital implementation of control techniques promise digital integration for advanced power management features. In addition, other benefits include programmable compensation and protection which can reduce, or eliminate passive components. Another advantage is decreased sensitivity to process and parameter variations. However, arguably most importantly, digital implementation allows for the use of a wide variety of sophisticated and non-linear control techniques.

To date, the adoption rate of digital control techniques in DC-DC converters has been low for various reasons including, cost versus benefit, ease of use and the lack of availability of low cost DSPs (Digital Signal Processors) and ASICs (Application Specific Integrated Circuits) that can match the performance of conventional analog techniques.

For future high frequency applications approaching 10MHz switching frequency, there is a more fundamental technical barrier which is widely known as the resolution problem, which is explained as follows. For Buck derived converters, for a given required resolution in the output voltage, ΔV_o , the number of bits required for the analog to digital converter (ADC), N_{ADC} , is given by (2.23), where V_{in} is the input voltage of the converter and ΔD is the change in duty cycle.

$$N_{ADC} = \log_2\left(\frac{1}{\Delta D}\right) = \log_2\left(\frac{V_{in}}{\Delta V_o}\right) \quad (2.23)$$

In order to avoid a phenomenon known as limit cycle oscillation [41], the number of bits required for the digital PWM generator, discrete PWM (DPWM), is at least one bit greater than the ADC, so N_{DPWM} is given by (2.24).

$$N_{DPWM} = N_{ADC} + 1 \quad (2.24)$$

Therefore, in order to achieve the desired output voltage resolution, the clock frequency requirement, f_{clock} , is given by (2.25).

$$f_{clock} = 2^{N_{DPWM}} f_S \quad (2.25)$$

Alternatively to achieve the required resolution, the number of stages, N_{stages} , required for a ring oscillator implementation is given by (2.26).

$$N_{stages} = 2^{N_{DPWM}} \quad (2.26)$$

The problem with the clock frequency implementation is that power consumption in the digital controller increases proportional to frequency. The problem with the ring oscillator implementation is that an excessive number of stages is required, which occupies a significant portion of the die area.

As an example, for a 12V/1V voltage regulator (VR) application for a computer, in order to achieve 10mV resolution at 10MHz switching frequency, a 9-bit ADC would be required. This leads to the requirement of a 10-bit DPWM and therefore, a controller with a 10.24GHz switching frequency, which is more than three times higher than the most advanced PC processors. This is of course impractical for low cost power supplies.

2.7.1 PWM Dithering

In order to solve the problem of the requirement of high clock frequencies, the PWM dithering method has been proposed [41]. This concept is illustrated in Figure 2.20, where 2-bit dither is implemented by dithering (averaging) the least significant bit (LSB) over four switching periods. In Figure 2.20, D_{C1} represents the steady-state duty cycle and D_{C2} represents D_{C1} plus one LSB of dither.

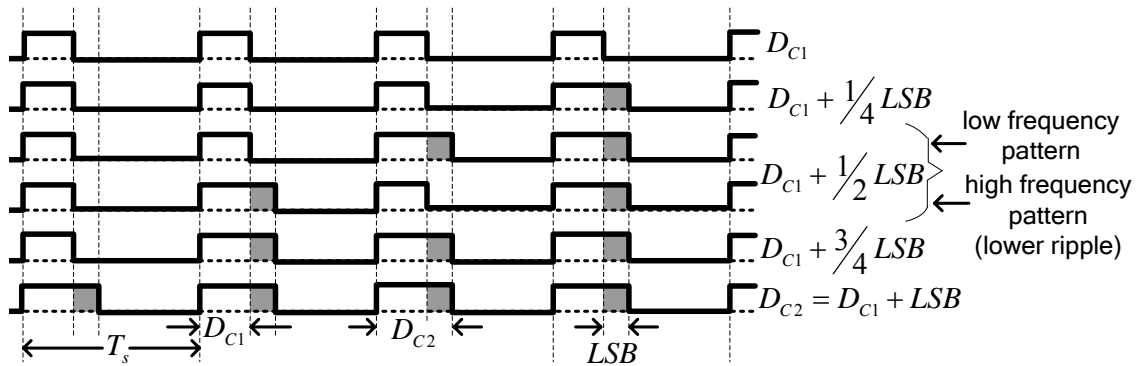


Figure 2.20 Switching waveform dither patterns realizing (1/4)LSB, (1/2)LSB, and (3/4)LSB DPWM levels (2-bit dither)

In general, by using dither patterns spanning 2^X switching periods, the effective DPWM resolution can be increased by X -bits as given by (2.27), where N_{DPWM} is the hardware resolution and $N_{DPWMeff}$ is the effective DPWM resolution. The result is a corresponding decrease in the required switching frequency by a factor of 2^X .

$$N_{DPWMeff} = N_{DPWM} + X \quad (2.27)$$

The problem with the dither method for a 10MHz application is that it still cannot reduce the clock frequency to realistic levels below 500MHz. For example, with 3-bit dither, the required clock frequency for the example given in the previous sub-section is 1.28GHz. It is also worth noting that achieving ZVS to enable even moderate efficiencies above 80% can be very difficult with PWM control since most soft-switching PWM converters lose ZVS at light load and/or high line conditions, so it can be argued that the types of converters that would use PWM dithering cannot be used at 10MHz to begin with, even before any discussion of control.

2.8 Conclusions

Present day low power DC-DC switching converters operate in the 300-500kHz switching frequency range. The trend is to increase this into the MHz range in the near future. However, increased switching frequencies lead to increased frequency dependent losses, particularly

switching loss and gate driving loss. These two loss components are related to the gate drive circuitry. Traditionally, conventional voltage source drivers have been used, however resonant gate drive techniques have been proposed [4]-[18]. These circuits have been proposed in order to only recover gate energy and not reduce switching loss. In addition, each circuit has other technical barriers preventing wide spread adoption, the most common being the requirement of a large inductor, or transformer. To solve the problems inherent to conventional drivers and existing resonant drivers and to reduce switching loss, new current source gate drive circuits are proposed in Chapters 3 and 4.

In order to optimally design high switching frequency DC-DC converters, engineers begin their design by estimating the losses in a design file. Device data sheet values and analytical models are used to calculate the losses. The conventional switching loss model [19] is widely used in the power electronics field. This model is very simple to use, however the accuracy of its switching loss predictions degrades at high switching frequencies since it neglects common source inductance. Comprehensive switching loss models proposed in [20] and [21] provide complex mathematical solutions to model switching loss, however closed form solutions are not achievable. To solve the complexity problem of the models in [20] and [21] while maintaining the main benefit of simplicity in the conventional model of [19], a new piecewise linear switching loss model is presented in Chapter 5 for the synchronous buck converter.

The most common conventional analog control methods for DC-DC converters have been reviewed with the objective of analyzing their suitability for future high switching frequency applications operating at 10MHz. The fundamental problem with conventional analog control methods for future high frequency converters operating at 10MHz is the requirement of a low cost very fast comparator to minimize delay in the control circuit. In addition, there are other drawbacks of analog implementation including poor adaptability, programmability and sensitivity

to process and parameter variations. Digital control implementation promises to solve these problems; however, the problem with high frequency digital implementation is the requirement of very high clock frequencies to achieve the required output voltage resolution. In order to solve these problems, a new digital control algorithm is proposed in chapter 6.

Chapter 3

A Current Source Gate Driver Achieving Switching Loss Reduction and Gate Energy Recovery at 1MHz[†]

3.1 Introduction

In recent years there has been a trend to increase the switching frequency beyond 1MHz in low voltage high current DC-DC power supplies. The objectives of this trend are to increase the power density by decreasing the size of passive components and to improve the dynamic performance. Furthermore, it is well understood that as switching frequency increases, both switching loss and gate loss increase.

In the past two decades, much work has been done on reducing, or eliminating turn on switching loss through soft switching techniques. However, in general, these techniques require additional components and require snubber capacitors to reduce turn off loss. Unfortunately, adding snubber capacitors to reduce turn off loss, makes achieving zero voltage switching (ZVS) at turn on more challenging for all line and load conditions. Furthermore, these techniques do not reduce gate loss. Therefore, with some improvements achieved through reduction in turn on switching loss, it is now essential to focus some effort on reducing turn off switching loss and gate loss in order to continue to achieve greater power density and dynamic performance.

This chapter proposes a new current source gate driver for ground referenced power MOSFETs. The proposed driver aims to reduce switching loss by providing a near constant gate charging and discharging currents to switch quickly. Furthermore, the driver can recover a

[†] The content of this chapter is subject to patent pending for U.S. patent number US 2006/0170043 A1, International patent number WO 2006/079219 A1 and is in press in the following journals:

[1] W. Eberle, Z. Zhang, Y.F. Liu and P.C. Sen, "A Current Source Gate Driver Achieving Switching Loss Savings and Gate Energy Recovery at 1-MHz," IEEE Trans. Power Electron., TPEL-2007-05-0257.

[2] W. Eberle, Y.F. Liu and P.C. Sen, "A Novel High Efficiency Resonant Gate Driver with Efficient Energy Recovery and Low Circulating Current" IEEE Trans Industrial Electron., TIE00485-2005.

portion of the QV gate energy otherwise lost in conventional voltage source drivers.

In section 3.2, the proposed current source driver circuit and operation are presented. The potential benefit of power converter switching loss reduction using current source drive is summarized in section 3.3. A detailed analysis of the driver loss mechanisms is presented in section 3.4 followed by a design procedure in section 3.5. A design example is presented in section 3.6. The logic circuit used to generate the driver gating waveforms is presented in section 3.7. Experimental results are provided in section 3.8. An alternate 3-pulse version of the proposed driver is presented in section 3.9 and the conclusions are presented in section 3.10.

3.2 Proposed Current Source Gate Driver

The following sub-sections present the proposed circuit and operation.

3.2.1 Proposed Circuit

The proposed current source gate driver is illustrated in Figure 3.1. It consists of four controlled switches, S_1 - S_4 (S_1, S_2 p-channel and S_3, S_4 n-channel) including their body diodes, D_1 - D_4 , and a small inductance, L . The switches are controlled and diodes are used to allow the inductor current to be discontinuous and allow the power MOSFET to turn on or off beginning from a non-zero pre-charge current. Following charging, or discharging of the power MOSFET, the excess energy stored in the inductor is allowed to return to the supply voltage, V_{cc} , thereby allowing the power MOSFET gate charge energy to be recovered.

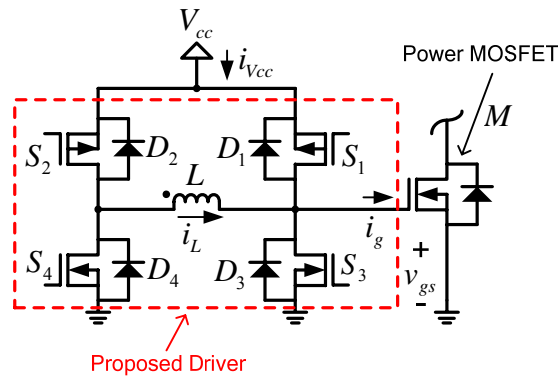


Figure 3.1 Proposed current source gate drive circuit

The gating waveforms of the four driver switches, S_1 - S_4 , along with the inductor current, gate current, power MOSFET gate-to-source voltage and the line current are illustrated in Figure 3.2. The key waveforms to note are: 1) the inductor current, labeled i_L , which is discontinuous to minimize conduction loss, 2) the gate drive current, labeled i_g , which remains approximately constant (in comparison to the conventional voltage source drivers), and 3) the line current, $i_{V_{cc}}$, which contains negative intervals, indicating that energy is returned to the line. The operation of the circuit is explained in the following paragraphs.

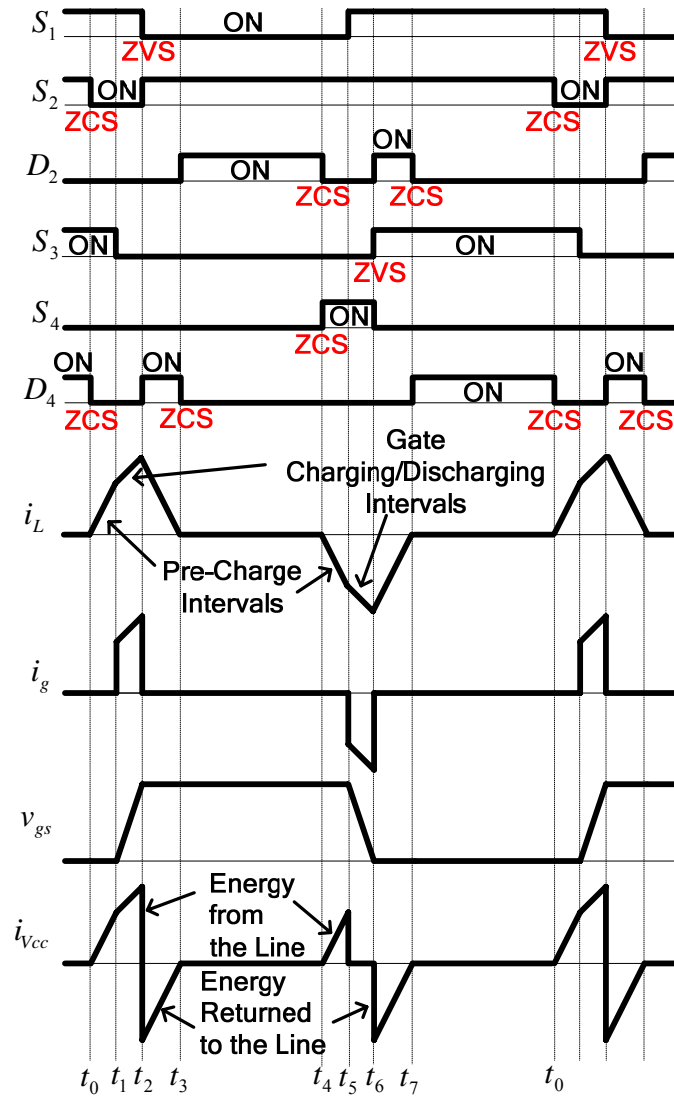


Figure 3.2 Waveforms of the proposed current source gate driver

3.2.2 Detailed Operation at Turn On

Initially it is assumed that the power MOSFET is in the off state before time t_0 . Initially, before t_0 , only switch S_3 and D_4 are on and the gate of M is clamped to zero volts. The current paths during the intervals of the turn-on stage are illustrated in Figure 3.3 to Figure 3.6. It is noted that M has been replaced by its equivalent total gate capacitance, C_g .

t_0 - t_1 : At t_0 , S_2 turns on (with ZCS), therefore turning off D_4 by commutation (with ZCS) and

allowing the inductor current to ramp up as illustrated in Figure 3.3. The current path during this interval is S_2 - L - S_3 . Since S_3 is in the on state, the gate of M is clamped low. This interval is the inductor current pre-charge interval and it ends at time t_1 , which is a pre-determined time set by the user.

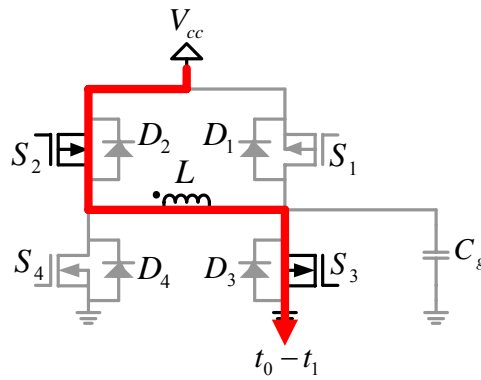


Figure 3.3 Current path during turn-on inductor pre-charge interval

t_1 - t_2 : At t_1 , S_3 is turned off, which allows the inductor current to begin to charge the power MOSFET gate as illustrated in Figure 3.4. Assuming a low natural resonant frequency for L - C_g , the inductor current continues to ramp up from the pre-charged level as the voltage across the gate capacitance increases. The current path during this interval is S_2 - L - C_g . This interval ends at t_2 , when v_{gs} reaches V_{cc} . If the inductor pre-charge current at the end of t_1 is much greater than the ripple amplitude during this interval, then the inductor can be assumed to be a current source charging the power MOSFET gate.

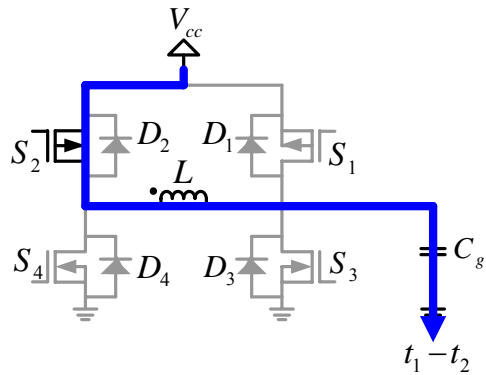


Figure 3.4 Current path during turn-on gate charging interval

t_2-t_3 : At t_2 , S_1 is turned on (with ZVS) and S_2 is turned off, therefore driving D_4 on to allow the inductor current to continue to conduct into the dot through the path D_4-L-D_1 as illustrated in Figure 3.5. Most importantly, during this interval the stored energy in the inductor is returned to the line. This can be observed from the negative portion of the $i_{V_{cc}}$ curve in Figure 3.2. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. During this interval, the gate voltage of M remains clamped to the line voltage, V_{cc} . The interval ends when the inductor current reaches zero at t_3 .

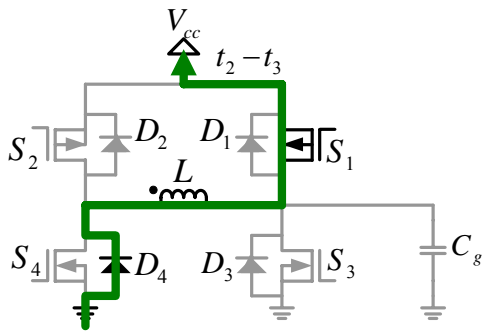


Figure 3.5 Current path during turn-on energy return interval

t_3-t_4 : At t_3 , D_4 turns off (with ZCS) and the equivalent circuit is illustrated in Figure 3.6. During this interval, the gate voltage of M remains clamped to V_{cc} . The interval ends at t_4 when the pre-charging interval for the turn off cycle begins as dictated by the PWM signal.

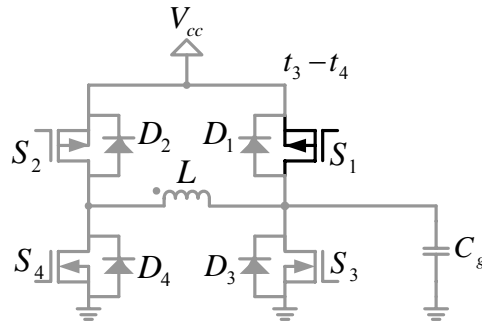


Figure 3.6 Clamping interval when the power MOSFET is on

3.2.3 Detailed Operation at Turn Off

The turn off interval begins at the end of t_4 . Initially, the inductor current is zero and S_1 is on. The current paths during the intervals of the turn off stage are illustrated in Figure 3.7 to Figure 3.10.

t_4-t_5 : At t_4 , the turn off inductor pre-charging interval begins as illustrated in Figure 3.7. S_4 is turned on (with ZCS) therefore turning off D_2 by commutation (with ZCS). Since S_1 was previously on, the inductor current begins to ramp negative out of the dot through the path S_1 - L - S_4 . During this interval, the gate voltage of M remains clamped to V_{cc} . The interval ends at t_5 .

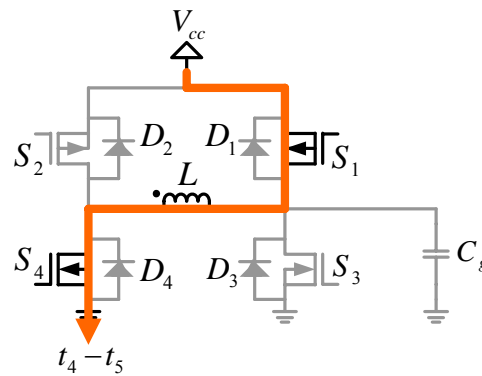


Figure 3.7 Current path during turn off inductor pre-charge interval

t_5-t_6 : At t_5 , S_1 is turned off, which allows the inductor current to begin to discharge the power MOSFET gate as illustrated in Figure 3.8. Assuming a low natural resonant frequency of L - C_g , the inductor current continues to ramp negative from the pre-charged level as the voltage

across the gate capacitance decreases. The current path during this interval is C_g-L-S_4 , where C_g represents the equivalent gate capacitance of M . This interval ends at t_6 , when v_{gs} reaches zero. If the inductor pre-charge current at the end of t_5 is much greater than the ripple amplitude during this interval, then the inductor can be assumed to be a current source discharging the power MOSFET gate.

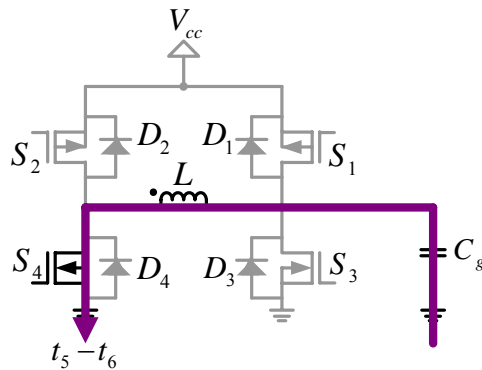


Figure 3.8 Current path during turn off gate discharging interval

t_6-t_7 : At t_6 , S_3 is turned on (with ZVS) and S_4 is turned off, therefore driving D_2 on to allow the inductor current to conduct out of the dot through the path D_3-L-D_2 as illustrated in Figure 2.5. Most importantly, during this interval the gate discharging energy is returned to V_{cc} . This can be observed from the negative portion of the $i_{V_{cc}}$ curve in Figure 3.9. Also, during this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down positive towards zero. During this interval, the gate voltage of M remains clamped to ground. The interval ends when the inductor current reaches zero at t_7 .

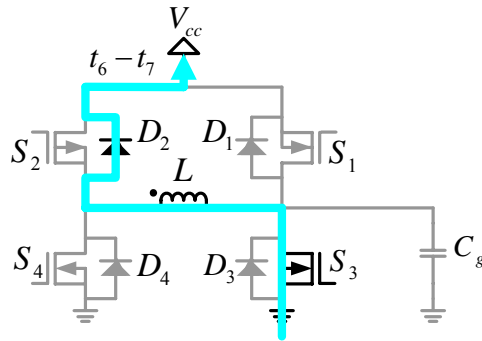


Figure 3.9 Current path during turn off energy return interval

t_7-t_0 : At t_7 , D_2 turns off (with ZCS) and the equivalent circuit is illustrated in Figure 3.10. During this interval, the gate voltage of M remains clamped to ground. The interval ends at t_0 when the pre-charging interval for the turn on cycle begins and the entire process repeats as dictated by the PWM signal.

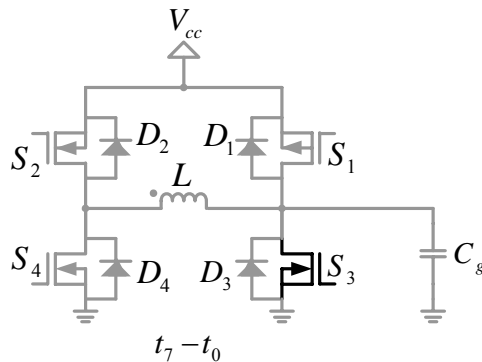


Figure 3.10 Clamping interval when the power MOSFET is off

There are several benefits of the proposed current source driver:

- 1) It behaves as a current source, which enables quick switching and reduced switching loss as shown in section 3.3.
- 2) The driver inductance is very small as shown in sections 3.5 and 3.6.
- 3) The driver has the potential to recover gate energy as shown in sections 3.2 and 3.8.
- 4) The peak current is independent of duty cycle and frequency, so it is suitable for different

types of control and wide operating conditions as shown in section 3.8.

- 5) The inductor current is discontinuous, minimizing circulating current, so conduction losses in the driver are minimized as shown in sections 3.2 and 3.8.
- 6) The driver switches operate with soft switching as shown in section 3.2.

3.3 Switching Loss Reduction

The potential for gate loss energy recovery was presented in the previous section. This section elaborates on the potential for switching loss energy reduction by faster switching with a current source driver. In hard switched converters, the actual potential total switching loss reduction can be much more significant than the gate loss savings. This statement can hold true for most soft switching converters, since ZVS converters typically only eliminate turn on loss, or with the addition of snubber capacitors, they are not able to maintain ZVS across varying line and load conditions.

In hard switching converters, neglecting any body diode reverse recovery and drain and common source inductance, the turn on switching loss can be approximated by (3.1), and the turn off switching loss by (3.2), where V_{ds} represents the voltage across the switch. In (3.1), I_{on} , represents the current through the switch at turn on and T_r represents the rise time. In (3.2), I_{off} represents the current through the switch at turn off and T_f represents the fall time. Since both T_r and T_f are both inversely proportional to the average gate current (during the switching interval), I_g , it is clear that switching losses can be reduced by increasing gate current. However, in conventional gate drivers, this is generally not possible since the peak current is already limited by the current handling capability of the driver switches.

$$P_{on} = \frac{1}{2} f_s V_{ds} I_{on} T_r \quad (3.1)$$

$$P_{off} = \frac{1}{2} f_s V_{ds} I_{off} T_f \quad (3.2)$$

In the conventional driver, the gate current decays significantly from its peak value due to the RC type charging and discharging. On the other hand, the proposed current source gate driver behaves like a nearly constant current source and the gate current actually increases slightly during the rise and fall times as illustrated in Figure 3.11 where it is clear that the magnitude of i_g is greater than I_{pl_on} and I_{pl_off} , respectively. The result is that the turn on and turn off times decrease significantly and more importantly, the rise and fall times decrease significantly, which reduces switching loss.

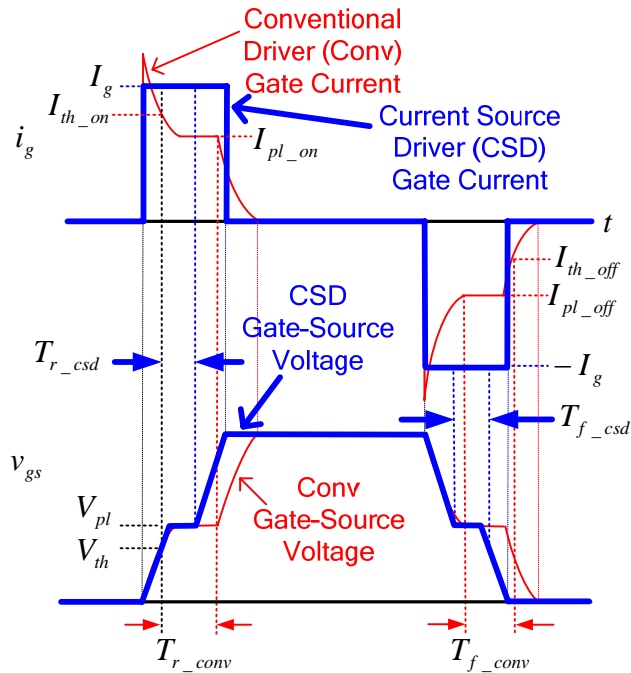


Figure 3.11 Comparison between the gate current waveform shapes for the conventional driver and an ideal current source driver

Using the conventional switching loss model [19], for a conventional voltage source gate driver, the turn on switching loss, P_{on_conv} , is given by (3.3), where T_{r_conv} is given by (3.4), I_{on} represents the current through the MOSFET at turn on and V_{ds} represents the voltage across the switch before turn on. In (3.4), I_{th_on} represents the gate current when the gate voltage is at the

threshold and is given by (3.5). Also in (3.4), I_{pl_on} represents the gate current when the gate voltage is at the plateau and is given by (3.6). Other parameters noted include the power MOSFET total gate charge at the beginning of the plateau, Q_{pl} , the total gate charge at the threshold, Q_{th} , the gate-to-drain charge, Q_{gd} , the source impedance of the driver, R_{hi} , the MOSFET internal gate resistance, R_g , the MOSFET plateau voltage, V_{pl} , the MOSFET threshold voltage V_{th} and the external gate resistance in the drive circuit, R_{ext} .

$$P_{on_conv} = \frac{1}{2} V_{ds} I_{on} T_{r_conv} f_s \quad (3.3)$$

$$T_{r_conv} = \frac{Q_{pl} - Q_{th}}{\frac{1}{2}(I_{th_on} + I_{pl_on})} + \frac{Q_{gd}}{I_{pl_on}} \quad (3.4)$$

$$I_{th_on} = \frac{V_{cc} - V_{th}}{R_{hi} + R_{ext} + R_g} \quad (3.5)$$

$$I_{pl_on} = \frac{V_{cc} - V_{pl}}{R_{lo} + R_{ext} + R_g} \quad (3.6)$$

For a conventional gate driver, the turn off switching loss, P_{off_conv} , is given by (3.7), where T_{f_conv} represents the fall time as given by (3.8), I_{off} represents the current through the MOSFET at turn off and V_{ds} represents the MOSFET voltage stress in the off state. In (3.8), I_{pl_off} represents the gate current when the gate voltage is at the plateau and is given by (3.9) and I_{th_off} represents the gate current when the gate voltage is at the threshold, as given by (3.10). In (3.9) and (3.10), R_{lo} represents the sink impedance of the driver.

$$P_{off_conv} = \frac{1}{2} V_o I_{off} T_{f_conv} f_s \quad (3.7)$$

$$T_{f_conv} = \frac{Q_{pl} - Q_{th}}{\frac{1}{2}|I_{th_off} + I_{pl_off}|} + \frac{Q_{gd}}{|I_{pl_off}|} \quad (3.8)$$

$$I_{pl_off} = \frac{V_{pl}}{R_{lo} + R_{ext} + R_g} \quad (3.9)$$

$$I_{th_off} = \frac{V_{th}}{R_{lo} + R_{ext} + R_g} \quad (3.10)$$

With an ideal current source driver with constant gate current, the turn on switching loss, P_{on_csd} , is given by (3.11), where T_{f_csd} , is given by (3.12).

$$P_{on_csd} = \frac{1}{2} f_s V_{ds} I_{onpk} \frac{Q_{pl} - Q_{th} + Q_{gd}}{I_g} \quad (3.11)$$

$$T_{r_csd} = \frac{Q_{pl} - Q_{th} + Q_{gd}}{I_g} \quad (3.12)$$

With an ideal current source driver with constant gate current, the turn on switching loss, P_{off_csd} , is given by (3.13), where T_{f_csd} , is given by (3.14).

$$P_{off_csd} = \frac{1}{2} V_{ds} I_{off} f_s T_{f_csd} \quad (3.13)$$

$$T_{f_csd} = \frac{Q_{pl} - Q_{th} + Q_{gd}}{|I_g|} \quad (3.14)$$

To demonstrate the potential switching loss reduction with a current source driver, a boost converter example is used. The boost circuit is illustrated in Figure 3.12. Circuit parameters are listed in Table 3.1.

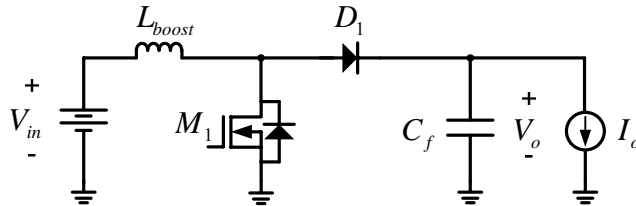


Figure 3.12 Boost converter circuit used in simulation

Table 3.1 Circuit parameters for switching loss calculation comparison

Boost Topology Parameters	
Input Voltage, V_{in}	5V
Output Voltage, V_o	10V
Load Current, I_o	5A
Inductor, L_{boost}	1 μ H
Output Capacitor, C_f	60 μ F
Gate Drive Voltage, V_{cc}	5V
MOSFET Turn On Current, I_{on}	10A
MOSFET Turn Off Current, I_{off}	12A
External Impedance, R_{ext}	1 Ω
Switching Frequency, f_s	1MHz
Diode, D_1	10TQ035
MOSFET, M_1	IRF6618
MOSFET Parameters	IRF6618
Q_{gd}	12nC
Q_{th}	8nC
Q_{pl}	15nC
V_{th}	1.64V
V_{pl}	3V
R_g	1 Ω
Conventional Driver	UCC37322
Source Impedance, R_{hi}	2.5 Ω
Sink Impedance, R_{lo}	1.1 Ω
Current Source Driver	
I_g	1.25A

Equations (3.3)–(3.14) are used to calculate the switching loss for the conventional driver and an ideal current source driver. To validate the results, the boost converter illustrated in Figure 3.12 was simulated with SIMetrix. Waveforms of the conventional driver are given in Figure 3.13 and for the current source driver are given in Figure 3.14. The results are summarized and a comparison is given in Table 3.2. P_{tot_sw} represents the sum of the turn on and turn off switching loss.

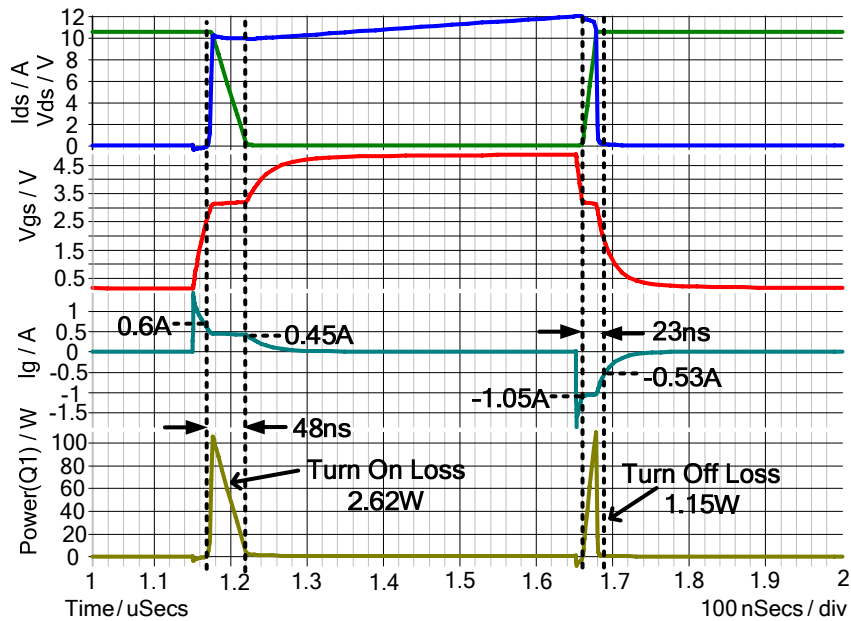


Figure 3.13 Boost converter MOSFET switching loss waveforms for the conventional driver; top: drain voltage and current, second: gate-source voltage, third: gate current, bottom: power loss

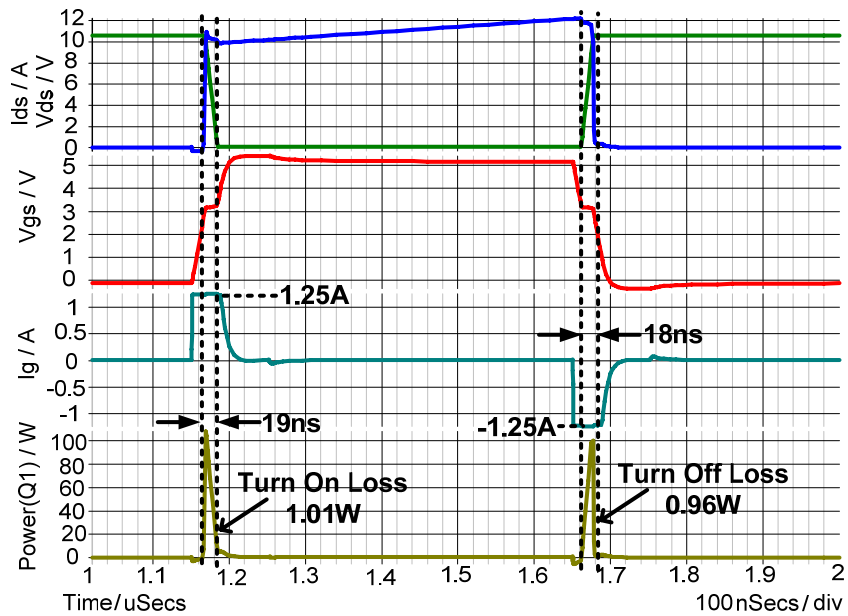


Figure 3.14 Boost converter MOSFET switching loss waveforms for the current source driver; top: drain voltage and current, second: gate-source voltage, third: gate current, bottom: power loss

Table 3.2 Circuit parameters for switching loss calculation comparison

	Conventional Driver (Conv) Calculated	Conventional Driver (Conv) Simulated	Current Source Driver (CSD) Calculated	Current Source Driver (CSD) Simulated	Switching Loss Reduction with CSD (Conv-CSD) Calculated	Switching Loss Reduction with CSD (Conv-CSD) Simulated
I_{th_on}	0.67A	0.60A	-	-	-	-
I_{pl_on}	0.44A	0.45A	-	-	-	-
I_{th_off}	-0.65A	-0.53A	-	-	-	-
I_{pl_off}	-0.97A	-1.05A	-	-	-	-
I_g	-	-	+/-1.25A	+/-1.25A	-	-
T_r	40ns	48ns	15ns	19ns	-	-
T_f	25ns	23ns	15ns	18ns	-	-
P_{on}	1.98W	2.62W	0.76W	1.01W	0.83W	1.05W
P_{off}	1.56W	1.15W	0.95W	0.96W	0.46W	0.22W
P_{tot_sw}	3.54W	3.77W	1.71W	1.97W	1.83W	1.8W

The results in Table 3.2 demonstrate that a current source driver can reduce switching loss significantly. There is also good agreement between the theoretical calculated results and the simulated results. In the example given, the rise time is reduced from 48ns to 19ns and the fall time is reduced from 23ns to 18ns. The turn on loss is reduced by 1.05W (from 2.62W to 1.01W) and the turn off loss is reduced by 0.22W (from 1.15W to 0.96W). Therefore, the total switching loss is reduced by 1.8W (from 3.77W to 1.97W) – a significant savings.

3.4 Driver Loss Analysis

The loss components of the proposed current source gate drive circuit are outlined in the following sub sections. The loss components include, conduction loss, gate drive loss in the driver switches, CV^2 output loss, turn off loss in the driver switches, core loss in the driver inductor, and loss in the driver logic circuit.

3.4.1 Driver Conduction Loss Calculation

The conduction loss can be determined by analyzing the losses during the three states of the turn on interval (t_0-t_3) and three states of the turn off interval (t_4-t_7) when the inductor current is

non-zero. The detailed inductor current waveform and power MOSFET gate voltage waveform are shown for the turn on interval in Figure 3.15. The analysis of the turn on intervals is explained as follows.

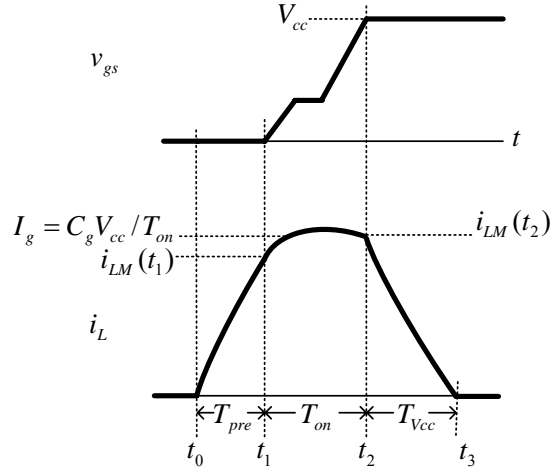


Figure 3.15 Power MOSFET gate-source voltage and current source driver inductor current waveforms during the turn on interval

It is assumed that the power MOSFET being driven, M , is represented by an RC network consisting of its parasitic series gate resistance, R_g , and an equivalent gate capacitance, C_g . During the on state, the control switches can be represented by series resistances R_1 - R_4 . The inductor copper loss can be represented by an equivalent series AC resistance, R_L .

The driver is designed to charge the gate-source voltage from zero to V_{cc} , during T_{on} by an average current source, I_g . Under this assumption, the turn on time, T_{on} , is given by (3.15), where Q_g represents the total gate charge of M .

$$T_{on} = \frac{Q_g}{I_g} \quad (3.15)$$

In the following sub-sections, the equivalent circuits during the pre-charge, turn on and energy return intervals are used and equations are derived to calculate the conduction loss in the proposed driver.

3.4.1.1 Pre-charge Interval

The interval from t_0 - t_1 is the inductor pre-charge interval, T_{pre} . During the pre-charge interval, switches S_2 and S_3 are on allowing the inductor current to ramp up into the dot. The equivalent circuit during T_{pre} is given in Figure 3.16, where R_2 , R_L and R_3 have been lumped together as R_{pre} (i.e. $R_{pre}=R_2+R_L+R_3$). The circuit is a voltage driven RL circuit with zero initial inductor current. The inductor current is given by (3.16), with the time constant, τ_{pre} , given by (3.17). The RMS current during the pre-charge interval is given by (3.18). Using (3.18), the power consumption, P_{pre} , during the interval is given by (3.39).

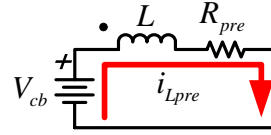


Figure 3.16 Equivalent circuit during the inductor pre-charge interval

$$i_{Lpre} = \frac{V_{cc}}{R_{pre}} (1 - e^{-t/\tau_{pre}}) \quad (3.16)$$

$$\tau_{pre} = \frac{L}{R_{pre}} \quad (3.17)$$

$$I_{preRMS} = \sqrt{f_s \int_0^{T_{pre}} i_{Lpre}^2 dt} \quad (3.18)$$

$$P_{pre} = R_{pre} f_s \int_0^{T_{pre}} i_{Lpre}^2 dt \quad (3.19)$$

3.4.1.2 Turn On Interval

t_1 - t_2 : The equivalent circuit during T_{on} is given in Figure 3.17. The circuit is a series RLC circuit consisting of R_2 , R_L , R_g , L and C_g , where R_2 , R_L and R_g have been lumped together as R_{on} (i.e. $R_{on}=R_2+R_L+R_g$). The inductor contains an initial current $i_L(t_1)$. In the s -domain, the KVL equation for the circuit is given by (3.20). Solving for the inductor current in the RLC circuit, the characteristic equation is of the form in (3.21) with poles at p_1 and p_2 as given in (3.22). The

parameters in (3.23) and (3.24) are the neper frequency, α and the resonant frequency ω_o .

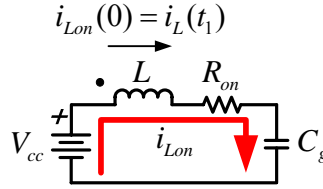


Figure 3.17 Equivalent circuit during the turn on interval

$$\frac{V_{cc}}{s} = sLI_L(s) - Li_L(t_1) + I_L(s)R_{on} + \frac{I_L(s)}{sC_g} \quad (3.20)$$

$$s^2 + \left(\frac{R_{on}}{L}\right)s + \left(\frac{1}{LC_g}\right) = (s + p_1)(s + p_2) \quad (3.21)$$

$$p_1 = -\frac{R_{on}}{2L} + \sqrt{\left(\frac{R_{on}}{2L}\right)^2 - \frac{1}{LC_g}} = -\alpha + \sqrt{\alpha^2 - \omega_o^2} \quad (3.22)$$

$$p_2 = -\frac{R_{on}}{2L} - \sqrt{\left(\frac{R_{on}}{2L}\right)^2 - \frac{1}{LC_g}} = -\alpha - \sqrt{\alpha^2 - \omega_o^2}$$

$$\alpha = \frac{R_{on}}{2L} \quad (3.23)$$

$$\omega_o = \frac{1}{\sqrt{LC_g}} \quad (3.24)$$

There are three possible solutions for the inductor current: over damped, critically damped and under damped. A driver designed with minimal conduction loss will be under damped with $R_{on} \rightarrow 0$ (R_{on} is typically 1Ω) and $\omega_o > \alpha$. The under damped solution for the inductor current is given by (3.25).

$$i_{Lon} = \left[\frac{V_{cc}}{L} - \alpha Li_L(t_1) \right] \frac{e^{-t\alpha}}{\sqrt{\omega_o^2 - \alpha^2}} \sin(\sqrt{\omega_o^2 - \alpha^2}t) + Li_L(t_1)e^{-t\alpha} \cos(\sqrt{\omega_o^2 - \alpha^2}t) \quad (3.25)$$

The RMS value of i_{Lon} is given by (3.26). Using (3.26), the conduction loss power, P_{on} , during T_{on} is given by (3.27).

$$I_{onRMS} = \sqrt{f_s \int_0^{T_{on}} i_{Lon}^2 dt} \quad (3.26)$$

$$P_{on} = R_{on} f_s \int_0^{T_{on}} i_{Lon}^2 dt \quad (3.27)$$

3.4.1.3 Energy Return Interval

t_2 - t_3 : The equivalent circuit during T_{Vcc} is given in Figure 3.18, where R_L and R_I have been lumped together as R_{Vcc} (i.e. $R_{Vcc}=R_I+R_L$). The diode voltage drop is considered constant at V_F . The inductor current is given by (3.28), with the time constant, τ_{Vcc} , given by (3.29).

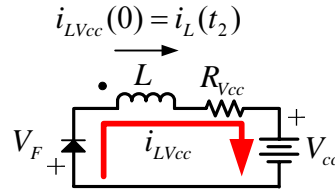


Figure 3.18 Equivalent circuit during the energy return interval

$$i_{LVcc} = \frac{-(V_{cc} + V_F)}{R_{Vcc}} + \left(i_L(t_2) + \frac{V_{cc} + V_F}{R_{Vcc}} \right) e^{-t/\tau_{Vcc}} \quad (3.28)$$

$$\tau_{Vcc} = \frac{L}{R_{Vcc}} \quad (3.29)$$

The RMS value of i_{LVcc} , I_{VccRMS} is given by (3.30). The average value of i_{LVcc} during T_{Vcc} over one period is given by (3.31). The conduction loss power, P_{Vcc} , during T_{Vcc} is given by (3.32).

$$I_{VccRMS} = \sqrt{f_s \int_0^{T_{Vcc}} i_{LVcc}^2 dt} \quad (3.30)$$

$$I_{VccAVG} = f_s \int_0^{T_{Vcc}} i_{LVcc} dt \quad (3.31)$$

$$P_{Vcc} = R_{Vcc} f_s \int_0^{T_{Vcc}} i_{LVcc}^2 dt + V_F f_s \int_0^{T_{Vcc}} i_{LVcc} dt \quad (3.32)$$

To calculate the total conduction loss, it can be assumed that the turn on and turn off states of operation are identical. Therefore, under this assumption, the total conduction loss in the proposed current source gate drive circuit is given by (3.33), which is two times the sum of P_{pre} ,

given by (3.19), plus P_{on} , given by (3.27), plus P_{Vcc} , given by (3.32).

$$P_{cond} = 2(P_{pre} + P_{on} + P_{Vcc}) \quad (3.33)$$

3.4.2 Driver Conduction Loss Estimation

Equations (3.19), (3.27) and (3.32) can be used in a software package to calculate conduction loss during the pre-charge time. However, under certain conditions, with simple piecewise linear approximations, the conduction loss calculations can be simplified for use in a spreadsheet design file.

In the intended ideal operation of the driver, the inductor current ramps up linearly (during T_{pre}), then charges the power MOSFET gate with a constant current (during T_{on}) and then the excess inductor energy is returned to the driver supply as the inductor current ramps down linearly (during T_{Vcc}) as illustrated in Figure 3.19. To achieve an inductor current close to the desired ideal operation, three conditions are required: 1) the resistance, R_{pre} during the pre-charge interval can be neglected, 2) the current at the end of the pre-charge interval should be much greater than the ripple deviation during T_{on} (i.e. $i_L(t_1) \gg |i_L(t_2) - i_L(t_1)|$); therefore, it is assumed that the inductor current remains constant at $i_L(t_1) = I_g$ during T_{on} , and 3) the resistance, R_{Vcc} during the energy return interval can be neglected. The three conditions are explained in the following subsections.

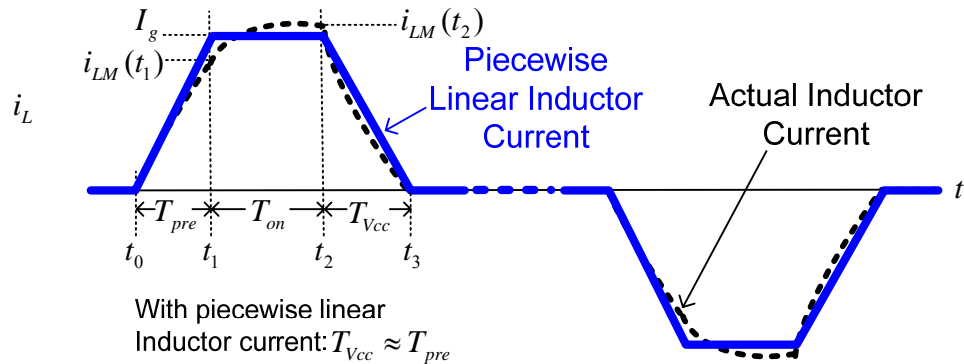


Figure 3.19 Piecewise linear inductor current and actual inductor current

3.4.2.1 Condition One: Pre-Charge Interval

The inductor current as a function of time is plotted in Figure 3.20 up to two time constants. If it is assumed that $R_{pre}=0$, then i_{Lpre} increases linearly as given by (3.34) and shown by the dotted line. From Figure 3.20, for driver designs with $T_{pre} < 0.25\tau_{pre}$, it can be assumed that the inductor current is linear as approximated by (3.34), allowing I_g to be expressed by (3.35).

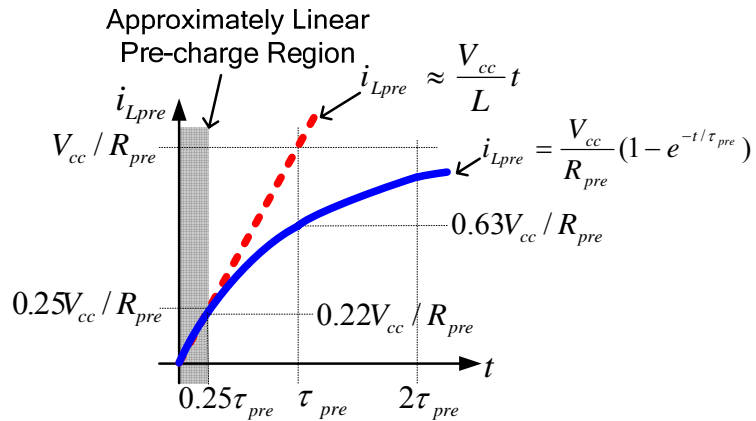


Figure 3.20 Inductor current during the pre-charge time

$$i_{Lpre} \approx \frac{V_{cc}}{L} t \quad (3.34)$$

$$I_g \approx \frac{V_{cc}}{L} T_{pre} \quad (3.35)$$

To simplify the design, the inductor current pre-charge ratio a is introduced as given by (3.36).

$$a = \frac{T_{pre}}{T_{on}} \quad (3.36)$$

The piecewise linear simplification of the inductor current waveform during T_{pre} is highlighted in bold in Figure 3.21. The RMS current during this interval is given by (3.37), which can be expressed by (3.38) using (3.35) and (3.36).

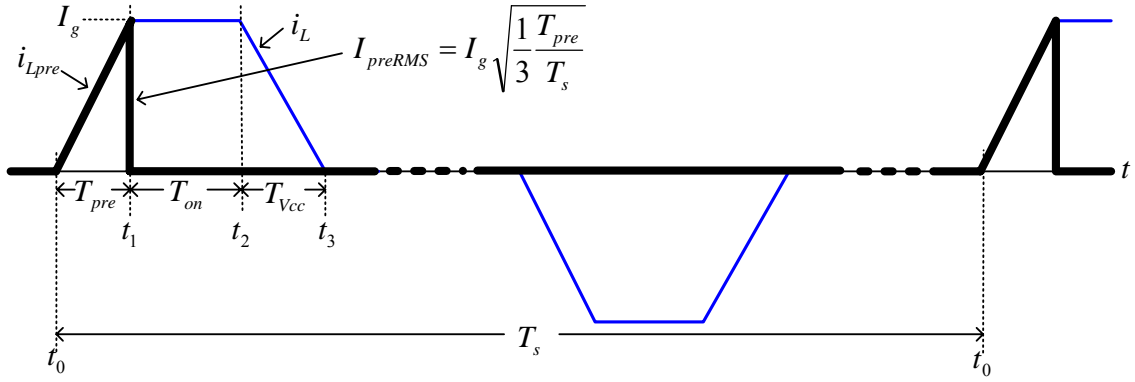


Figure 3.21 Piecewise linear inductor current during the pre-charge interval overlaid on the actual piecewise linear inductor current

$$I_{preRMS} \approx I_g \sqrt{\frac{T_{pre} f_s}{3}} \quad (3.37)$$

$$I_{preRMS} \approx \sqrt{\frac{I_g^3 L f_s}{3 V_{cc}}} \quad (3.38)$$

The conduction loss power, P_{pre} , as a function of I_g and T_{pre} , during the interval is approximated by (3.39) using (3.37). P_{pre} as a function of V_{cc} , L and I_g is approximated by (3.40) using (3.38).

$$P_{pre} \approx R_{pre} I_g^2 \frac{T_{pre} f_s}{3} \quad (3.39)$$

$$P_{pre} \approx R_{pre} \frac{I_g^3 L f_s}{3V_{cc}} \quad (3.40)$$

3.4.2.2 Condition Two: Turn On Interval

In the intended operation of the driver, the current at the end of the pre-charge interval should be much greater than the ripple deviation (i.e. $i_L(t_2) - i_L(t_1)$) during T_{on} . Therefore, it is assumed that the inductor current remains constant at $i_{Lon} = i_L(t_1) = i_L(t_2) = I_g$ through T_{on} , following the piecewise linear approximation illustrated in Figure 3.19. The piecewise linear simplification of the inductor current waveform during T_{on} is highlighted in bold in Figure 3.22.

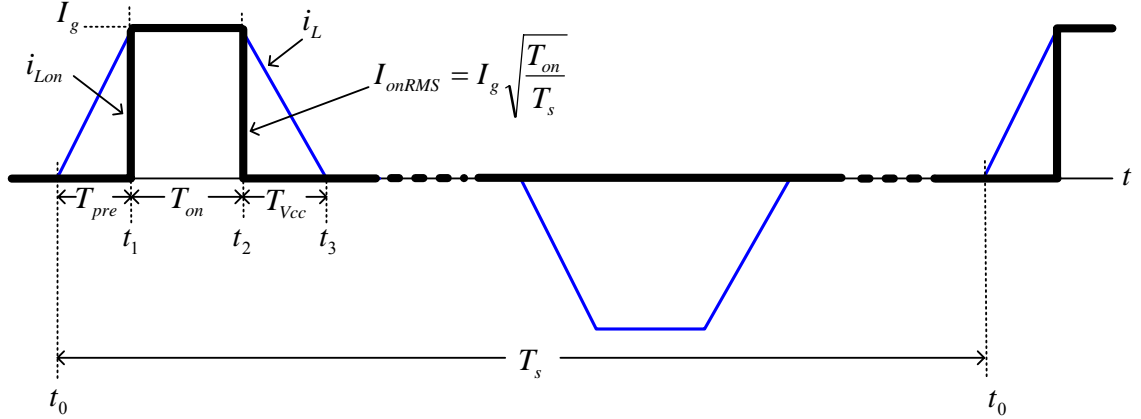


Figure 3.22 Piecewise linear inductor current during the turn on interval overlaid on the actual piecewise linear inductor current

The RMS current during this interval is given by (3.41), which can be expressed by (3.42) using (3.35) and (3.36).

$$I_{onRMS} \approx I_g \sqrt{a T_{pre} f_s} \quad (3.41)$$

$$I_{onRMS} \approx \sqrt{I_g Q_g f_s} \quad (3.42)$$

The conduction loss power, P_{on} , as a function of a , I_g and T_{pre} , during the interval is approximated by (3.43) using (3.41). P_{on} as a function of V_{cc} , L and I_g is approximated by (3.44) using (3.42).

$$P_{on} \approx R_{on} I_g^2 a T_{pre} f_s \quad (3.43)$$

$$P_{on} \approx R_{on} I_g Q_g f_s \quad (3.44)$$

3.4.2.3 Condition Three: Energy Return Interval

Following the condition presented for the pre-charge interval, for driver designs with $T_{Vcc} < 0.25\tau_{Vcc}$, it can be assumed that the inductor current is linear as approximated by (3.45), where V_F represents the diode forward voltage drop in the body diode of S_4 . The energy return interval can be estimate by (3.46).

$$i_{LVcc} \approx I_g - \frac{V_{cc} + V_F}{L} t \quad (3.45)$$

$$T_{Vcc} \approx I_g \frac{L}{V_{cc} + V_F} \quad (3.46)$$

The piecewise linear simplification of the inductor current waveform during T_{Vcc} is highlighted in bold in Figure 3.23. The RMS current during this interval is given by (3.47), which can be expressed by (3.48) using (3.46).

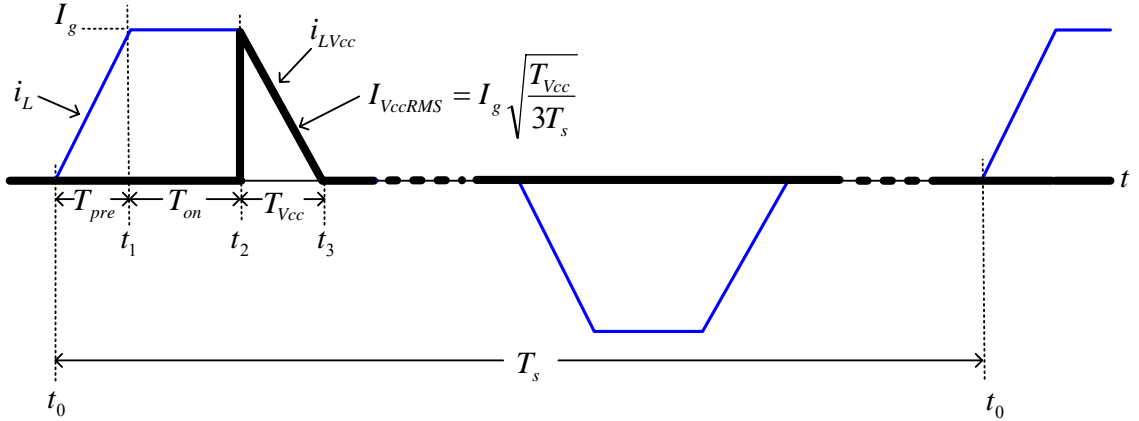


Figure 3.23 Piecewise linear inductor current during the energy return interval overlaid on the actual piecewise linear inductor current

$$I_{VccRMS} \approx I_g \sqrt{\frac{T_{Vcc} f_s}{3}} \quad (3.47)$$

$$I_{V_{cc}RMS} \approx \sqrt{\frac{I_g^3 L f_s}{3(V_{cc} + V_F)}} \quad (3.48)$$

The conduction loss power, $P_{V_{cc}}$, as a function of I_g and $T_{V_{cc}}$, during the interval is approximated by (3.49) using (3.47). $P_{V_{cc}}$ as a function of V_{cc} , L and I_g is approximated by (3.50) using (3.48).

$$P_{V_{cc}} \approx I_g T_{V_{cc}} f_s \left(\frac{1}{3} R_{V_{cc}} I_g + \frac{1}{2} V_F \right) \quad (3.49)$$

$$P_{V_{cc}} \approx \frac{I_g^2 L f_s}{V_{cc} + V_F} \left(\frac{R_{V_{cc}} I_g}{3} + \frac{1}{2} V_F \right) \quad (3.50)$$

To calculate the total estimated conduction loss, it can be assumed that the turn on and turn off states of operation are identical. Therefore, under this assumption, the total estimated piecewise linear conduction loss in the proposed current source gate drive circuit is given by (3.51), which is two times the sum of P_{pre} , given by (3.39), plus P_{on} , given by (3.43), plus $P_{V_{cc}}$, given by (3.49). Alternately, P_{cond} can be expressed by (3.52), using (3.40), (3.44) and (3.50).

$$P_{cond} \approx 2 \left[I_g^2 \left(R_{pre} \frac{T_{pre}}{3} + R_{on} T_{pre} + R_{V_{cc}} \frac{T_{V_{cc}}}{3} \right) + I_g \frac{V_F T_{V_{cc}}}{2} \right] f_s \quad (3.51)$$

$$P_{cond} \approx 2 \left[\left(I_g^3 \left(\frac{R_{pre}}{3V_{cc}} + \frac{R_{V_{cc}}}{3(V_{cc} + V_F)} \right) + I_g^2 \frac{V_F}{2(V_{cc} + V_F)} \right) L + I_g R_{on} Q_g \right] f_s \quad (3.52)$$

3.4.3 Gate Loss

The second significant component of driver circuit loss is driver switch gate loss and is given by (3.53), where Q_{g1} , Q_{g2} , Q_{g3} and Q_{g4} represent the total gate charge in S_1 - S_4 and V_{dd} represents the gate driving voltage for S_1 - S_4 .

$$P_{S_1-S_4 gate} = (Q_{g1} + Q_{g2} + Q_{g3} + Q_{g4}) V_{dd} f_s \quad (3.53)$$

3.4.4 CV² Output Loss

The CV² output loss in S_2 and S_4 at turn on, is given by (3.54) where C_{oss2} and C_{oss4} represent the output capacitance values for S_2 and S_4 obtained from the MOSFET data sheets.

$$P_{out} = \frac{1}{2}(C_{oss2} + C_{oss4})V_{cc}^2 f_s \quad (3.54)$$

3.4.5 Turn Off Loss

S_2 and S_4 turn off at the peak inductor current, $i_L(t_2)=I_g$. The turn off loss in S_2 and S_4 is given by (3.55) where the fall times, T_{f2} and T_{f4} are obtained from the MOSFET data sheets.

$$P_{off} = \frac{1}{2}V_{cc} I_g (T_{f2} + T_{f4}) f_s \quad (3.55)$$

3.4.6 Core Loss

The core loss can be obtained by standard core loss estimation methods and should be small in comparison to the other loss components. If air core inductors are used, the core loss is zero.

3.4.7 Logic Loss

The loss in the logic circuit should be negligible in comparison to the other components, so it can be neglected.

3.4.8 Total Driver Loss

The total loss, P_{tot} , in the proposed driver is the sum of the loss components presented in 3.4.2-3.4.5 as given by (3.56).

$$P_{tot} = P_{cond} + P_{S1-S4gate} + P_{out} + P_{off} \quad (3.56)$$

3.5 Current Source Driver Design Procedure

The power MOSFET turn on transition time, T_{on} , (from 0V to V_{cc}), or average gate current, I_g , must be chosen by the designer for the given application. For the designer, there is a tradeoff between speed (i.e. switching loss reduction, or reduced body diode conduction) and gate energy

recovery. Increased gate current (smaller values of T_{on}) results in greater conduction loss in the driver. Typically, T_{on} should be less than 10% of the switching period.

After selecting T_{on} (or I_g), a circuit designer has a choice of the turn on inductor pre-charge time, T_{pre} , or inductor value, L , using the ratio, a . This is illustrated in Figure 3.15 from t_0 - t_1 , of the inductor current waveform during the turn on interval. Typically, T_{pre} should be in the range of $0.25T_{on} < T_{pre} < 3T_{on}$. Larger values of T_{pre} (and a) yield a larger required inductance and add more delay in the control loop, but provide a more constant gate current and improved gate energy recovery. Smaller values of T_{pre} (and a) yield a smaller required inductance, which is beneficial for component size, however, loss in the drive circuit increases since the inductor pre-charge interval becomes non-linear and the inductor current ripple during T_{on} becomes large.

Using (3.15), (3.35) and ratio a defined in (3.36), the required inductance can be calculated using (3.57).

$$L = a \frac{V_{cc} T_{on}^2}{Q_g} \quad (3.57)$$

Setting $a=0.5$ is a good starting point assumption for the driver design. With this assumption, using (3.15) and (3.35), the required inductance can be calculated using (3.58).

$$L = 0.5 \frac{V_{cc} T_{on}^2}{Q_g} \quad (3.58)$$

3.6 Design Example

A design and loss analysis of the proposed driver was conducted using the total driver loss in section 3.4.8 and the design procedure presented in section 3.5. The parameters for the design are given in Table 3.3. A turn on time, T_{on} , of 50ns, was selected along with a pre-charge time, T_{pre} , of 25ns ($a=0.5$). Using these values, the calculated driver inductance is 139nH.

A loss breakdown of the proposed driver is given in Figure 3.24. The results are compared to

the estimated loss in a conventional driver using (2.1) at 1.5 times the QV loss as explained in Chapter 2, section 2.4.1. It is noted that the losses in the conventional driver are 82% greater than those in the proposed current source driver.

Table 3.3 Current source driver design parameters

Parameters			
Switching Frequency	1MHz		
Gate Drive Voltage, V_{cc}	5V		
Turn On Time, T_{on}	50ns		
Pre-charge Time, T_{pre}	25ns		
Energy Return Time, $T_{V_{cc}}$	50ns		
Driver Inductor, L	139nH		
Driver Inductor Resistance, R_L	25m Ω		
MOSFET, M		IRF6618	
Total Gate Charge, Q_g	45nC		
Internal Gate Resistance, R_g	1 Ω		
Diodes, D_2 & D_4		MBR0520	
Diode Forward Voltage, V_F	0.385V		
Current Source Driver Switches, S_1-S_4		NDS351AN (S_3 & S_4)	FDN342P (S_1 & S_2)
Total Gate Charge, Q_g	1.25nC	6nC	
On Resistance, R_{dson}	90m Ω	60m Ω	
Output Capacitance, C_{oss}	50pF	200pF	
Fall Time, T_f	1ns	2ns	

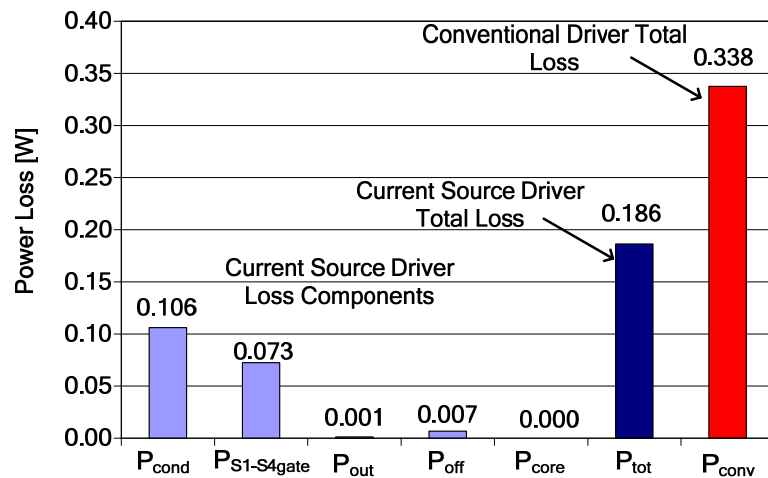


Figure 3.24 Proposed current source driver gate drive loss breakdown with comparison of total losses to total loss in a conventional driver circuit

The largest loss component in the proposed current source driver is conduction loss. The

largest portion of the conduction loss is dissipated in the power MOSFET parasitic gate resistance, R_g , which is typically about 1Ω . Curves of current source driver loss and conventional driver loss as a function of R_g are given in Figure 3.25 in order to demonstrate the potential benefits of using MOSFETS with lower internal gate resistance.

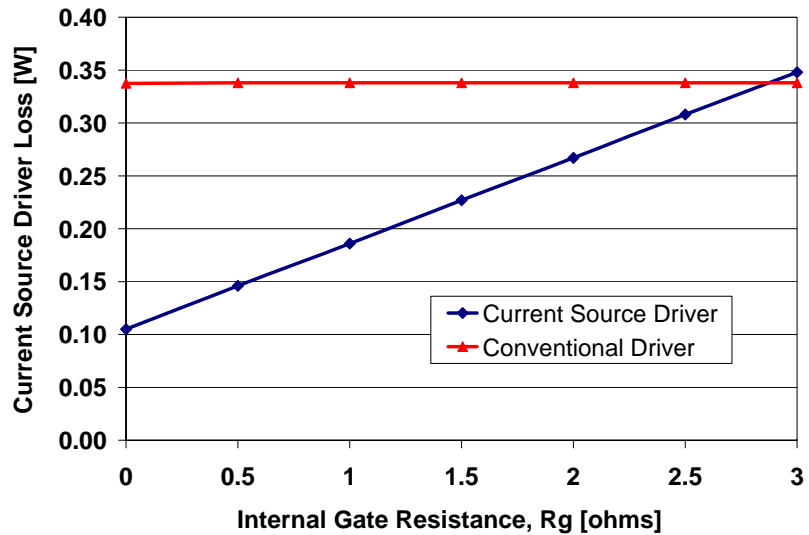


Figure 3.25 Current source driver loss as a function of MOSFET gate resistance

3.7 Logic Circuit Implementation

The logic circuit required to produce the gating signals for the four driver switches, S_1 - S_4 is very simple. The waveforms used to derive the logic are illustrated in Figure 3.26. The logic circuit is illustrated in Figure 3.27. The circuit requires only 2 delay elements and 6 logic elements. The delay elements can be implemented using tapped delay line ICs. The output of the logic circuit is the four gate drive signals. Following the logic, BJT pre-drivers are used to drive the four switches.

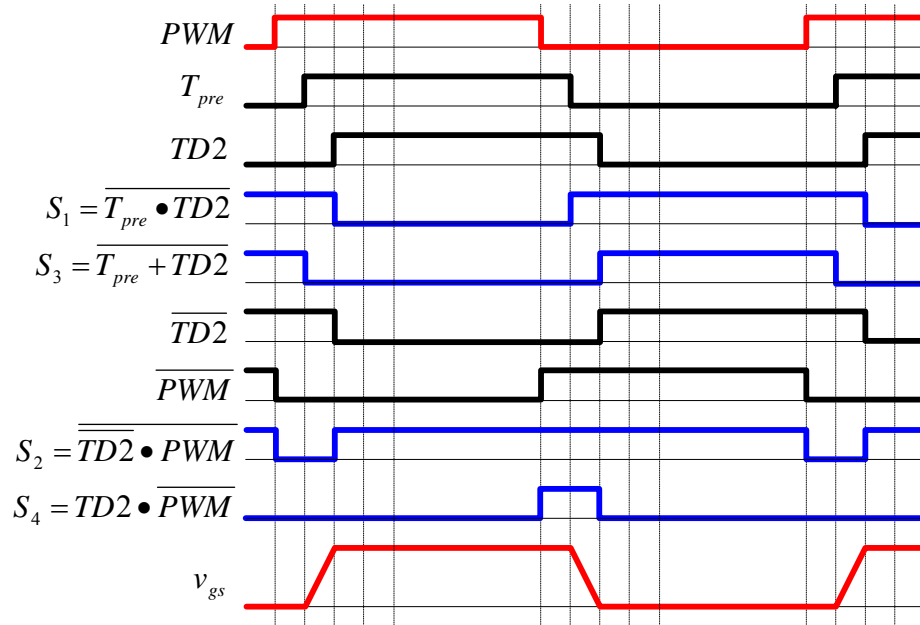


Figure 3.26 Logic waveforms

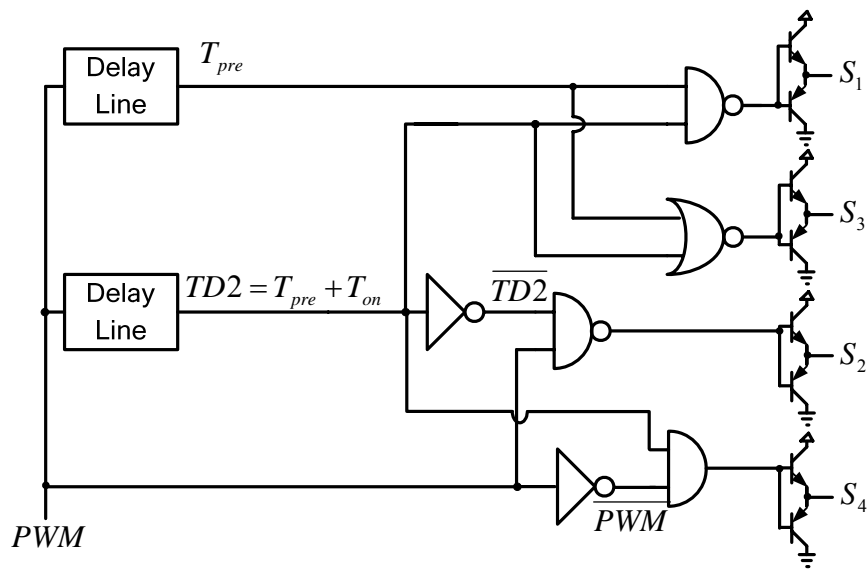


Figure 3.27 Logic circuit

3.8 Experimental Results

In this section, experimental results are presented for the proposed current source driver.

3.8.1 Driver and Circuit Parameters

The proposed current source driver was built using discrete components and compared to the Texas Instruments UCC37322 state of the art driver using the boost converter topology operating at 1MHz. The boost converter and its input/output specifications were chosen as a simple, ground referenced drive, single switch test application in order to demonstrate the capabilities of the proposed current source driver.

The circuit boost converter specifications were as follows: $V_{in}=5V$, $V_o=10V$, $I_o=5A$, $L_{boost}=1mH$, $f_s=1MHz$. The boost MOSFET was part number IRF6618, rated for 30V. In addition, an International Rectifier 10TQ035 schottky diode was used in the boost converter. The output capacitance consisted of six 10 μ F, 16V, 1206 ceramic capacitors. A 6-layer, 1.5oz. PCB was used for both prototypes. A photo displaying both prototypes is given in Figure 3.28. The boost converter with current source driver is on the left and the boost converter with conventional driver, UCC37322, is on the right. It is noted that the circuit area occupied by the proposed driver is much larger than the conventional driver. However, for practical implementation and wide spread use, complete semiconductor integration of the proposed driver would reduce its size significantly.

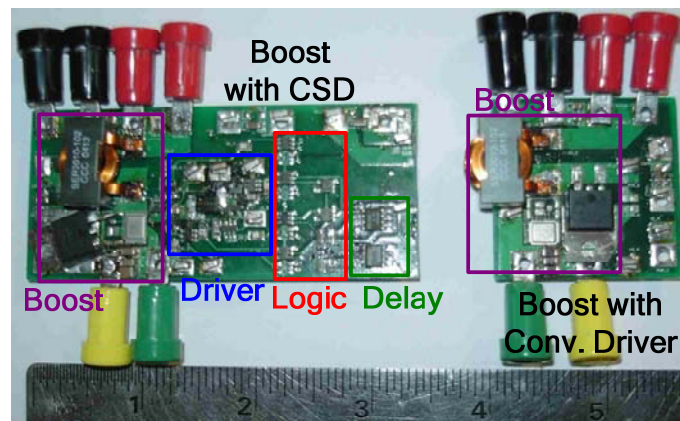


Figure 3.28 Photo of the proposed current source driver (CSD) in a boost converter topology (left) and the boost converter with UCC37322 driver (right; driver on bottom)

The current source driver was designed to deliver 1.25A average gate charging current to the IRF6618 gate in order to demonstrate the switching loss reduction discussed in section 3.3. In order to do so, a turn on time of approximately 40ns ($T_{on}=Q_g/I_g=45nC/1.25A=36ns$) was selected with a pre-charge time, T_{pre} , of 20ns. Dallas Semiconductor DS1100 tapped delay lines were used to implement the delay times. Fairchild UHS series discrete logic components were used to implement the logic. Fairchild FMBT3646 BJT pair pre-drivers were used to drive the CSD driver switches, S_1 - S_4 . A 100nH Coilcraft 1812SMS-R10L air core inductor was used for the driver inductance, L . Fairchild NDS351AN n-channel MOSFETs were used for S_3 and S_4 . Fairchild FDN342P p-channel MOSFETs were used for S_1 and S_2 .

3.8.2 Driver Operation

Waveforms for the proposed current source driver are given in Figure 3.29. The waveforms are given for one period of operation at 1MHz. The four driver switch gate signals are given along with the gate-source voltage of the IRF6618 MOSFET and the driver inductor current. All waveforms agree with the theory. Most notably, the pre-charge intervals and turn on/off intervals are demonstrated by the gating signals and inductor current shape. Note that the S_1 and S_2 switches are p-channel MOSFETs, so they are active low. The inductor current is discontinuous as expected.

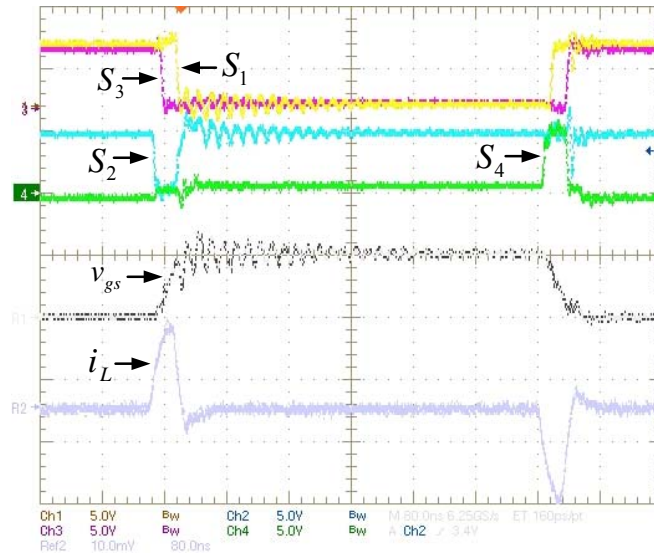


Figure 3.29 Current source driver waveforms; top: S_1 and S_3 gate signals (5V/div, 200ns/div), second: S_2 and S_4 gate signals (5V/div), third: IRF6618 gate-source voltage (5V/div), bottom: inductor current (1A/div)

Detailed waveforms of the turn on transition are provided in Figure 3.30. The three control signals for S_1 , S_2 and S_3 are at the top (S_4 is not shown and remains off for the entire turn on transition). The middle waveform is the IRF6618 gate voltage and the bottom waveform is the driver inductor current. The turn on of S_2 (active low) initiates the turn on inductor pre-charge interval where the inductor current ramps up during T_{pre} . After the designed 20ns, S_3 turns off allowing the inductor to charge the gate of the IRF6618 power MOSFET during T_{on} . During this interval the gate current remains at approximately 1.25A and the power MOSFET voltage charges from 0V to $V_{cc}=5V$. After 40ns, the gate is clamped high when S_1 (active low) turns on. After S_1 turns on, the inductor current ramps back down to zero while the inductor energy is returned to V_{cc} .

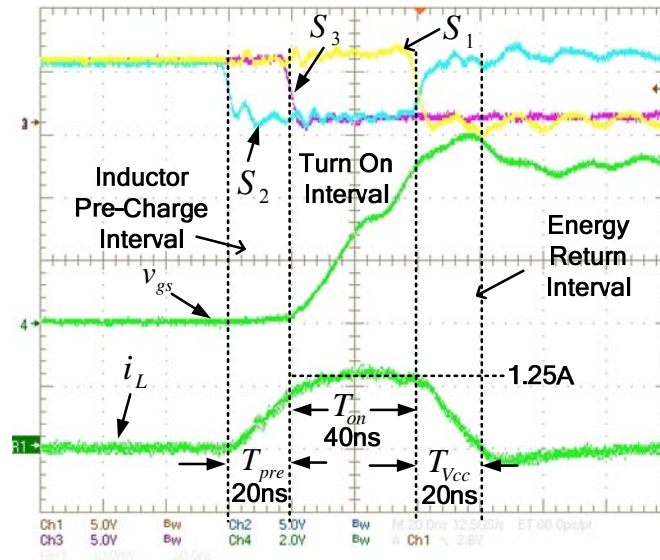


Figure 3.30 Detailed turn on waveforms; top: gate signals for S_1 , S_2 and S_3 (5V/div, 20ns/div), second: IRF6618 gate-source voltage (2V/div), bottom: CSD inductor current (1A/div)

Detailed waveforms of the turn off transition are provided in Figure 3.31. The three control signals for S_1 , S_3 and S_4 are at the top (S_2 is not shown and remains off for the entire turn on transition). The middle waveform is the IRF6618 gate voltage and the bottom waveform is the driver inductor current. The turn on of S_4 initiates the turn off inductor pre-charge interval where the inductor current ramps negative during T_{pre} . After the designed 20ns, S_1 turns off (active low) allowing the inductor continue to continue to ramp negative at a decreasing rate while at the same time discharging the gate of the IRF6618 power MOSFET. During this interval the gate current remains at approximately -1.25A and the power MOSFET gate voltage discharges from $V_{cc}=5V$ to 0V. After 40ns, the gate is clamped low when S_3 turns on. After S_3 turns on, the inductor current ramps back down to zero while the inductor energy is returned to V_{cc} .

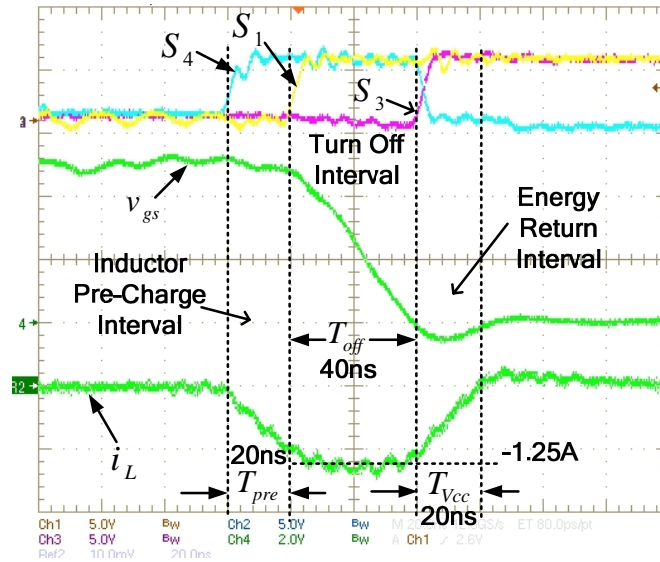


Figure 3.31 Detailed turn off waveforms; top: gate signals for S_1 , S_3 and S_4 (5V/div, 20ns/div), second: IRF6618 gate-source voltage (2V/div), bottom: CSD inductor current (1A/div)

3.8.3 Boost Converter Efficiency and Losses

The efficiency and total loss curves (driver and boost converter powertrain) for the proposed current source driven boost and UCC37322 driven boost are provided in Figure 3.32 and Figure 3.33, respectively. It is noted that in the testing, all components were the same in both circuits except for the drivers. The current source driver maintains greater efficiency and lower power loss across the entire load range. Furthermore, the efficiency improvement at full load is 2.9%, representing a total power loss reduction of 1.85W. It is noted that the loss reduction of 1.85W is very close to the 1.8W predicted and simulated in section 3.3. The loss reduction with the proposed driver is achieved by reduced gate drive loss and reduced switching loss. In addition, at 1A load current in Figure 3.33, the proposed current source driver achieves a loss reduction of 0.16W (1.36-1.20W). At 1A load current, switching loss and conduction loss are very small, so this loss reduction can be attributed to gate energy recovery. The loss reduction of 0.16W is very close to the 0.15W predicted in the analysis results reported in Figure 3.24.

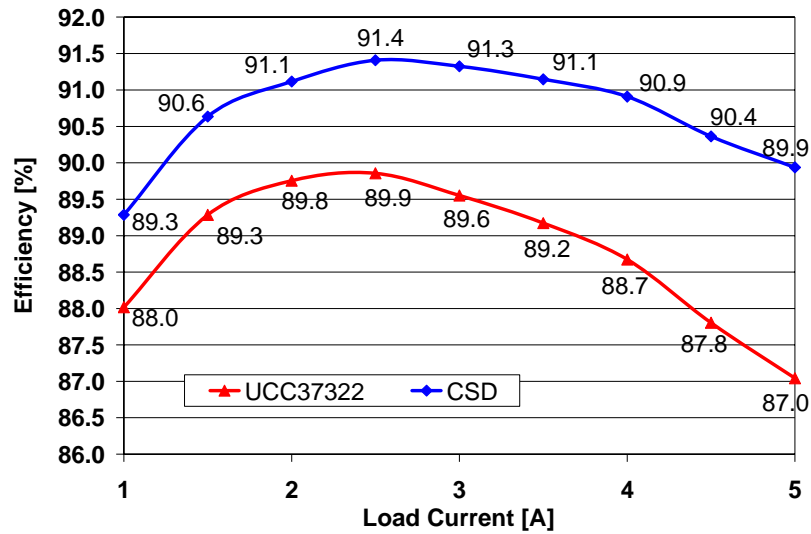


Figure 3.32 Efficiency curves as a function of load for the boost converter with proposed current source driver and UCC37322 driver operating at 1MHz, 5V input and 10V output; NOTE: 2.9% efficiency improvement at full load

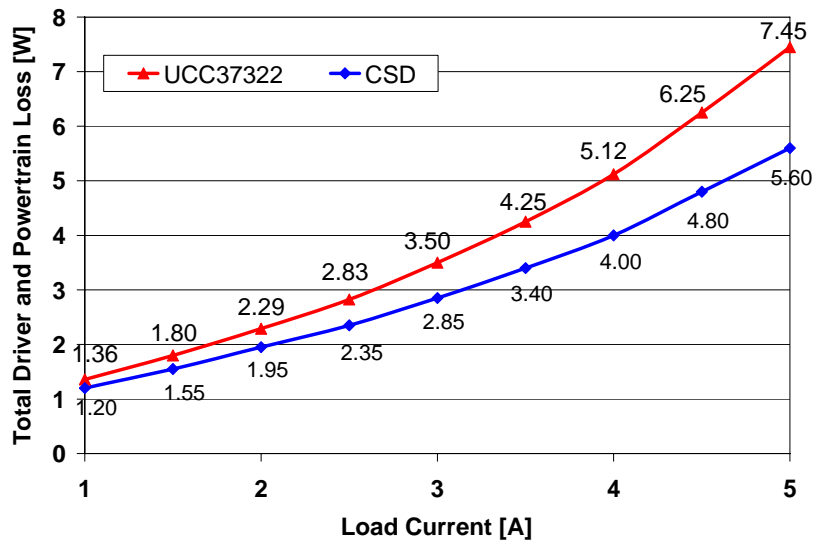


Figure 3.33 Total loss curves as a function of load for the boost converter with proposed current source driver and UCC37322 driver operating at 1MHz, 5V input and 10V output; NOTE: 1.8W loss reduction achieved at full load

A curve of loss reduction with the current source driver with respect to the conventional driver is given in Figure 3.34. It is noted that the proposed driver enables the boost converter to operate with 24.8% less loss at full load than the conventional driver. For many applications, this

loss reduction could potentially lead to significant cost savings in components, heat sinks, or cooling.

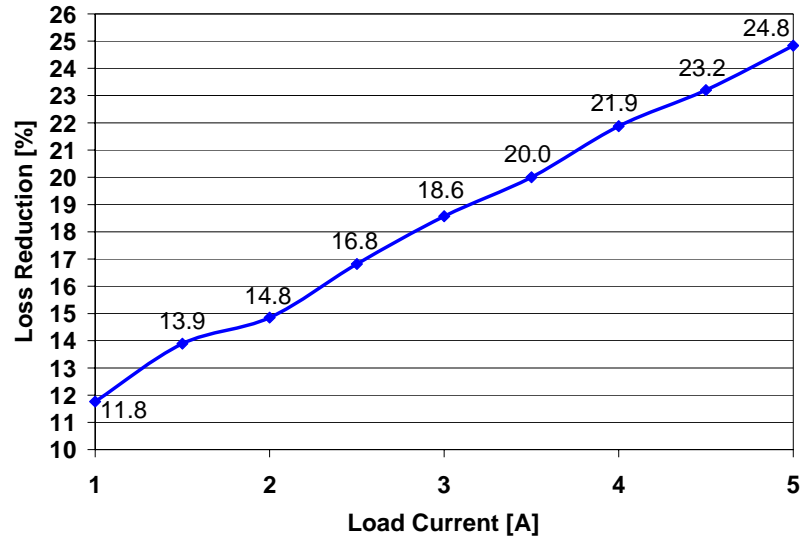


Figure 3.34 Loss reduction as a function of load current for the boost converter with proposed current source driver with respect to the UCC37322 driver operating at 1MHz, 5V input and 10V output

3.8.4 Driver Losses

The proposed driver was tested at other turn on times of 20ns, 50ns, 80ns, 110ns and 140ns. There is a design tradeoff for the proposed driver between speed and driver loss. Greater switching speed (i.e. smaller T_{on}) requires greater driver current, which increases conduction loss in the driver. On the other hand, an added benefit is that as turn on time decreases, the required driver inductance also decreases. Curves of the proposed driver loss are given as a function of turn on time, T_{on} , in Figure 3.35. Curves of the actual measured driver loss are also included. It is noted that the proposed driver operates with lower driving loss than the UCC37322 for all turn on times achievable with the UCC37322 driver. While the driving loss reduction is small (50mW-100mW for the example given), in other applications at higher switching frequencies, or with multiple switches, the potential for gate energy savings can become a significant.

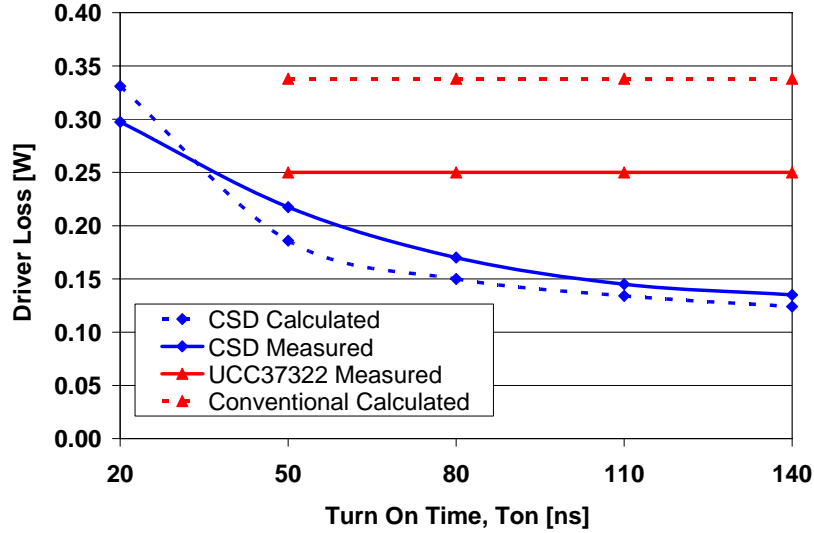


Figure 3.35 Curves of driver loss as a function of turn on time

3.8.5 Range of Duty Cycle Operation

The proposed current source driver operates correctly for duty cycles ranging from 0%-100%. Driver waveforms at 3% duty cycle are given in Figure 3.36. The top waveform is the PWM signal. The second waveform is the IRF6618 gate-source voltage and the bottom waveform is the driver inductor current. The peak inductor current during turn on is 1.25A as expected. However, at turn off the peak inductor current is -1A. The lower peak inductor current at narrow duty cycles is expected since the turn on energy recovery time, $T_{V_{cc}}$ and the turn off pre-charge time, T_{pre} overlap. This overlap causes the turn off time to be slightly slower than expected. However, if the power MOSFET gate is not fully discharged by the inductor current after T_{off} , it quickly discharges when S_3 turns on. It is also noted that when the PWM input duty cycle is 0%, the power MOSFET gate-source voltage will remain clamped at 0V.

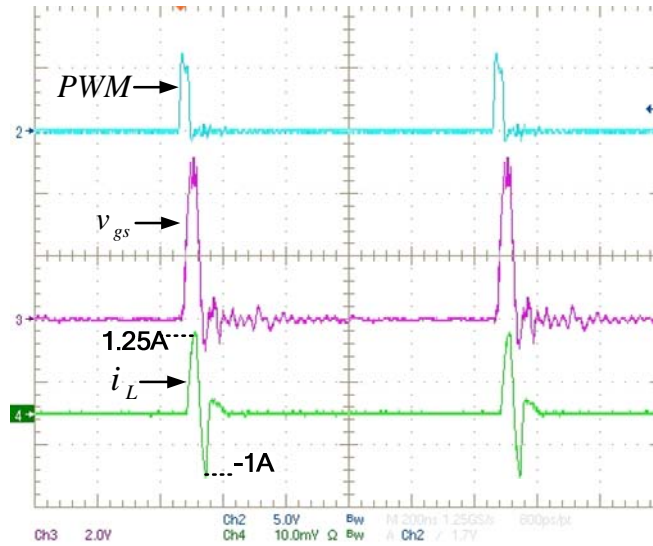


Figure 3.36 Current source driver waveforms at 3% duty cycle; top: PWM signal (5V/div, 200ns/div), second: IRF6618 gate-source voltage (2V/div), bottom: driver inductor current (1A/div)

Driver waveforms at 97% duty cycle are given in Figure 3.37. The top waveform is the PWM signal. The second waveform is the IRF6618 gate-source voltage and the bottom waveform is the driver inductor current. In contrast to the 3% duty cycle example, the peak inductor current during turn off is -1.25A as expected and the peak inductor current at turn on is 1A. At wide duty cycles, the turn off energy recovery time, $T_{V_{cc}}$ and the turn on pre-charge time, T_{pre} overlap, resulting in the turn on time to be slightly slower than expected. However, if the power MOSFET gate is not fully charged by the inductor current after T_{on} , it quickly charges to V_{cc} when S_I turns on.

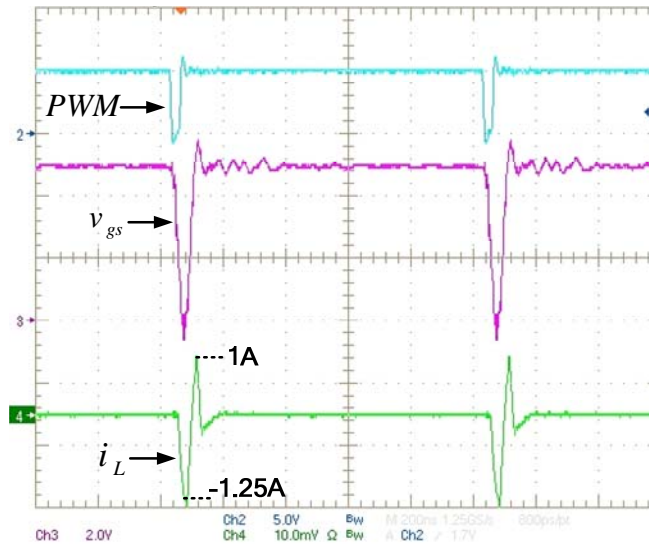


Figure 3.37 Current source driver waveforms at 97% duty cycle; top: PWM signal (5V/div, 200ns/div), second: IRF6618 gate-source voltage (2V/div), bottom: driver inductor current (1A/div)

3.8.6 Driver Inductor Tolerance

The most significant benefit of the proposed current source driver is that it operates as a current source to drive the power MOSFET during the turn on and turn off times. In addition, another significant benefit is that during the remainder of the switching period, the driver behaves like a conventional driver with the power MOSFET gate clamped high, or low by the driver switches. This complementary behavior of the driver switches makes the driver very robust.

One common issue in implementation is inductor tolerance. Inductors typically have tolerances of +/- 20% or more. In the proposed driver, if the inductor is undersized, the power MOSFET gate will charge and discharge quicker than expected. If the gate voltage reaches the supply rails during the dead time between S_1 and S_3 , then the body diodes of S_1 and S_3 clamp the voltage high at turn on and low at turn off. This is illustrated in Figure 3.38, where the 100nH inductance was replaced by a 40nH inductance. The smaller inductance yields greater inductor current, allowing the gate capacitance to charge/discharge quicker and reach the supply rail before S_1 turns on at the turn on transition of the power MOSFET and before S_3 turns off at the

turn off transition of the power MOSFET. At turn on, the gate voltage is briefly clamped to approximately 1V above V_{cc} by D_1 . At turn off, the gate voltage is briefly clamped to approximately -1V by D_3 .

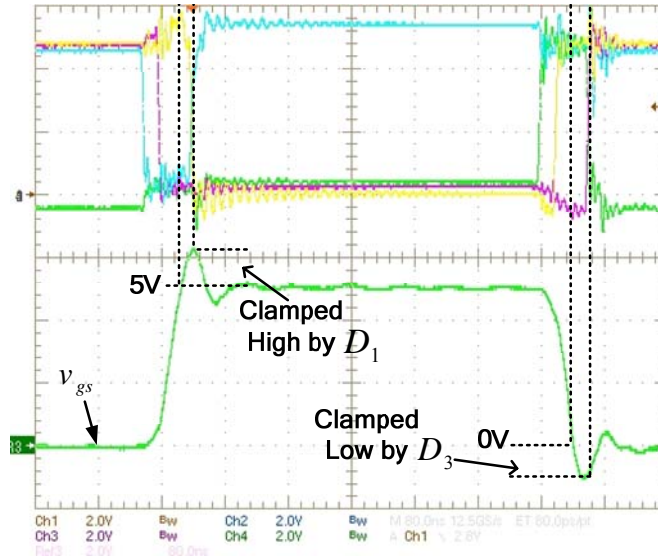


Figure 3.38 Current source driver waveforms illustrating the effect of an undersized inductor; top: gate signals for S_1 - S_4 (2V/div, 80ns/div), bottom: IRF6618 gate-source voltage (2V/div)

The examples in Figure 3.36 and Figure 3.37 demonstrate similar behaviour to when the inductor is above tolerance. In this case, the inductor current is lower than expected when S_1 , or S_3 turn on, so the additional gate charge is supplied from the line, or discharged to ground through S_1 , or S_3 when they turn on.

3.9 Alternate 3-Pulse Driver Implementation

With the proposed circuit illustrated in Figure 3.1, using switches S_2 and S_4 instead of diodes D_2 and D_4 , an alternate version of the proposed driver is illustrated in Figure 3.39. With the alternate version, switches S_2 and S_4 operate at three times the switching frequency (i.e. 3-pulse). The advantage of this approach is potentially lower conduction loss in the switches than the diodes. The disadvantages are a slightly more complex control circuit, illustrated in Figure 3.40,

requiring seven gates and dead time control for S_2/S_4 and increased gate loss driving S_2/S_4 .

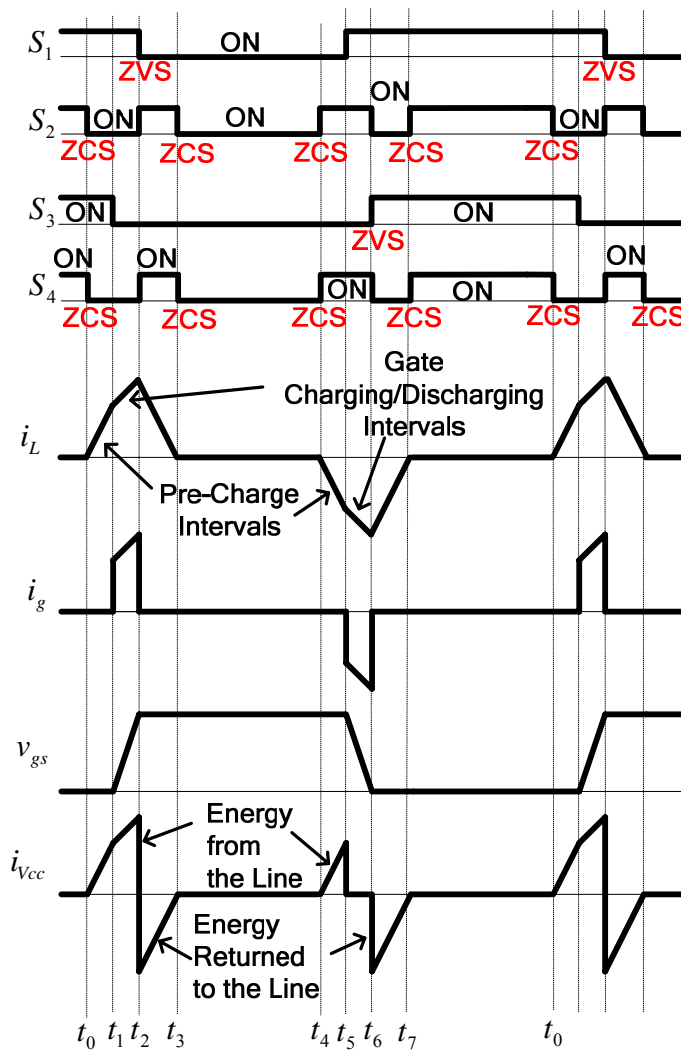


Figure 3.39 Alternate 3-Pulse proposed current source gate driver waveforms

The alternate version of the 3-pulse current source driver was built and tested to drive a pair of IRF6691 power MOSFETs at 1.5MHz switching frequency. The driver waveforms are illustrated in Figure 3.41.

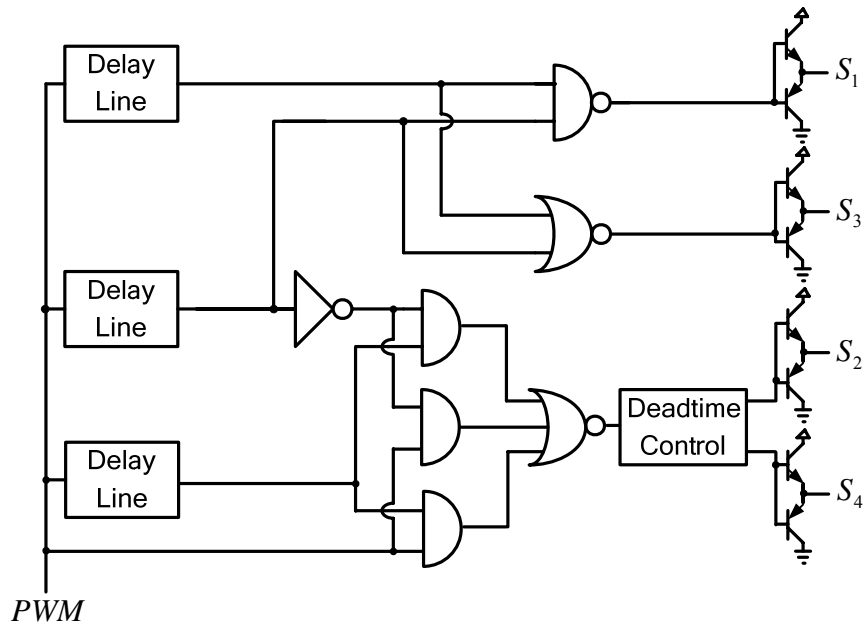


Figure 3.40 Logic circuit used to create the control switch gating signals for S_1 - S_4

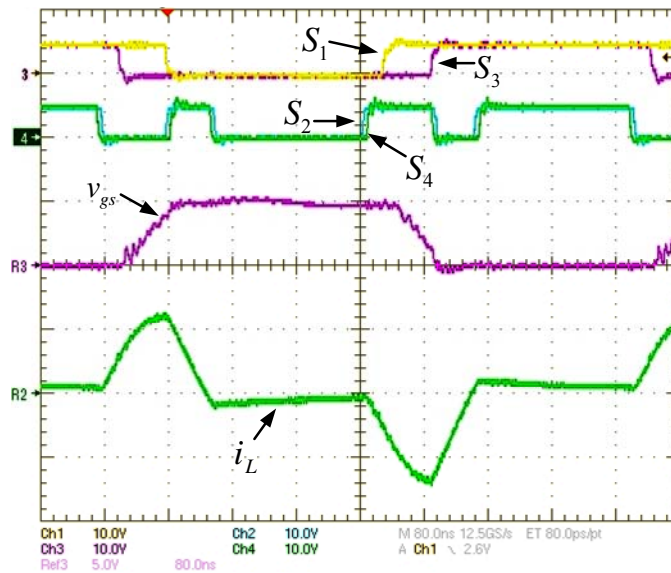


Figure 3.41 Current source driver waveforms; top: S_1 and S_3 gate signals (10V/div, 80ns/div), second: S_2 and S_4 gate signals (10V/div), third: power MOSFET gate-source voltage (5V/div), bottom: inductor current (1A/div)

3.10 Conclusions

A new current source gate drive circuit has been proposed for power MOSFETs. The driver

operation has been explained and a detailed loss analysis has been provided. A design procedure and design example were presented. The logic circuit implementation was included and extensive experimental results were presented.

The proposed circuit achieves quick turn on and turn off transition times to reduce switching loss and conduction loss in power MOSFETS. In addition, it can recover a portion of the QV gate energy normally dissipated in a conventional driver. The circuit consists of four controlled switches and a small inductor (100nH or less, typical). The current through the inductor is discontinuous in order to minimize circulating current conduction loss in the driver. This also allows the driver to operate effectively over a wide range of duty cycles with constant peak current – a significant advantage for many applications since turn on and turn off times do not vary with the operating point. The driver provides superior performance in comparison to conventional drivers and solves the problems of existing resonant gate drivers. Experimental results have been presented for the proposed driver operating in a boost converter at 1MHz, 5V input, 10V/5A output. At 5V gate drive, a 2.9% efficiency improvement is achieved representing a loss reduction of 24.8% in comparison to a conventional driver.

Chapter 4

A High Efficiency MHz Synchronous Buck Voltage Regulator with Current Source Gate Driver^{*}

4.1 Introduction

The multi-phase synchronous buck converter is used nearly exclusively as the voltage regulator (VR) module to power microprocessors due to its simplicity and low component count. In order to reduce the size of the VR passive components and to improve the dynamic response, the switching frequency must increase beyond 300kHz into the MHz range [53]-[56]. However, as the switching frequency increases, the switching loss in the buck high side (HS) MOSFET and gate loss in the HS and synchronous rectifier (SR) MOSFETs increase. These two frequency dependent loss components can significantly degrade VR efficiency when switching in the MHz.

In existing multi-phase buck VRs, a conventional complementary pair voltage source driver is used almost exclusively for the buck HS and synchronous MOSFETs. It was demonstrated in Chapter 3 that current source drive can reduce switching loss and recover gate energy. Therefore, this chapter presents a new synchronous buck VR featuring an improved version of the current source driver proposed in Chapter 3.

In section 4.2, the synchronous buck VR current source driver circuit and operation are presented. The benefits of current source drive in a synchronous buck VR are summarized in section 4.3. The logic and level shift circuits are presented in section 4.4. The driver design and optimization are presented in section 4.5 and a design example is provided in section 4.6. Experimental results are provided in section 4.7 and the conclusions are presented in section 4.8.

^{*} The content of this chapter is subject to patent pending for US 2006/0170043 A1, International patent number WO 2006/079219 A1, and has been submitted to the following journal:

[1] W. Eberle, Z. Zhang, Y.F. Liu and P.C. Sen, "A High Efficiency MHz Synchronous Buck Voltage Regulator with Current Source Gate Driver," IEEE Trans. Power Electron, TPEL-2008-02-0067.

4.2 Proposed Synchronous Buck Current Source Gate Driver and Operation

The following sub-sections present the proposed circuit and operation.

4.2.1 Proposed Circuit

The proposed synchronous buck current source gate drive circuit is illustrated in Figure 4.1. The circuit consists of the synchronous buck and two current source drivers similar to the ground referenced driver proposed in Chapter 3. Each driver has four small MOSFETs and two very small inductors that carry a discontinuous current, which minimizes conduction loss and allows the driver to work effectively over a wide duty cycle range. The driver for the HS MOSFET M_1 contains a bootstrap diode D_b and capacitor C_b . The operation of the driver is similar for M_1 and M_2 since each driver operates using independent control signals ($pwmM_1$ and $pwmM_2$) derived with dead time from the PWM controller input.

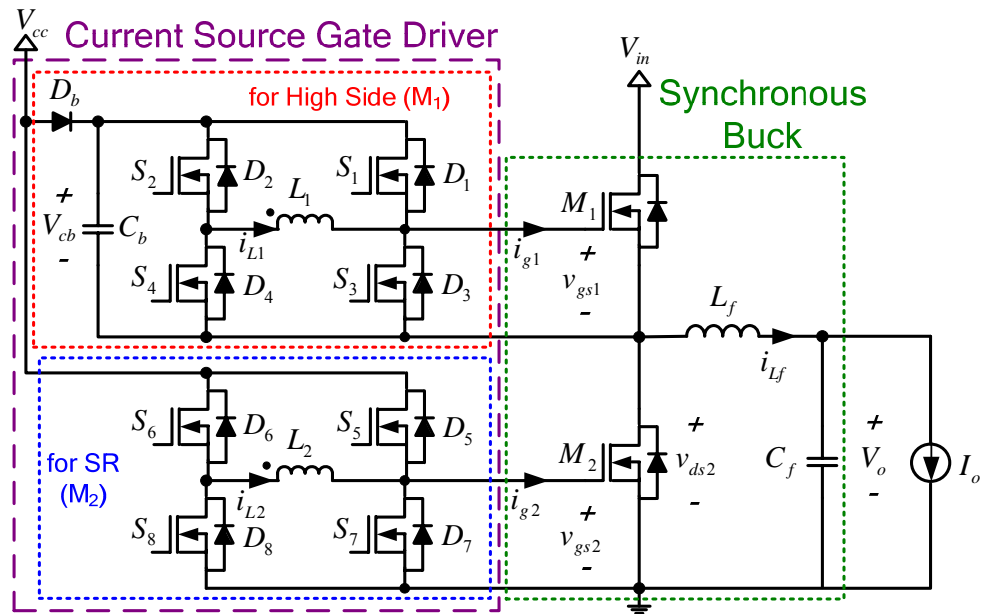


Figure 4.1 Proposed synchronous buck current source gate drive circuit

The piecewise linear driver waveforms are given in Figure 4.2. It is assumed that each driver is supplied with independent PWM inputs, $pwmM1$ for M_1 and $pwmM2$ for M_2 .

Waveforms S_1 - S_4 and S_5 - S_8 represent the gating signals for driver MOSFETs S_1 - S_8 . It is assumed that N-channel MOSFETs are used, so all devices are active high. The D_2 , D_4 , D_6 and D_8 waveforms represent the diode conduction intervals. i_{L1} and i_{L2} represent the inductor currents in the HS MOSFET driver and SR MOSFET driver, respectively. v_{gs1} and v_{gs2} represent the gate-to-source voltage waveforms for MOSFETs M_1 and M_2 , respectively.

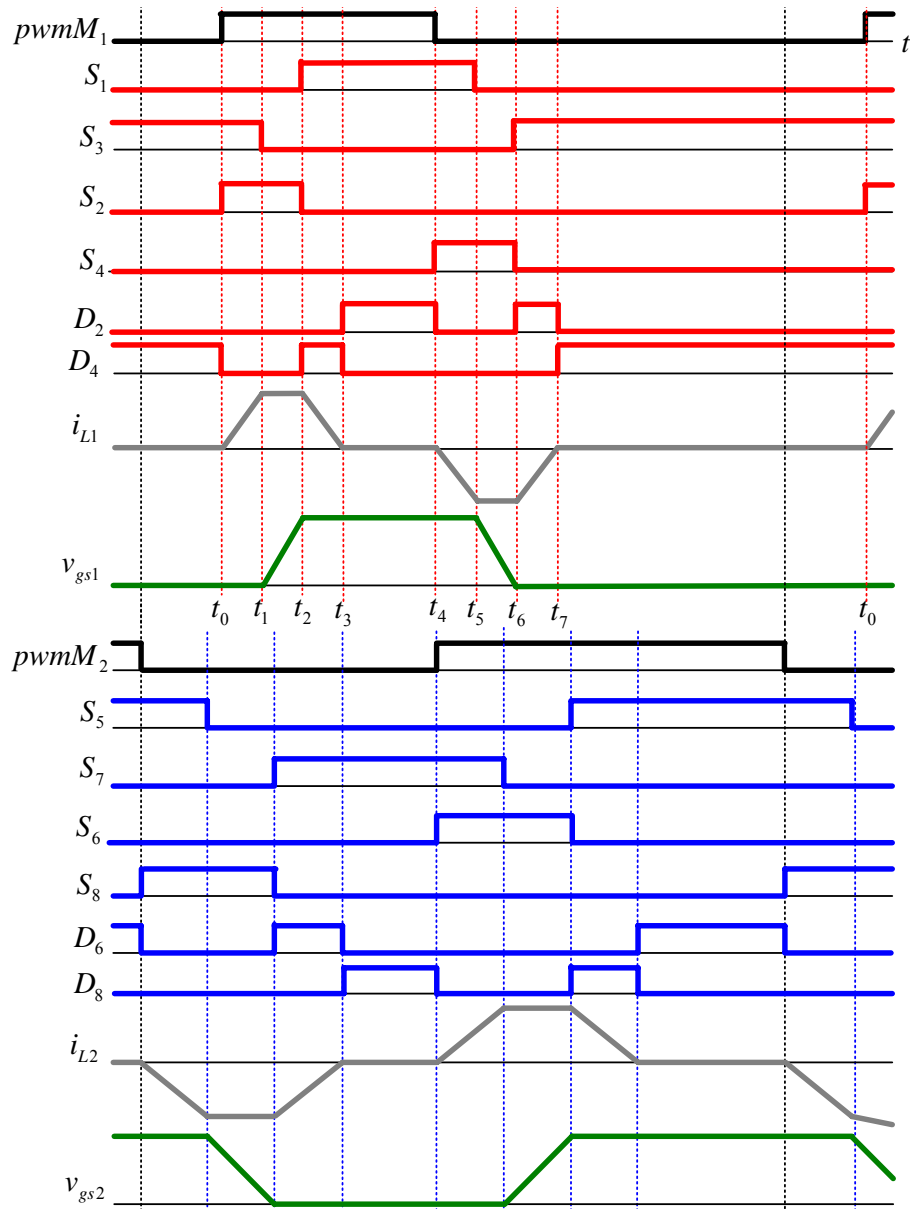


Figure 4.2 Proposed driver waveforms

The key to the driver operation is the controlling of the driver switches and use of the body diodes to generate the discontinuous inductor current waveforms, i_{L1} and i_{L2} . A portion of the inductor current waveform at its peak is then used to charge the power MOSFET gate as a nearly constant current source. This concept is illustrated in Figure 4.3, for the HS driver of M_1 .

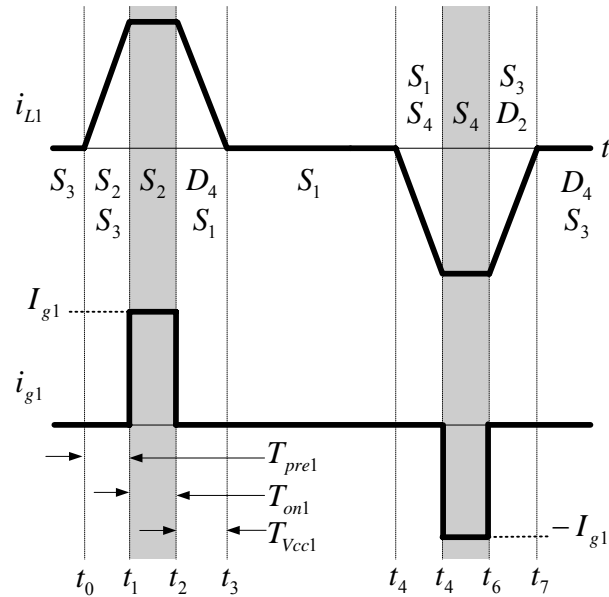


Figure 4.3 Current source driver inductor (top) and gate (bottom) piecewise linear current waveforms for the HS MOSFET (M_1)

4.2.2 Detailed Operation at Turn On

The operation of the circuit is explained for the control MOSFET, M_1 as follows. The timing for M_1 is dictated by the $pwmMI$ signal derived from the PWM signal. Initially, it is assumed that the power MOSFET is in the off state before time t_0 . Initially, only switch S_3 is on and the gate-to-source of M_1 is clamped to zero volts. It is assumed that C_b is large and therefore, $V_{cb} = V_{cc}$.

t_0 - t_1 : At t_0 , S_2 is turned on (with ZCS), therefore turning off D_4 by commutation (with ZCS) and allowing the inductor current to ramp up. The current path during this interval is S_2 - L_1 - S_3 as shown in Figure 4.4. Since S_3 is in the on state, the gate-to-source of M_1 is clamped low. The

interval ends at t_1 dictated by the designed fixed pre-charge time.

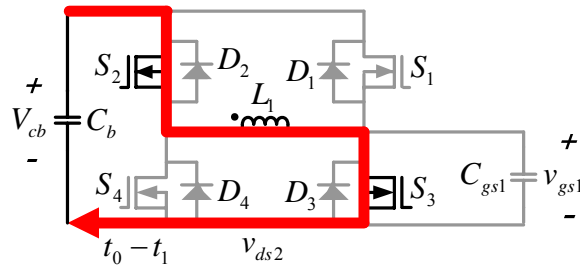


Figure 4.4 HS driver operation during t_0-t_1

t_1-t_2 : At t_1 , S_3 is turned off, allowing the inductor current to begin to charge the gate of M_1 . The current path during this interval is $S_2-L_1-C_{g1}$ as shown in Figure 4.5, where C_{g1} represents the equivalent gate capacitance of M_1 . This interval ends at t_2 , when v_{gs1} reaches V_{cb} . If the inductor pre-charge current at the end of t_1 is much greater than the ripple amplitude during this interval, then the inductor can be assumed to be a current source charging the power MOSFET gate.

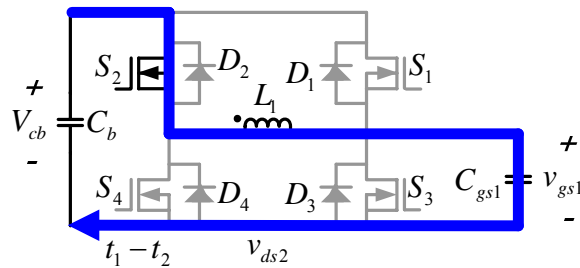


Figure 4.5 HS driver operation during t_1-t_2

t_2-t_3 : At t_2 , S_1 is turned on (with ZVS) and S_2 is turned off, therefore driving on D_4 and allowing the inductor current to conduct into the dot through the path $D_4-L_1-S_1$ as shown in Figure 4.6. In addition, the stored energy in the inductor is returned to the line. During this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps down towards zero. Additionally, the gate-to-source voltage of M_1 remains clamped to V_{cb} . The interval ends when the inductor current reaches zero at t_3 .

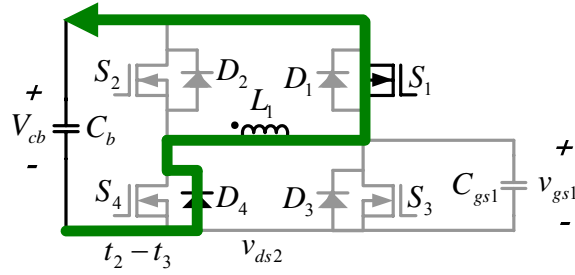


Figure 4.6 HS driver operation during t_2-t_3

t_3-t_4 : At t_3 , S_1 remains on and D_4 turns off (with ZCS), allowing the inductor current to remain at zero as shown in Figure 4.7. During this interval, the gate-to-source voltage of M_1 remains clamped to V_{cb} by S_1 and D_2 . The interval ends at t_4 when the next pre-charging interval for the turn off cycle begins as dictated by the driver logic generated from the *PWM* signal.

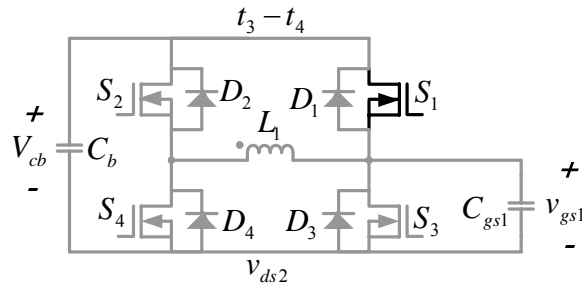


Figure 4.7 HS driver operation during t_3-t_4

4.2.3 Detailed Operation at Turn Off

The turn off interval begins at the end of t_4 . Initially, the inductor current is zero and S_1 is on.

t_4-t_5 : At t_4 , the turn off pre-charging interval begins. S_4 is turned on (with ZCS), therefore turning off D_2 (with ZCS) by commutation. Since S_1 was previously on, the inductor current begins to ramp negative out of the dot through the path $S_1-L_1-S_4$ as shown in Figure 4.8. During this interval, the gate-to-source voltage of M_1 remains clamped to V_{cb} . The interval ends at t_5 dictated by the designed fixed pre-charge time.

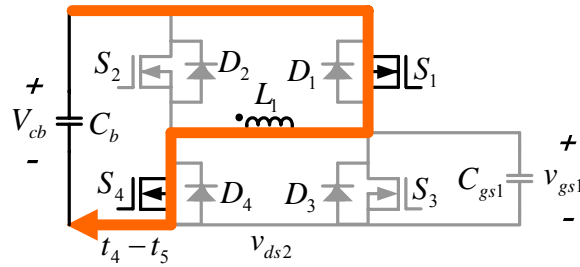


Figure 4.8 HS driver operation during t_4-t_5

t_5-t_6 : At t_5 , S_1 is turned off, allowing the inductor current to begin to discharge the power MOSFET gate. The current path during this interval is $C_{gs1}-L_1-S_4$ as shown in Figure 4.9. The interval ends at t_6 , when v_{gs1} reaches zero. If the inductor pre-charge current at the end of t_5 is much greater than the ripple amplitude during this interval, then the inductor can be assumed to be a current source discharging the power MOSFET gate.

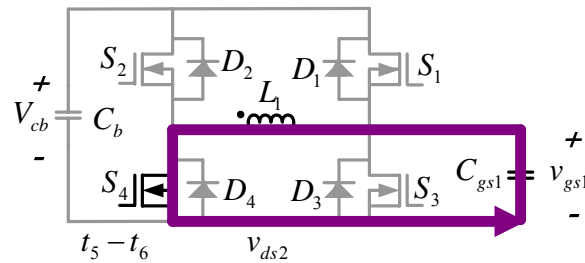


Figure 4.9 HS driver operation during t_5-t_6

t_6-t_7 : At t_6 , S_3 is turned on (with ZVS) and S_4 is turned off, therefore driving on D_2 and allowing the inductor current to conduct out of the dot through the path $S_3-L_1-D_2$ as shown in Figure 4.10. During this interval, the inductor voltage has become reverse biased, so the inductor current quickly ramps to zero. The gate-to-source voltage of M_1 remains clamped to its source voltage, v_{ds2} . The interval ends when the inductor current reaches zero at t_7 .

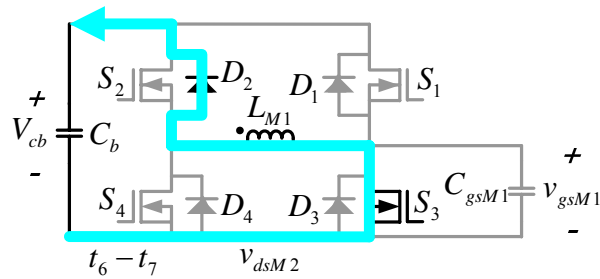


Figure 4.10 HS driver operation during t_6-t_7

t_7-t_0 : At t_7 , S_3 remains on and D_2 turns off (with ZCS), allowing the inductor current to remain at zero as shown in Figure 4.11. During this interval, the gate-to-source voltage of M_1 remains clamped low. The interval ends at t_0 when the pre-charging interval for the turn on cycle begins and the entire process repeats.

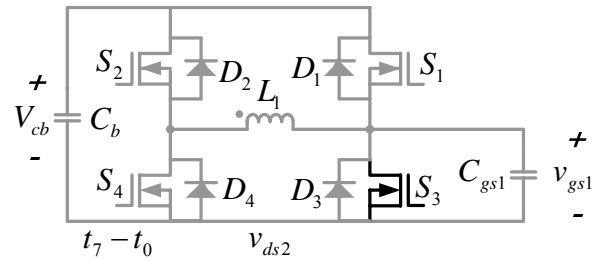


Figure 4.11 HS driver operation during t_7-t_0

The operation of the low side driver for the SR, M_2 is similar to M_1 , except M_2 uses the input signal $pwmM2$ generated with dead time from the PWM signal.

There are several circuit specific benefits of the proposed current source driver in a synchronous buck VR:

- 1) The driver inductors can be very small since the inductor current is discontinuous.
- 2) The peak current is independent of duty cycle and frequency, so it is suitable for narrow duty cycle operation.
- 3) The inductor current is discontinuous, minimizing circulating current, so conduction losses in the driver are minimized.

- 4) The driver switches operate with soft switching.
- 5) The driver does not require DC blocking capacitors which can lead to high current stresses during transients.

4.3 Benefits of Current Source Drive in a Synchronous Buck Voltage Regulator

This section summarizes the four significant system level benefits of current source drive in high frequency synchronous buck voltage regulators. The benefits include: 1) HS MOSFET switching loss reduction, 2) reduced impact on switching loss of HS MOSFET common source inductance, 3) reduced SR body diode conduction, and 4) SR gate energy recovery.

4.3.1 HS MOSFET Switching Loss Reduction

A comparison of gate current waveform for a current source driver and a conventional driver is given in Figure 4.12. The key advantage of the current source driver is that it maintains a large, nearly constant current, I_{gl} , during the rise, T_r , and fall times, T_f , of the switching transitions. On the other hand, for the conventional gate driver, the gate current decays significantly from its peak. The increased gate charging and discharging current during the switching transitions enables faster switching and therefore reduced switching loss.

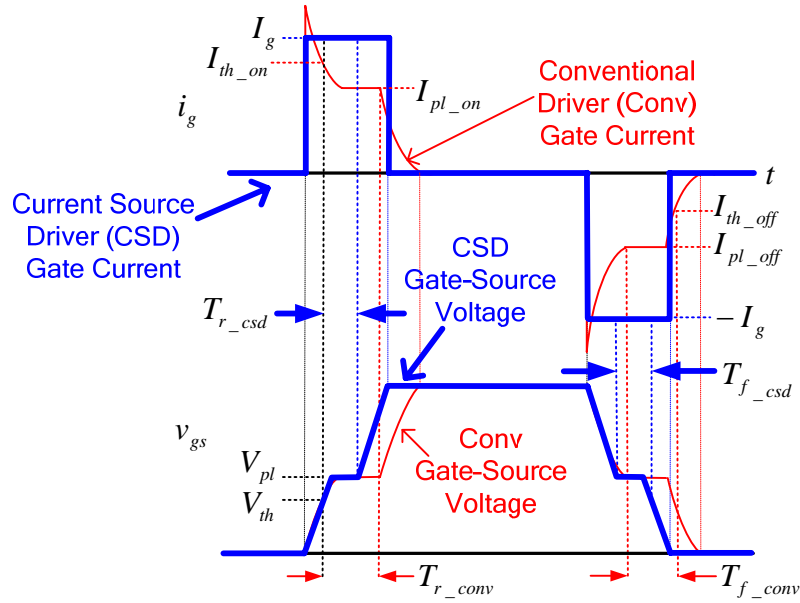


Figure 4.12 Comparison between the gate current and gate-source voltage waveform for the conventional driver and an ideal current source driver

Using the conventional switching loss model [19], neglecting the buck inductor ripple current, the switching loss, P_{sw1} , for the HS MOSFET in a synchronous buck VR can be approximated by (4.1).

$$P_{sw1} \approx \frac{1}{2} f_s V_{in} I_o (T_r + T_f) \quad (4.1)$$

For an ideal current source driver with constant gate drive current, the rise and fall times can be represented by the relationship between gate charge and gate current given by (4.2). In (4.2), Q_{gd} represents the gate-drain charge, Q_{pl} represents the gate charge at the beginning of the turn on plateau and Q_{th} represents the gate charge when the gate-source voltage equals the threshold voltage as illustrated in Figure 4.13.

$$T_r = T_f = \frac{Q_{gd} + Q_{pl} - Q_{th}}{|I_{gM1}|} \quad (4.2)$$

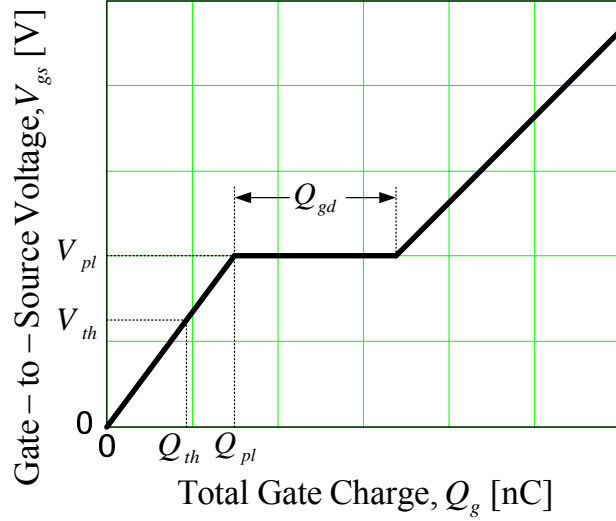


Figure 4.13 Power MOSFET gate-to-source voltage as a function of total gate charge

With a conventional driver, neglecting gate, drain and common source inductance, the rise and fall times are given by (4.3) and (4.4), respectively, where V_{cc} represents the driver supply voltage, V_{pl} represents the MOSFET plateau voltage, V_{th} represents the threshold voltage, R_g represents the HS MOSFET internal gate resistance, R_{ext} represents any external resistance in the driver circuit, R_{lo} represents the resistance of S_N in and R_{hi} represents the resistance of S_P in Figure 2.5.

$$T_r = (R_{hi} + R_{ext} + R_g) \left[\frac{Q_{gd}}{V_{cc} - V_{pl}} + \frac{Q_{pl} - Q_{th}}{V_{cc} - 0.5(V_{pl} + V_{th})} \right] \quad (4.3)$$

$$T_f = (R_{lo} + R_{ext} + R_g) \left[\frac{Q_{gd}}{V_{pl}} + \frac{Q_{pl} - Q_{th}}{0.5(V_{pl} + V_{th})} \right] \quad (4.4)$$

At a switching frequency of $f_s=1\text{MHz}$, input voltage of $V_{in}=12\text{V}$, load current of $I_o=30\text{A}$ and using an IRF6617 HS MOSFET with $V_{pl}=3\text{V}$, $V_{th}=1.85\text{V}$, $Q_{gd}=4\text{nC}$, $Q_{pl}=4\text{nC}$ and $Q_{th}=2\text{nC}$, switching loss as a function of gate current, I_{gl} for a current source driver is given in Figure 4.14 using (4.1) and (4.2). With current source drive, switching loss is inversely proportional to gate current. In addition, in the example given, the HS MOSFET switching loss is reduced from over

2W at 1A gate current to under 1W at 2.5A gate current. For a conventional driver, such as the UCC27222 with $R_{hl}=R_{lo}=1.82\Omega$, $R_{ext}=0\Omega$, $R_g=1\Omega$ and $V_{cc}=6V$, using (4.1)-(4.4), the total HS MOSFET switching loss is 2.1W, with $T_r=5.3ns$ and $T_f=6.1ns$. Therefore, it is clear that a current source driver can reduce the switching loss by providing a gate current greater than 1A.

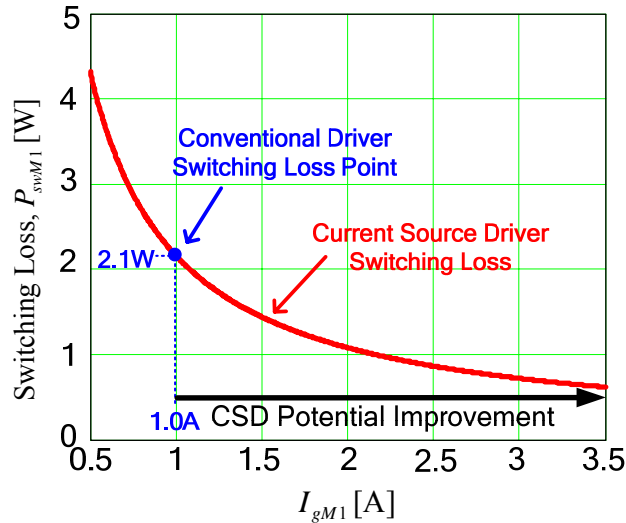


Figure 4.14 Example synchronous buck VR HS MOSFET switching loss as a function of gate current with current source drive

4.3.2 Reduced Impact of HS Driver Common Source Inductance on Switching Loss

Common source inductance, L_{s1} , is parasitic inductance at the source terminal of the power MOSFET that is also in series with the gate circuit loop. This inductance is primarily due to the MOSFET lead inductance and printed circuit board trace. It has the detrimental effect of reducing the gate charging and discharging current. The equivalent drive circuit during turn on under voltage source drive with L_{s1} is illustrated in Figure 4.15. In the plateau region during turn on, i_{ds} increases leading to an induced voltage of $L_{s1}di_{ds}/dt$ adding to the plateau voltage, V_{pl} , and therefore reducing the gate charging current as given by (4.5). The decrease in charging and discharging current tends to increase the rise and fall times, therefore increasing switching loss.

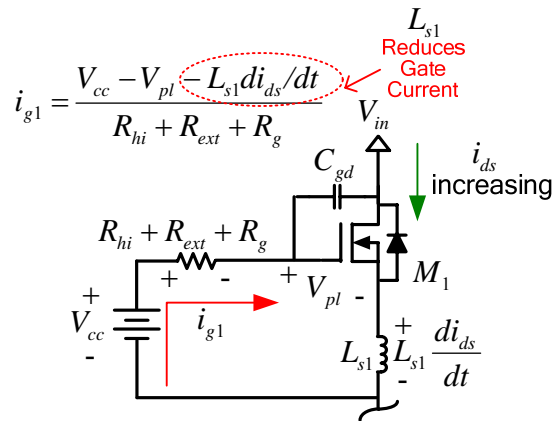


Figure 4.15 Conventional driver equivalent circuit during the plateau region of turn on with common source inductance

$$i_{g1} = \frac{V_{cc} - V_{pl} - L_{s1} \frac{di_{ds}}{dt}}{R_{hi} + R_{ext} + R_g} \quad (4.5)$$

With current source drive, the back voltage due to the common source inductance does not reduce the gate current since the gate current is generated by the current source. To illustrate this point, the equivalent circuit during turn on with current source drive is given in Figure 4.16. Since current source with magnitude I_{g1} charges the C_{gd} capacitance, the gate-source can remain fixed at the plateau, but the $L_{s1} di_{ds}/dt$ back voltage does not increase the rise or fall times.

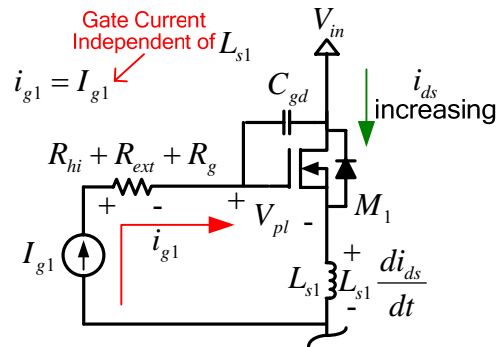


Figure 4.16 Conventional driver equivalent circuit during the plateau region of turn on with common source inductance

4.3.3 Reduced SR Body Diode Conduction

The potential for switching loss reduction through quick switching has been demonstrated.

With adequate dead time, the SR does not have switching loss since the body diode will conduct at turn on and turn off of the HS MOSFET. However, quick switching can be beneficial for the SR to minimize conduction loss. As the gate-source voltage rises from the plateau voltage to V_{cc} , the R_{dson} of the SR is decreasing. Quick switching enables a fast transition to the minimum value of R_{dson} at $v_{gs}=V_{cc}$. A plot of R_{dson} as a function of v_{gs} from the IRF6691 power MOSFET datasheet has been included in Figure 4.17. It is clear that as v_{gs} is increased from the plateau voltage (approximately 3-3.5V), the R_{dson} decreases dramatically. Therefore, it is desirable to drive v_{gs} from the plateau to the final value of V_{cc} (i.e. 5-10V) as quickly as possible to minimize the conduction loss during the time when v_{gs} is 3-5V. As an added benefit of quick switching, dead time can be further minimized as the slopes of the gate-source voltage waveforms increase.

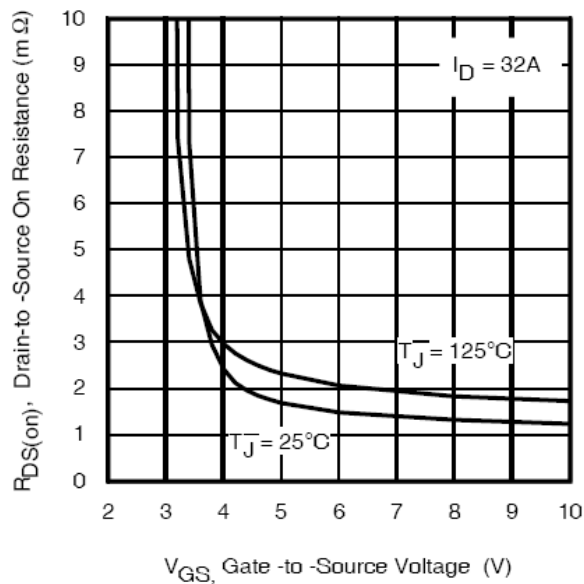


Figure 4.17 IRF6691 R_{dson} as a function of gate-to-source voltage (source: www.irf.com)

4.3.4 SR Gate Energy Recovery

Current source drivers use an inductor to store energy, which can be recovered to the driver supply voltage rail. In the proposed driver, the inductor returns its stored energy to the line during intervals t_2-t_3 and t_6-t_7 for the HS MOSFET, M_1 . Energy is also returned to the driver

supply during the corresponding time intervals for the SR. However, additional energy is dissipated in the driver as conduction loss in the switches and inductors and as the gate current increases, the conduction loss increases exponentially. Therefore, there is a tradeoff between switching speed and gate energy recovery.

In a synchronous buck voltage regulator, the HS MOSFET has very low gate charge and associated gate loss, but high switching loss. Therefore, in an optimal design with a current source driver, the objective is to minimize switching loss with high gate current but, this comes at the expense of gate energy recovery.

In contrast, the SR is selected to minimize conduction loss, so it has high gate charge and associated gate loss. In an optimal design with a current source driver, the objective is to find the optimal tradeoff between gate energy recovery and body diode conduction.

4.4 Logic and Level Shift Circuits

In this section the logic and level shift circuits are presented. The logic circuit is needed to generate the gating waveforms for the eight driver switches, S_1 - S_8 , from a single PWM input signal. The level shift circuit is needed to drive the gates of S_1 - S_6 , since their source terminals are floating. The level shift circuit in this chapter permits the use of all N-channel MOSFETs in the driver and the use of a driver supply voltage greater than the 5V supply used in the driver presented in Chapter 3.

4.4.1 Logic Circuit

In order to fine tune the dead time conveniently, in the experimental prototype the logic used to generate the gating signals for S_1 - S_8 was implemented using an Altera MaxII EPM240 complex programmable logic device (CPLD). The logic circuit consists of edge detector (EDn) cells, as illustrated in Figure 4.18 and digital time delay (TDn) cells as illustrated in Figure 4.19. In the

4.20. The waveforms of the proposed driver presented in Figure 4.2 have been re-drawn in Figure 4.21 to include the logic pulse edges, which are noted by the shaded areas in the S_1 - S_8 gating waveforms. The logic circuit takes the PWM waveform as an input and generates the gating signals S_1 - S_4 and S_5 - S_8 using the PWM signal and the EDn and TDn cells.

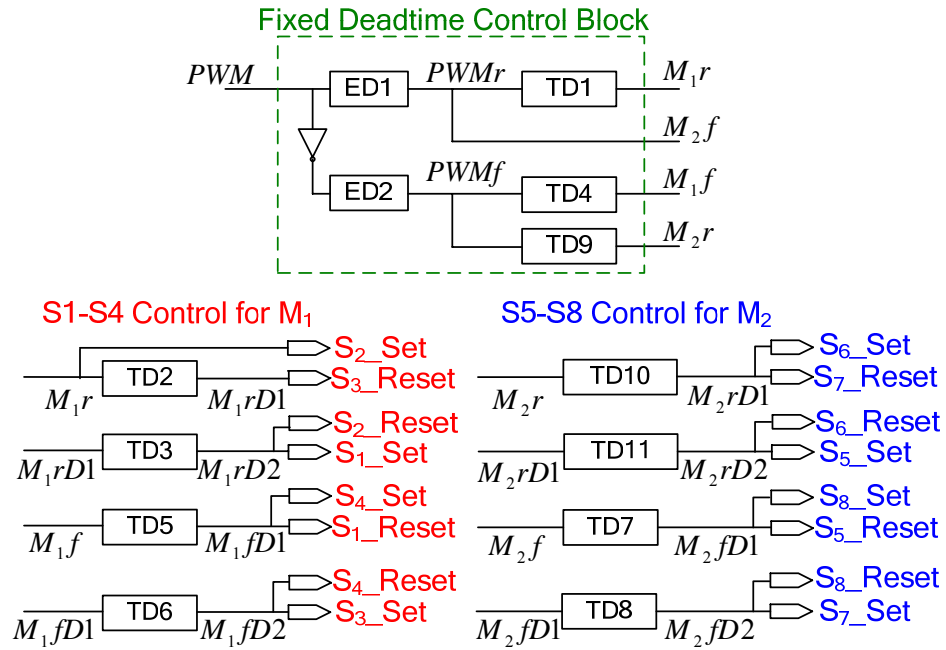


Figure 4.20 Block diagram of logic implementation using the Altera MaxII EPM240

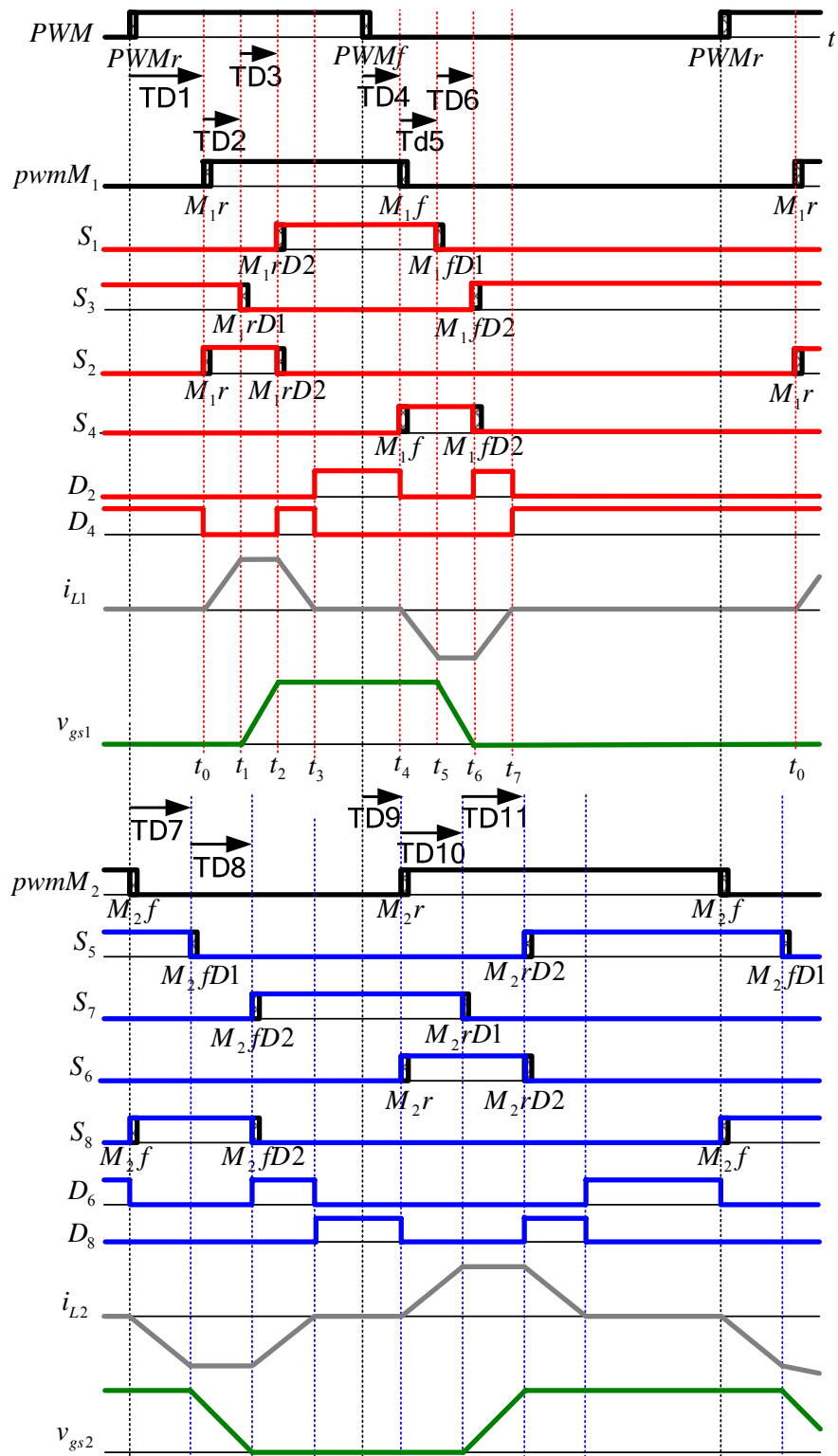


Figure 4.21 Proposed driver waveforms with rising and falling pulse edges for the M_1 and M_2 gating waveforms noted

In the fixed dead time control block, the two edge detectors use the PWM and inverted PWM signals as their inputs in order to generate the $PWMr$ (PWM rising) and $PWMf$ (PWM falling) signals. TDn blocks TD1, TD4 and TD9 are then used to generate the rising and falling edges of the inputs to each driver with appropriate dead time. Then, four time delay blocks are used to generate S_1 - S_4 (for the HS MOSFET, M_1) and four more to generate S_5 - S_8 (for the SR MOSFET, M_2). An internally generated 400MHz asynchronous ring oscillator clock is used for the counter, compare block and edge detector.

The advantage of using a CPLD implementation is that the dead time between the HS and SR gate-source voltages can be controlled by the internally generated clock, so it can be minimized to within 2.5ns. In addition, the CPLD solution occupies a smaller portion of printed circuit board area. 147 gates were used in the CPLD implementation of the logic circuit. If the proposed driver was implemented in an integrated circuit, the logic circuit could easily be integrated in the driver package at a low cost.

4.4.2 Level Shift Circuit

Driver switches S_1 - S_6 in Figure 4.1 are not ground referenced, but referenced to floating voltages, so these small MOSFET switches in the proposed driver require level shift circuits to properly drive their gate-to-source voltages to 5V. A modified version of the pulsed latch level shift circuit presented in [19] was used to drive each of S_1 - S_6 as illustrated in Figure 4.22. The pulsed level-shifter takes the rising and falling edge signals from the CPLD logic circuit as its inputs. In the experimental prototype, FDV301N MOSFETs were used for S_S and S_R , R_1 and R_3 were 150Ω , R_2 and R_4 were 75Ω , NC7SZ00 NAND gates were used and one FMB3946 BJT switch pair was used for Q_1 . The bootstrap diode, D_b , was MBR0540 and the bootstrap capacitor, C_b , was 100nF. A logic supply of $V_{dd}=5V$ was used to power the six level shift circuits for S_1 - S_6 .

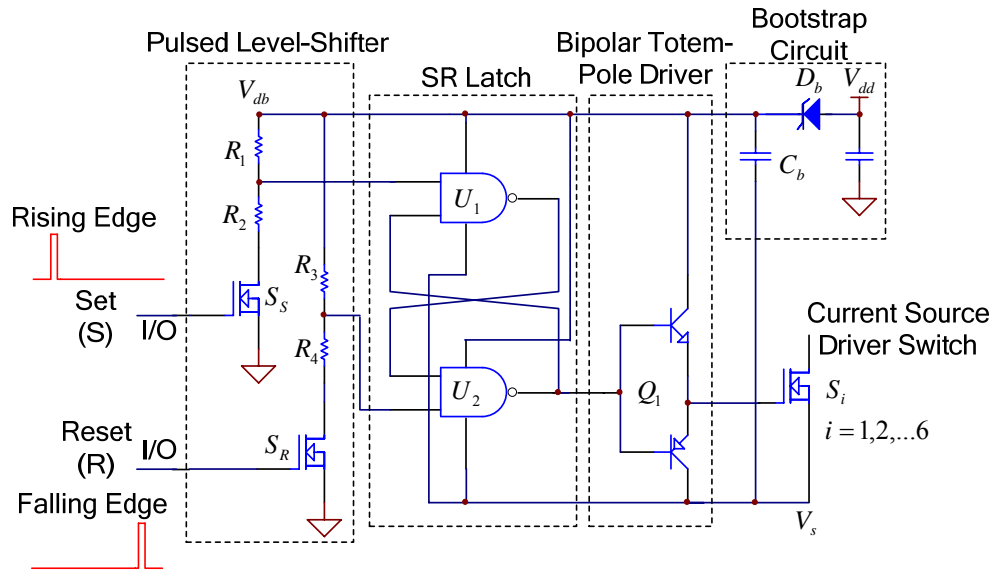


Figure 4.22 Pulsed latch level shift circuit

4.5 Driver Design and Optimization

The design and optimization is presented in this section in order to quantify the tradeoffs discussed in the previous section and enable an optimal design for the HS MOSFET and SR MOSFET in a synchronous buck voltage regulator.

4.5.1 HS MOSFET Driver Design and Optimization

Optimal design of the HS MOSFET current source driver involves a tradeoff between driver loss and switching loss reduction. As illustrated in Figure 4.23, as gate current, I_{gl} , increases, switching loss, P_{swl} , decreases inversely proportionally, while driver loss, P_{drl} , increases linearly. It is noted that P_{drl} increases linearly and not exponentially since as I_{gl} increases, the duration of the conduction loss intervals in the driver decrease inversely proportionally to I_{gl} . The total loss, P_{totl} , is the sum of P_{drl} and P_{swl} . It is clear from the figure that there is an optimal gate current, I_{glopt} , where P_{totl} is minimized at point $P_{totlmin}$. The remainder of this sub-section presents a procedure to derive I_{glopt} in order to achieve an optimal design.

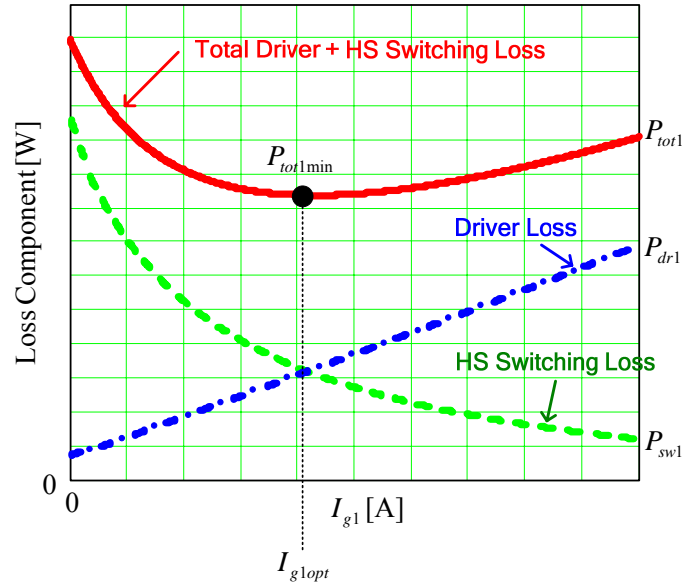


Figure 4.23 Optimization loss curves for the HS MOSFET M_1 as a function of gate current

In the desired operation of the proposed HS driver, during the pre-charge interval, T_{pre1} , the driver inductor current, i_{L1} , is linearly increasing, during the turn on interval, the inductor current is assumed constant at I_{g1} and during the energy return interval, T_{Vcc1} , the inductor current is linearly decreasing.

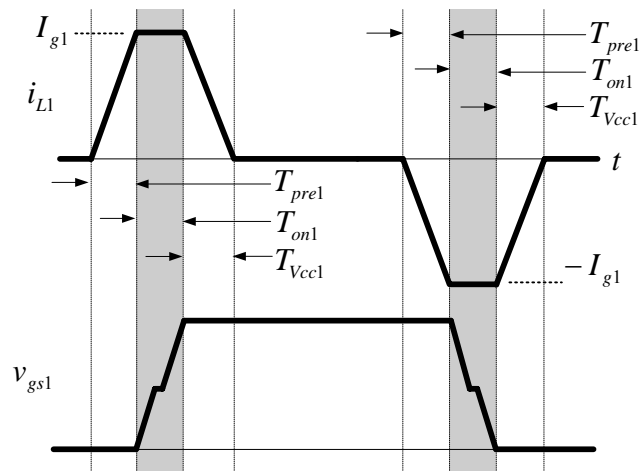


Figure 4.24 Current source driver inductor current (top) and gate-to-source voltage (bottom) piecewise linear waveforms for the HS MOSFET (M_1)

Driver design involves selection of the inductor value, L_1 , or pre-charge time, T_{pre1} for a

given gate current, I_{g1} . The designer has a choice of which variable to define in their design. However, since the range of inductor values is often limited, or if inductor integration in the driver IC is desired, L_l can be selected first.

For a given L_l , assuming linear pre-charging, the inductor current pre-charge time for M_l , T_{pre1} , can be calculated using (4.6). Equation (4.6) is valid provided (4.7) is satisfied as explained in Chapter 3 section 3.4.2.1. In (4.7), $R_{pre1}=R_{dsS2}+R_{Ll}+R_{dsS3}$, R_{dsS2} represents the on resistance of driver switch S_2 , R_{dsS3} represents the on resistance of driver switch S_3 and R_{Ll} represents the winding resistance of L_l .

$$T_{pre1} = \frac{L_l I_{g1}}{V_{cc}} \quad (4.6)$$

$$T_{pre1} < \frac{1}{4} \frac{L_l}{R_{pre1}} \quad (4.7)$$

The two driver loss components that are gate current dependent are conduction loss and turn off switching loss in S_2 and S_4 . These losses are calculated as follows.

It was demonstrated in Chapter 3 section 3.6, that the greatest source of loss in the current source driver is conduction loss. For the HS MOSFET driver, the conduction loss, $P_{drcond1}$, is given by (4.8) assuming four identical driver switches are used. In (4.8), V_F represents the diode forward voltage drop of the body diodes of S_2 and S_4 , Q_{g1} represents the total gate charge of M_l driven at V_{cc} volts.

$$P_{drcond1} = 2 \left[\left(I_{g1}^3 \left(\frac{R_{pre1}}{3V_{cc}} + \frac{R_{pre1}}{3(V_{cc} + V_F)} \right) + I_{g1}^2 \frac{V_F}{2(V_{cc} + V_F)} \right) L_l + I_{g1} R_{on1} Q_{g1} \right] f_s \quad (4.8)$$

S_2 and S_4 turn off at I_{g1} . The turn off loss in S_2 and S_4 is given by (4.9) where the fall times, T_{f2} and T_{f4} can be obtained from the MOSFET data sheets.

$$P_{offS2-S4} = \frac{1}{2} V_{cc} I_{g1} (T_{f2} + T_{f4}) f_s \quad (4.9)$$

The total gate current dependent loss in the HS MOSFET driver is the sum of $P_{drcond1}$ and $P_{offS2-S4}$ as given by (4.10).

$$P_{dr1} = P_{drcond1} + P_{offS2-S4_s} \quad (4.10)$$

Using (4.1) and (4.2), the switching loss in M_1 can be approximated by (4.11).

$$P_{sw1} \approx V_{in} I_o \left(\frac{Q_{gd1} + Q_{pl1} - Q_{th1}}{|I_{g1}|} \right) f_s \quad (4.11)$$

The total gate current dependent losses for the HS MOSFET M_1 are the sum of P_{dr1} and P_{sw1} as given by (4.12).

$$P_{tot1} = P_{dr1} + P_{sw1} \quad (4.12)$$

Since P_{tot1} has a minimum value, it is possible to derive a closed form expression for I_{g1opt} by deriving P_{tot1} with respect to I_{g1} , setting the derivative equal to zero and solving for I_{g1} , however I_{g1opt} can also easily be found by plotting a curve of P_{dr1} vs. I_{g1} .

4.5.2 SR MOSFET Driver Design and Optimization

Optimal design of the SR MOSFET current source driver involves a tradeoff between driver loss and body diode conduction. As illustrated in Figure 4.25, as I_{g2} increases, body diode conduction, P_{BD2} , decreases inversely proportionally, while driver loss, P_{dr2} , increases linearly. The total loss, P_{tot2} , is the sum of P_{dr2} and P_{BD2} . It is clear from the figure that there is an optimal gate current, I_{g2opt} , where P_{tot2} is minimized at point $P_{tot2min}$. The remainder of this sub-section presents a procedure to derive I_{g2opt} in order to achieve an optimal design.

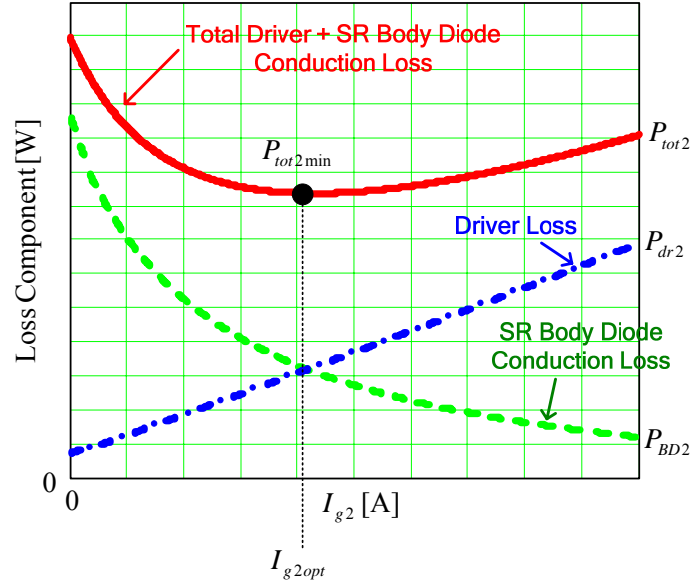


Figure 4.25 Optimization loss curves for the SR MOSFET M_2 as a function of gate current

Following the procedure in the previous sub-section, for a given L_2 , assuming linear pre-charging, the inductor current pre-charge time for M_2 , T_{pre2} , can be calculated using (4.13).

$$T_{pre2} = \frac{L_2 I_{g2}}{V_{cc}} \quad (4.13)$$

For the SR MOSFET driver, the conduction loss, $P_{drcondM2}$ is given by (4.14), assuming four identical driver switches are used. In (4.14), Q_{g2} represents the total gate charge of M_2 , $R_{pre2} = R_{dsS6} + R_{L2} + R_{dsS7}$, R_{dsS6} represents the on resistance of driver switch S_6 , R_{dsS3} represents the on resistance of driver switch S_7 and R_{L2} represents the winding resistance of L_2 .

$$P_{drcond2} = 2 \left[\left(I_{gM2}^3 \left(\frac{R_{pre2}}{3V_{cc}} + \frac{R_{pre2}}{3(V_{cc} + V_F)} \right) + I_{g2}^2 \frac{V_F}{2(V_{cc} + V_F)} \right) L_2 + I_{g2} R_{on2} Q_{g2} \right] f_s \quad (4.14)$$

S_6 and S_8 turn off at I_{g2} . The turn off loss in S_6 and S_8 is given by (4.15) where the fall times, T_{f6} and T_{f8} are obtained from the MOSFET data sheets.

$$P_{offS6-S8} = \frac{1}{2} V_{cc} I_{g2} (T_{f6} + T_{f8}) f_s \quad (4.15)$$

The total gate current dependent loss in the SR MOSFET driver is the sum of $P_{drcond2}$ and $P_{offS2-S4}$ as given by (4.16).

$$P_{dr2} = P_{drcond2} + P_{offS6-S8} \quad (4.16)$$

SR body diode conduction occurs during the turn on and turn off switching transitions of the M_1 . As an approximation, it can be assumed that the body diode conduction occurs during the interval when the gate-to-source voltage of M_2 transitions between V_{pl2} and zero as illustrated in Figure 4.26.

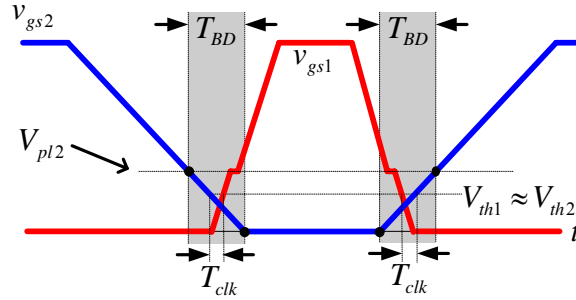


Figure 4.26 Gate-to-source voltage waveforms of M_1 and M_2 during the switching transitions illustrating the body diode conduction times, T_{BD}

Using the waveform approximations in Figure 4.26, T_{BD} occurs during the transitions when v_{gs2} is charged to V_{pl2} and discharged from V_{pl2} to zero. Therefore, T_{BD} is approximated by (4.17), where Q_{pl2} represents the gate charge at the gate plateau voltage. In (4.17) it is assumed that the dead time has been minimized to one clock period, T_{clk} , of the CPLD dead time controller.

$$T_{BD} = \frac{Q_{pl2}}{I_{g2}} \quad (4.17)$$

The body diode conduction loss can be estimated using (4.18), where V_{F_2} represents the forward voltage drop of the SR body diode, and T_{BD} represents the body diode conduction time at turn on and turn off.

$$P_{BD2} = 2V_{F_2}I_oT_{BD}f_s \quad (4.18)$$

The total gate current dependent losses for the SR MOSFET M_2 are the sum of P_{dr2} and P_{BD2}

as given by (4.19).

$$P_{tot2} = P_{dr1} + P_{BD2} \quad (4.19)$$

4.6 Design Example

This section includes design examples for the HS MOSFET driver for M_1 and SR MOSFET driver, for M_2 .

4.6.1 HS MOSFET Driver Design Example

A design of the HS MOSFET current source driver was completed using the procedure outlined in section 4.5.1. The parameters for the design are given in Table 4.1. An inductor value of 68nH was selected for L_1 .

Table 4.1 HS MOSFET Current source driver design parameters

Circuit Parameters	
Switching Frequency, f_s	1MHz
Gate Drive Voltage, V_{cc}	10V
Load Current, I_o	30A
Input Voltage, V_{in}	12V
MOSFET, M_1	IRF6617
Total Gate Charge, Q_{gl}	20nC
Internal Gate Resistance, R_{gl}	1 Ω
Gate Charge at V_{pl1} , Q_{pl1}	4nC
Gate Charge at V_{th1} , Q_{th1}	2nC
Gate-Drain Charge, Q_{gd1}	4nC
Driver Switches, $S_1 - S_4$	NDS351AN
Diode Forward Voltage, V_F	0.7V
$R_{dsS1}-R_{dsS4}$	140m Ω
Fall Time, T_{f2} , T_{f4}	1ns
Driver Inductor, L_1	1812SMS-68N
Inductor Value, L_1	68nH
Driver Inductor Resistance, R_{L1}	20m Ω

Using the values in Table 4.1, along with (4.8)-(4.12), the loss curves for the driver, P_{dr1} , switching loss, P_{sw1} and total gate current dependent loss, P_{tot1} are given in Figure 4.27. The minimum power loss point, $P_{tot1min}$ corresponds to a gate current of $I_{g1opt}=3.25A$, enabling the pre-charge inductor current to be calculated as 20ns using (4.6).

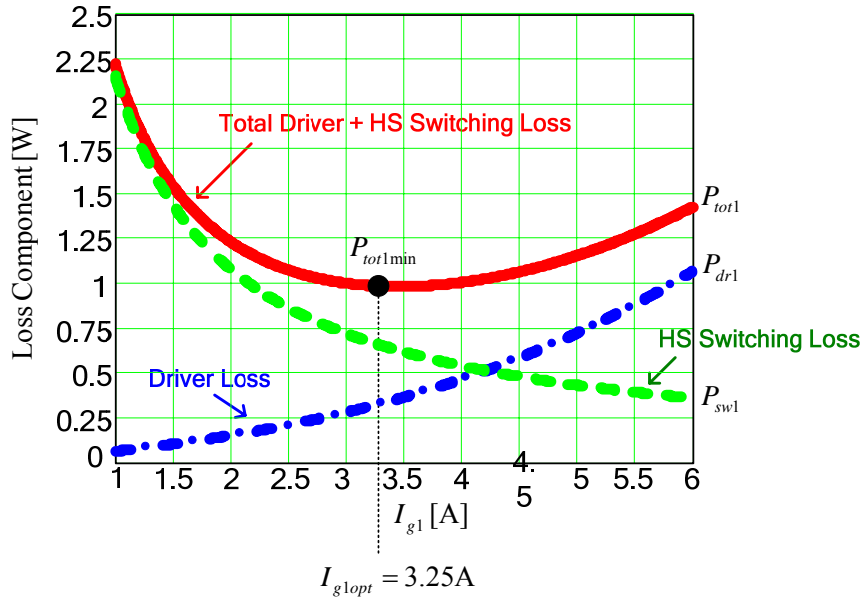


Figure 4.27 Optimization curves for the control MOSFET M_1 ; power loss vs. gate current, I_{g1}

4.6.2 SR MOSFET Driver Design Example

A design of the SR MOSFET current source driver was completed using the procedure outlined in section 4.5.2. The parameters for the design are given in Table 4.2. An inductor value of 307nH was selected for L_2 .

Using the values in Table 4.2, along with (4.14)-(4.19), the loss curves for the driver, P_{dr2} , body diode conduction loss, P_{BD2} and total gate current dependent loss, P_{tot2} are given in Figure 4.28. The minimum power loss point, $P_{tot2min}$ corresponds to a gate current of $I_{g1opt}=1.3A$, enabling the pre-charge inductor current to be calculated as 40ns using (4.13).

Table 4.2 SR MOSFET Current source driver design parameters

Circuit Parameters	
Switching Frequency, f_s	1MHz
Gate Drive Voltage, V_{cc}	10V
Load Current, I_o	30A
Input Voltage, V_{in}	12V
MOSFET, M_2	IRF6691
Total Gate Charge, Q_{g2}	60nC
Internal Gate Resistance, R_{g2}	1 Ω
Gate Charge at V_{pl2} , Q_{pl2}	18nC
Diode Forward Voltage, $V_{F,2}$	0.5V
Driver Switches, $S_1 - S_4$	NDS351AN
Diode Forward Voltage, V_F	0.7V
$R_{dsS5}-R_{dsS8}$	140m Ω
Fall Time, $T_{f\beta}, T_{f\delta}$	1ns
Driver Inductor, L_2	132-16SM
Inductor Value, L_2	307nH
Driver Inductor Resistance, R_{L2}	70m Ω

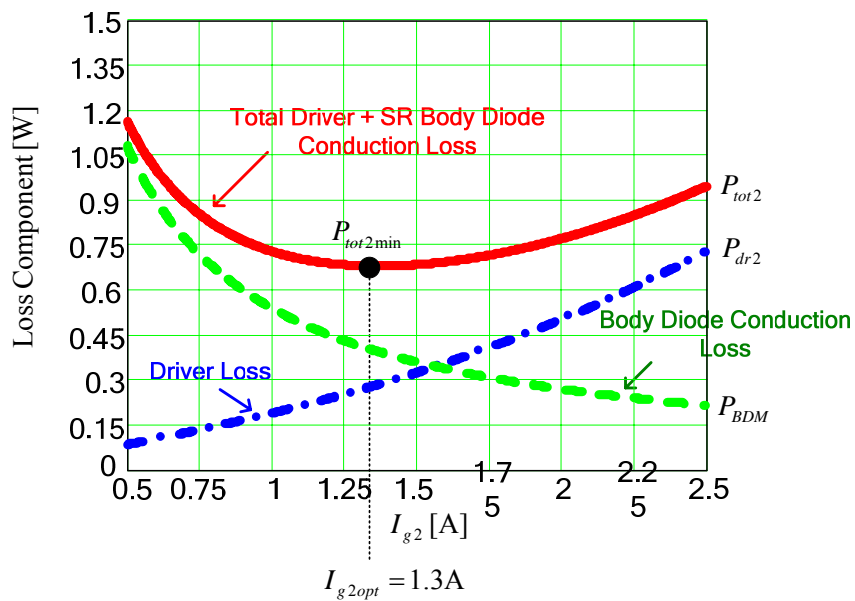


Figure 4.28 Optimization curves for the SR MOSFET M_2 ; power loss vs. gate current, I_{g2}

4.7 Experimental Results

In this section, experimental results are presented to compare the proposed VR with current source gate driver to a benchmark synchronous buck VR with conventional driver.

4.7.1 Driver and Circuit Parameters

A prototype of the synchronous buck converter with current source gate driver was built on a 6 layer printed circuit board (PCB) as shown in the photo in Figure 4.29. The driver was built using discrete components with an Altera MaxII EPM240 CPLD used to generate the control signals. Circuit, driver and MOSFET parameters from Table 4.1 and Table 4.2 in section 4.6 were used. The buck inductor was IHLP5050FD, 330nH from Vishay. Load voltages were tested at 1.5V, 1.3V, 1.2V and 1.0V up to a full load current of $I_o=30A$. The output voltage was regulated within $\pm 30mV$ of the nominal value using a function generator with 1ns resolution control of the duty cycle. The proposed synchronous buck with current source gate driver was compared to an identical synchronous buck with the conventional UCC27222 driver from Texas Instruments as the benchmark. A photo of the synchronous buck with conventional driver is given in Figure 4.30. The powertrain components and layout were the same for the two circuits.

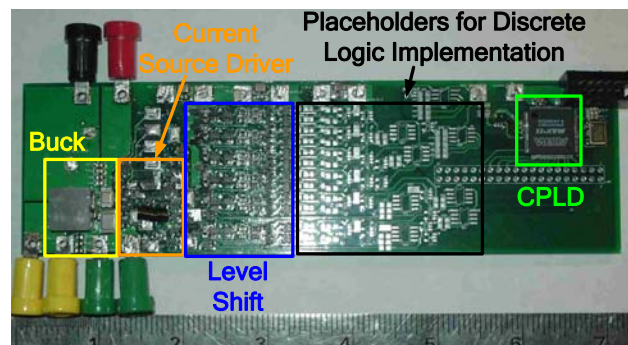


Figure 4.29 Photo of the proposed synchronous buck VR with current source gate driver prototype

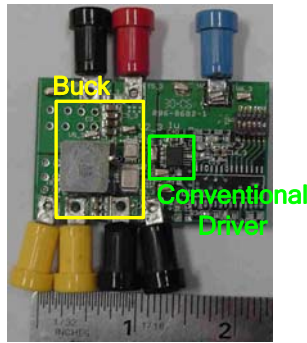


Figure 4.30 Photo of the benchmark conventional voltage source driver prototype

4.7.2 Driver Operation

Waveforms of v_{gs1} , v_{gs2} and i_{L1} for the proposed synchronous buck VR with current source driver are given in Figure 4.31 for 1MHz switching frequency operation. The waveforms illustrate the turn on and turn off switching transitions of M_1 . It is noted that the gate-to-source waveforms rise and fall with constant linear slopes due to the constant current source drive (at the peak inductor current) and the inductor current is discontinuous as expected. The inductor current used to charge the gate at turn on is 2.9A and at turn off is -3.2A used to discharge the gate. The inductor pre-charge time, T_{pre1} , is 20ns as designed in section 4.6.1. The turn on time, T_{on1} , (for the v_{gs1} transition from 0 to V_{cc}) is approximately 6ns and the turn off time, T_{off1} , (for the v_{gs1} transition from V_{cc} to 0) is approximately 5ns.

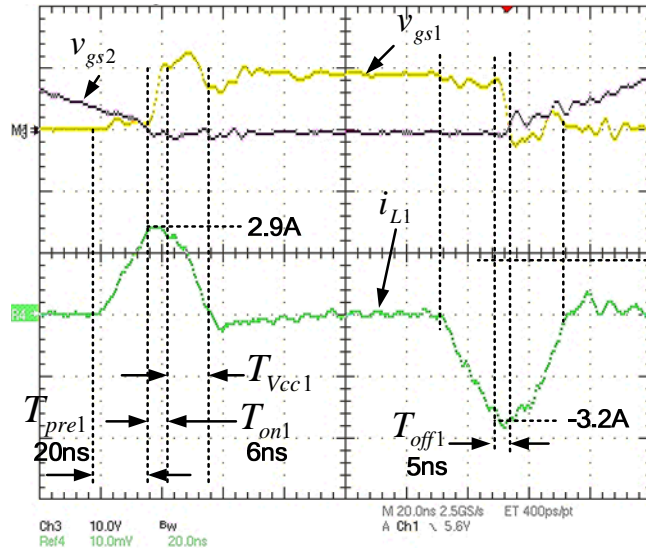


Figure 4.31 Top: Current source driver HS MOSFET (M_1) and SR (M_2) gate-to-source voltages at 1MHz (Y-axis: 10V/div and X-axis 20ns/div); Bottom: M_1 current source driver inductor current (Y-axis: 2A/div)

Waveforms of v_{gs1} , v_{gs2} and i_{L2} for the proposed synchronous buck VR with current source driver are given in Figure 4.32 for 1MHz switching frequency operation. The inductor current used to charge the gate of the SR, M_2 , at turn on is 1.3A and at turn off is -1.3A used to discharge the gate. The inductor pre-charge time, T_{pre2} , is 40ns as designed in section 4.6.2. The turn on time, T_{on2} , (for the v_{gs1} transition from 0 to V_{cc}) is approximately 50ns and the turn off time, T_{off2} , (for the v_{gs2} transition from V_{cc} to 0) is also approximately 50ns.

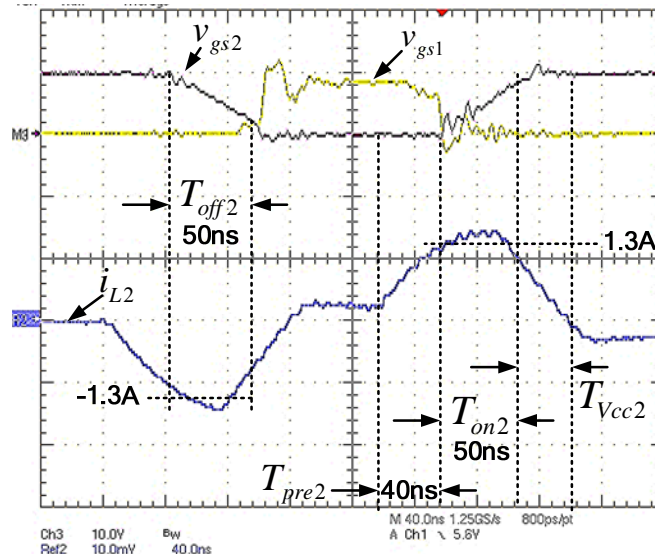


Figure 4.32 Top: Current source driver HS MOSFET (M_1) and SR (M_2) gate-to-source voltages at 1MHz (Y-axis: 10V/div and X-axis 40ns/div); Bottom: M_2 current source driver inductor current (Y-axis: 1A/div)

A waveform of v_{gs1} for the synchronous buck VR with conventional UCC27222 driver is given in Figure 4.33 illustrating the turn on and turn off switching transitions of M_1 . The measurement was taken at $V_o=1.3V$, $V_{in}=12V$ and $I_o=20A$. The rise and fall times cannot be accurately measured since the common source inductance voltage is included in the probed measurement, however the turn off plateau is clearly evident. The measured fall time is approximately 8ns.

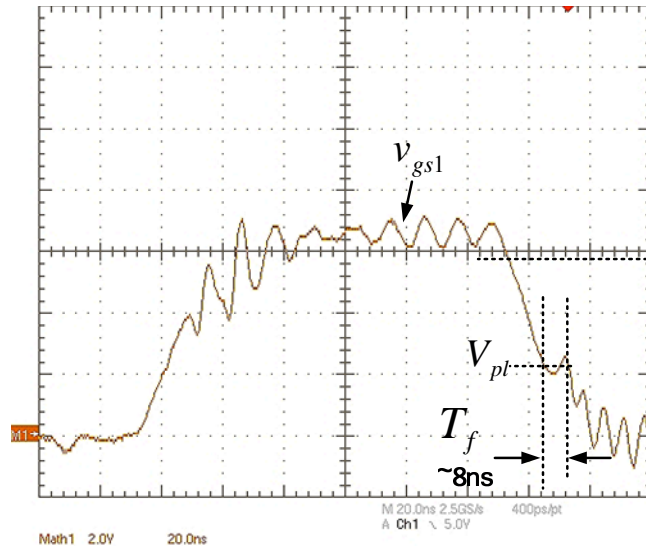


Figure 4.33 Synchronous buck VR with UCC27222 driver HS MOSFET (M_1) gate-to-source voltage at 1MHz (Y-axis: 2V/div and X-axis 20ns/div)

A waveform of v_{gsM1} for the synchronous buck VR with the proposed current source driver is given in Figure 4.34 illustrating the turn on and turn off switching transitions of M_1 . The measurement was taken at $V_o=1.3V$, $V_{in}=12V$ and $I_o=20A$. The measured fall time is approximately 4ns, which is half of the fall time for the UCC27222 driver implying that the turn off switching loss is reduced by half with the current source driver.

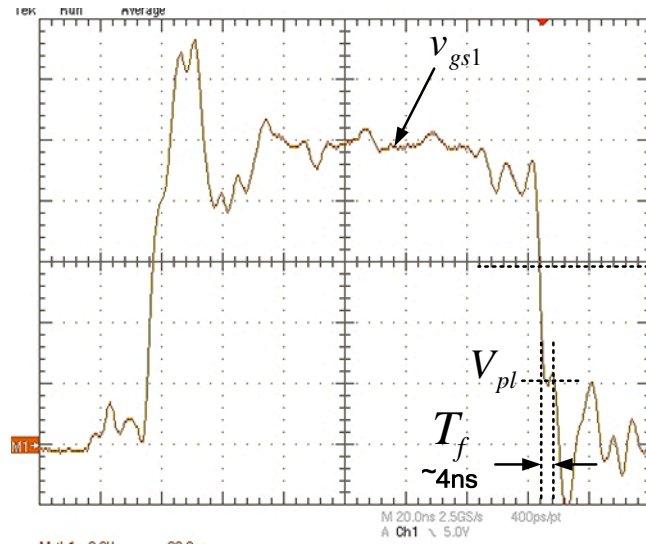


Figure 4.34 Synchronous buck VR with current source driver HS MOSFET (M_1) gate-to-source voltage at 1MHz (Y-axis: 2V/div and X-axis 20ns/div)

4.7.3 Efficiency and Losses at 1.5V Output

The efficiency as a function of load is given in Figure 4.35 for the synchronous buck VR with current source driver and synchronous buck VR with UCC27222 driver at 1MHz switching frequency and 1.5V output. The converter with current source driver achieved an efficiency of 87.5% at 15A load and 83.3% at 30A load, compared to 85.2% and 79.4%, respectively for the UCC27222 driver.

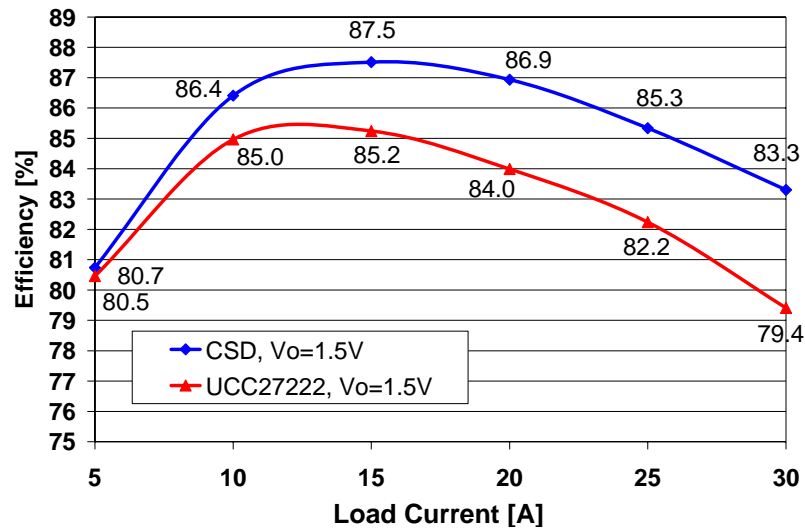


Figure 4.35 Efficiency as a function of load for the current source gate driver and UCC27222 gate driver at 1.5V output and 1MHz switching frequency

The total power loss including powertrain and gate drive loss for both converters is given in Figure 4.36. The loss reduction of the single phase VR with the current source driver with respect to the VR with UCC27222 driver are illustrated in Figure 4.37. It is noted that at 30A load, the proposed current source gate driver saves 2.6W, or 21.9% compared to the UCC27222 conventional driver. This loss reduction is significant for a multi-phase VR. For example, in a five phase VR, the total loss reduction would be 13W.

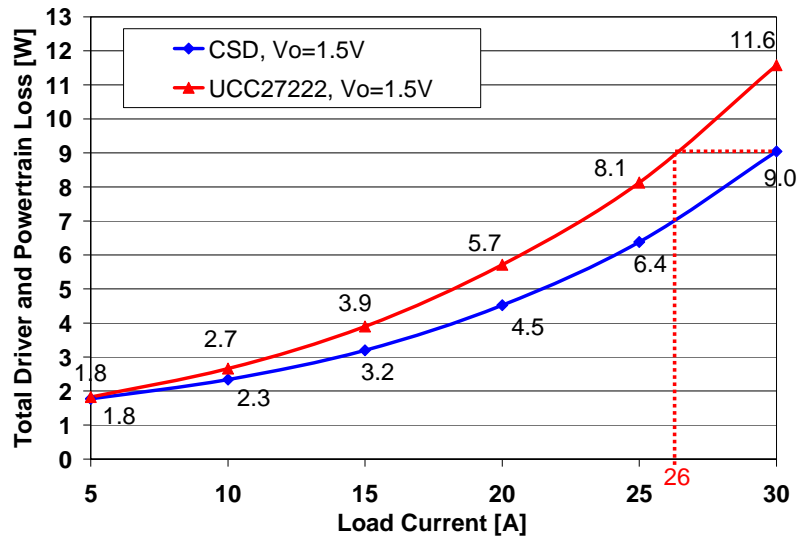


Figure 4.36 Total measured loss as a function of load for the current source gate driver and UCC27222 gate driver at 1.5V output and 1MHz switching frequency

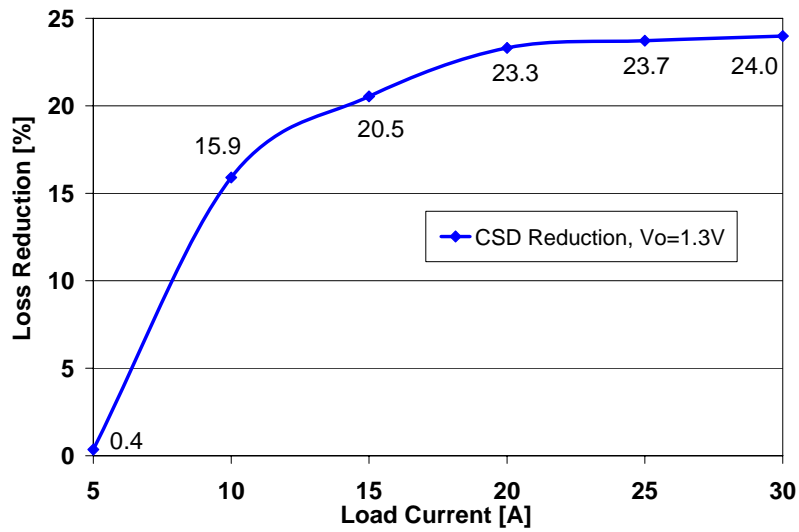


Figure 4.37 Loss reduction as a function of load for the current source gate driver with respect to the UCC27222 gate driver at 1.5V output and 1MHz switching frequency

Another interesting observation is that if the power loss per phase is limited to 9W, the Buck converter with conventional gate drive can only provide 26A output current, while the Buck converter with current source gate driver can provide 30A (an improvement of 15%). In other words, if the total output current is 120A, we need 5 phases ($120A/26A$ per phase=4.6 phases) for

the conventional gate driver and only 4 phases (120A/30A per phase) for the current source gate driver. This will yield a significant cost savings.

4.7.4 Efficiency and Losses at 1.3V Output

The efficiency as a function of load is given in Figure 4.38 for the synchronous buck VR with current source driver and the synchronous buck VR with UCC27222 driver at 1MHz switching frequency and 1.3V output. The converter with current source driver achieved an efficiency of 86.6% at 15A load and 81.9% at 30A load, compared to 83.8% and 77.5%, respectively for the UCC27222 driver.

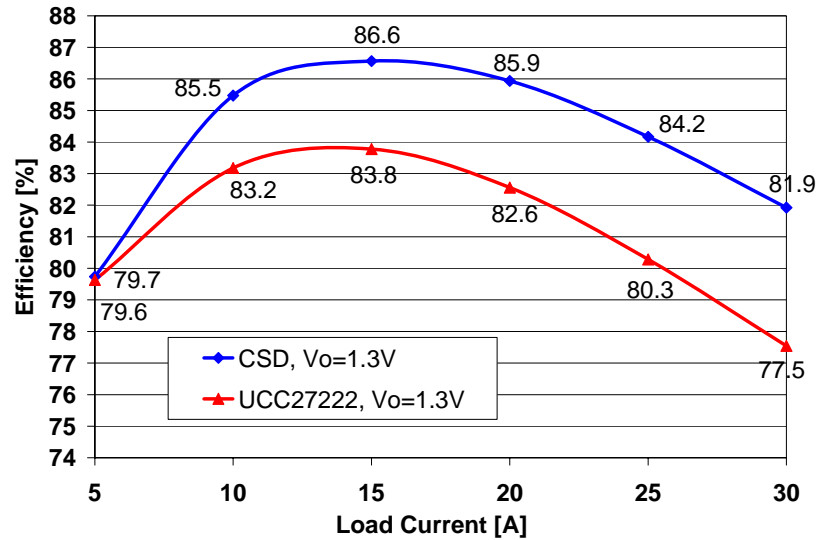


Figure 4.38 Efficiency as a function of load for the current source gate driver and UCC27222 gate driver at 1.3V output and 1MHz switching frequency

The total power loss including powertrain and gate drive loss for both converters is given in Figure 4.39. The loss reduction of the single phase VR with the current source driver with respect to the VR with UCC27222 driver are illustrated in Figure 4.40. It is noted that at 30A load, the proposed current source gate driver saves 2.7W, or 24.0% compared to the UCC27222 conventional driver. This loss reduction is significant for a multi-phase VR. For example, in a five phase VR, the total loss reduction would be 13.5W.

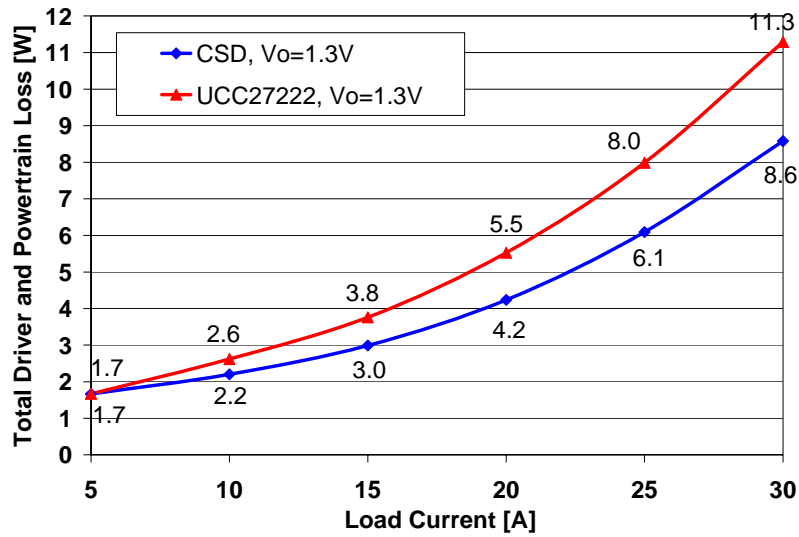


Figure 4.39 Total measured loss as a function of load for the current source gate driver and UCC27222 gate driver at 1.3V output and 1MHz switching frequency

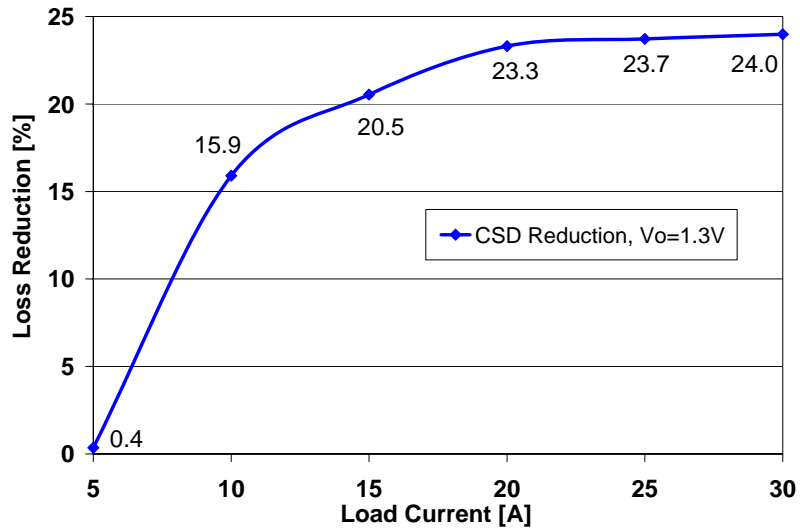


Figure 4.40 Loss reduction as a function of load for the current source gate driver with respect to the UCC27222 gate driver at 1.3V output and 1MHz switching frequency

4.7.5 Efficiency and Losses at 1.2V Output

The efficiency as a function of load is given in Figure 3.37 for the synchronous buck VR with current source driver and the synchronous buck VR with UCC27222 driver at 1MHz switching frequency and 1.2V output. The converter with current source driver achieved an

efficiency of 85.5% at 15A load and 80.5% at 30A load, compared to 82.5% and 73.1%, respectively for the UCC27222 driver.

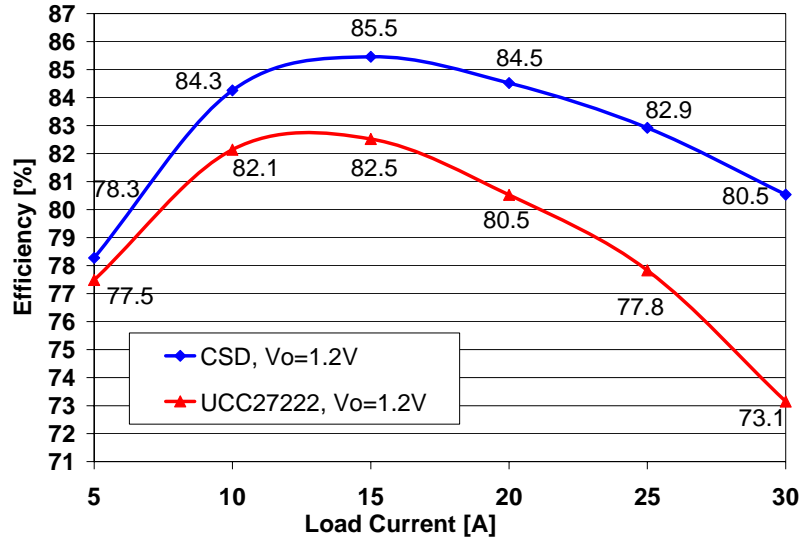


Figure 4.41 Efficiency as a function of load for the current source gate driver and UCC27222 gate driver at 1.2V output and 1MHz switching frequency

The total power loss including powertrain and gate drive loss for both converters is given in Figure 4.42. The loss reduction of the single phase VR with the current source driver with respect to the VR with UCC27222 driver are illustrated in Figure 4.43. It is noted that at 30A load, the proposed current source gate driver saves 4.5W, or 34.0% compared to the UCC27222 conventional driver. This loss reduction is significant for a multi-phase VR. For example, in a five phase VR, the total loss reduction would be 22.5W.

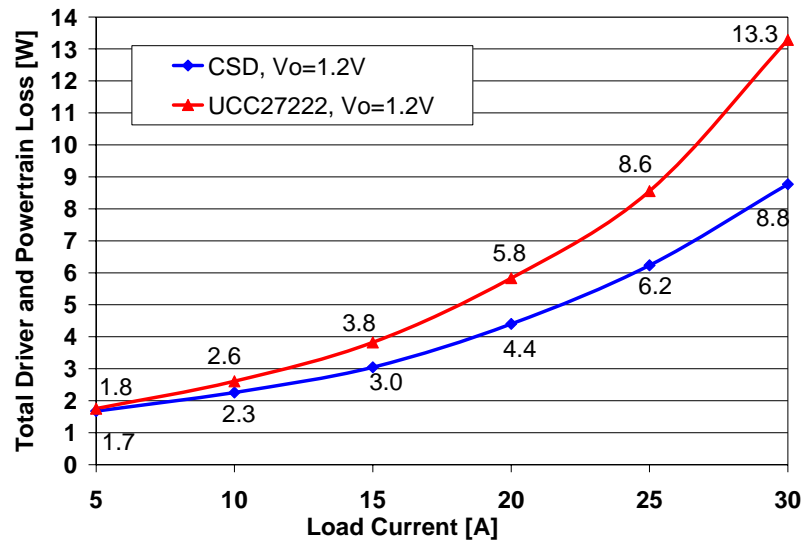


Figure 4.42 Total measured loss as a function of load for the current source gate driver and UCC27222 gate driver at 1.2V output and 1MHz switching frequency

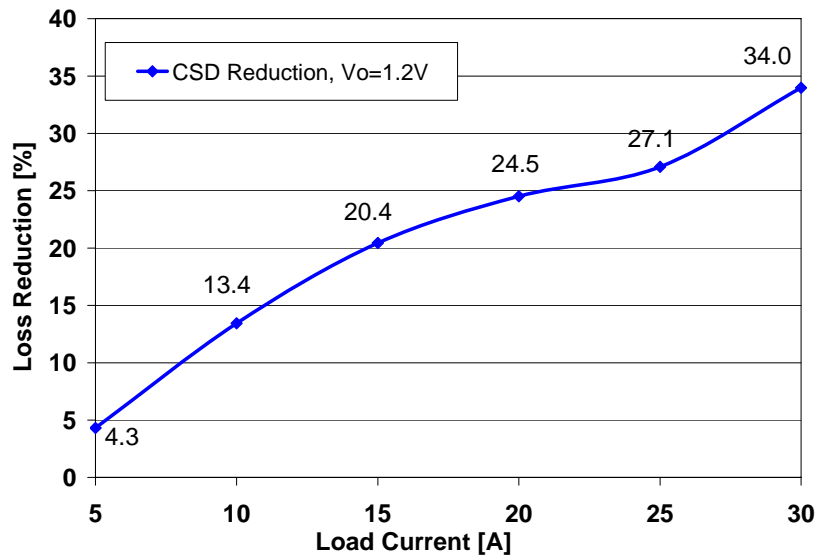


Figure 4.43 Loss reduction as a function of load for the current source gate driver with respect to the UCC27222 gate driver at 1.2V output and 1MHz switching frequency

4.7.6 Efficiency and Losses at 1.0V Output

The efficiency as a function of load is given in Figure 4.44 for the synchronous buck VR with current source driver and the synchronous buck VR with UCC27222 driver at 1MHz switching frequency and 1.0V output. The converter with current source driver achieved an

efficiency of 83.3% at 15A load and 79.6% at 30A load, compared to 77.2% and 71.4%, respectively for the UCC27222 driver.

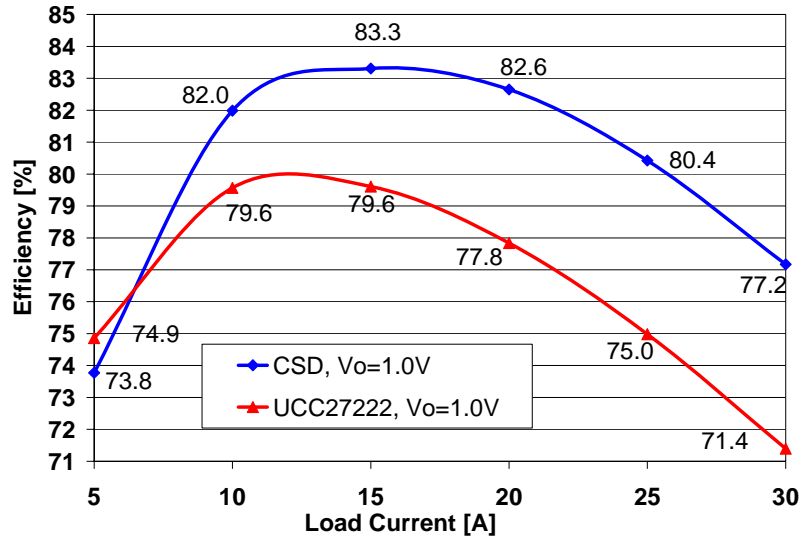


Figure 4.44 Efficiency as a function of load for the current source gate driver and UCC27222 gate driver at 1.0V output and 1MHz switching frequency

The total power loss including powertrain and gate drive loss for both converters is given in Figure 4.45. The loss reduction of the single phase VR with the current source driver with respect to the VR with UCC27222 driver are illustrated in Figure 4.46. It is noted that at 30A load, the proposed current source gate driver saves 3.4W, or 27.6% compared to the UCC27222 conventional driver. This loss reduction is significant for a multi-phase VR. For example, in a five phase VR, the total loss reduction would be 17W.

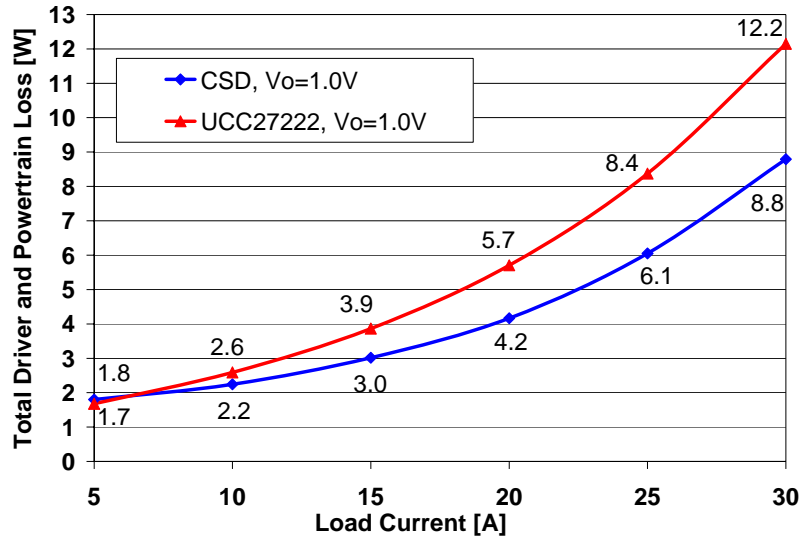


Figure 4.45 Total measured loss as a function of load for the current source gate driver and UCC27222 gate driver at 1.0V output and 1MHz switching frequency

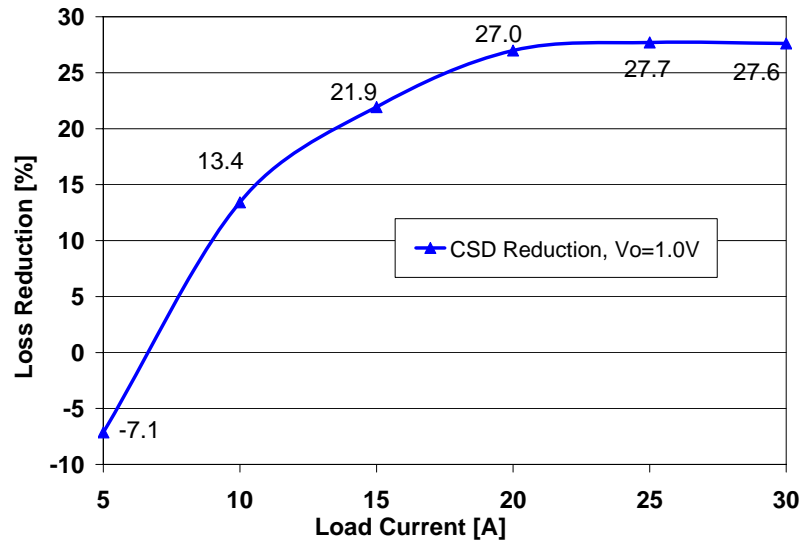


Figure 4.46 Loss reduction as a function of load for the current source gate driver with respect to the UCC27222 gate driver at 1.0V output and 1MHz switching frequency

4.7.7 Comparison with Other High Efficiency Voltage Regulators

An efficiency comparison of state of the art 12V input VRs operating at 1MHz and 1.5V output is provided in Table 4.3. The proposed current source driver achieves an efficiency of 87.3% compared to 84% for the tapped-inductor buck converter in [57] at 12.5A. It is also noted

that an efficiency improvement of 1.9% is achieved in comparison to the Toshiba synchronous buck Multi Chip Module using a semiconductor integration approach.

The semiconductor integration approach has a significant advantage since the parasitic inductance of the package leads between the buck HS and SR MOSFETs is negligible. The potential reduction using this type of technology is apparent from the proposed switching loss model calculations in Chapter 4, Figure 5.19(c), where it is evident that switching loss decreases as common source inductance decreases. It is believe that if the proposed synchronous buck VR with current source driver were similarly integrated, the efficiency of the proposed solution would be improved further.

Table 4.3 Efficiency comparison between the proposed current source driver and other state of the art VRs at 12V input, 1.5V output and 1MHz switching frequency

VR Topology	Output Current/ Phase [A]	Efficiency [%]
Proposed current source driver	12.5	87.3
	20	86.9
Tapped inductor buck converter [57]	12.5	84
Toshiba Multi Chip Module (TB7001FL)	20	85

A second efficiency comparison is given in Table 4.4 for 1.3V output. The proposed current source driver achieves an efficiency of 86.4% compared to 82% for the phase-shift buck converter in [58] at 17.5A. In addition, the proposed driver achieves nearly the same efficiency as the self-driven soft-switching buck-derived multiphase converter in [59] at 25A. However, in terms of power density and cost, the current source driver has significant advantages, since the self-driven soft-switching buck requires an additional transformer.

Table 4.4 Efficiency comparison between the proposed current source driver and other state of the art VRs at 12V input, 1.3V output and 1MHz switching frequency

VR Topology	Output Current/ Phase [A]	Efficiency [%]
Proposed current source driver	17.5	86.4
	25	84.2
Soft-switching phase-shift buck converter [58]	17.5	82
Soft-switching buck-derived multiphase converter [59]	25	84.7

In addition to the above performance advantages, it should be noted that the current source driver does not require a change in the multiphase buck architecture of today's VRs, which feature low cost and simple control.

4.8 Conclusions

A new current source gate drive circuit has been proposed for high efficiency synchronous buck voltage regulators. The proposed circuit achieves quick turn on and turn off transition times to reduce switching loss and conduction loss. The circuit consists of two sets of four control switches and two small current source inductors (68nH and 307nH) and it can drive both the HS MOSFET and synchronous MOSFET in a synchronous buck VR. The current through the current source inductance is discontinuous in order to minimize circulating current conduction loss present in other methods. The circuit operation, summary of advantages, logic and level shift circuits, optimal design procedure and design example and experimental results have been presented for the proposed circuit.

Experimental results demonstrate an efficiency of 87.5% at 15A load and 83.3% at 30A load for 12V input and 1.5V output at 1MHz. At 1.5V output, the synchronous buck VR achieved a loss reduction of 21.9% in comparison to an identical synchronous buck VR with UCC27222 conventional driver. At 1.3V output, a loss reduction of 24% was achieved in comparison to the

conventional driver. At 1.2V, the loss reduction was 34% and at 1.0V output, a loss reduction of 27.6% was achieved. The loss reduction translates into fewer phases for a voltage regulator. For example, it was demonstrated that if implemented in a 120A multiphase VR, the proposed driver would eliminate one of the required buck phases, yielding a significant potential cost savings.

Chapter 5

A Practical and Accurate Switching Loss Model for Buck Voltage Regulators[‡]

5.1 Introduction

In order to optimally design a high frequency switching converter, engineers and researchers begin their design by estimating the losses in a design file that is typically created using a spreadsheet, or other mathematical software. Device data sheet values and analytical models are used to calculate the losses. Using the loss models, many design parameters and components are compared to achieve a design with the optimal combination of efficiency and cost.

With analytical models, most often piecewise linear turn on and turn off waveforms are used, or simplified equivalent circuits are used to derive switching loss equations. These methods yield closed form mathematical expressions that can be easily used to produce optimization curves within a design file, however the challenge is to improve accuracy while minimizing complexity. Most often, piecewise linear turn on and turn off waveforms are used, or simplified equivalent circuits are used to derive switching loss equations.

One of the most popular analytical models is the piecewise linear model presented in [19]. This model is referred to as the conventional model and is used as a benchmark later for comparison purposes with the proposed model. This model enables simple and rapid estimation of switching loss, however, the main drawback is that it neglects the switching loss dependences due to common source inductance and other parasitic inductances. Typically, this model predicts that turn on and turn off loss are nearly similar in magnitude, however in a real converter

[‡] The content of this chapter has been submitted to the following journal:

[1] W. Eberle, Z. Zhang, Y.F. Liu and P.C. Sen, "A Practical Switching Loss Model for Buck Voltage Regulators," IEEE Trans. Power Electron., TPEL-2008-02-0070.

operating at a high switching frequency, the model is highly inaccurate since turn off loss is much larger due to common source inductance and other parasitic inductances.

A comprehensive analytical model is presented in [21]. This model is an extension of the model presented in [19], with the advantage that it provides accurate characterization of switching loss when common source inductance is included. The main drawback of the models in [21] and [19] is their complexity.

The synchronous buck remains the topology of choice for voltage regulators in today's computers [12],[13],[44]-[54]. However, in order to properly model switching loss in a buck VR, a detailed understanding of the impact of MOSFET gate capacitance, common source inductance, other parasitic inductance and load current on switching loss is necessary. This is most easily accomplished through careful examination of waveforms through simulation and experiments, which are included in section 5.2 following the approach presented in [44].

In section 5.3, a new switching loss model is proposed with the goal of maintaining the relative simplicity of the very popular conventional model in [19], while improving the accuracy for high frequency synchronous buck with parasitic circuit inductances, including common source inductance. In particular, the model predicts the large decrease in turn on loss and increase in turn off loss that occurs as undesired circuit parasitic inductance increases. The proposed model is then extended to current source drivers in section 5.4. The proposed model is compared to the conventional model and Spice simulation results in section 5.5. The model validation with experimental results are presented in section 5.6. The conclusions are presented in section 5.7.

5.2 Impact of Parasitic Inductance and Load Current

A synchronous buck converter is illustrated in Figure 5.1. In a synchronous buck VR, it is well known that the input voltage, load current and high side (HS) MOSFET gate-to-drain charge

influence switching loss in the HS MOSFET. However, it is not well known that the inductances associated with the device packaging and PCB traces also contribute significantly to HS MOSFET switching loss. It is worth noting, but generally well known that with proper dead time, the synchronous rectifier (SR) switches with near zero switching loss.

The synchronous buck in Figure 5.1 includes parasitic drain and source inductances for the HS MOSFET, M_1 , and SR MOSFET, M_2 . It can be assumed that the source inductances, L_{s1} and L_{s2} are common to their respective drive signals. Any other inductance in the source that is not common to the source is assumed to be lumped with the drain inductances, L_{d1} and L_{d2} . These inductances have a significant impact on the switching loss behavior in high frequency synchronous buck voltage regulators.

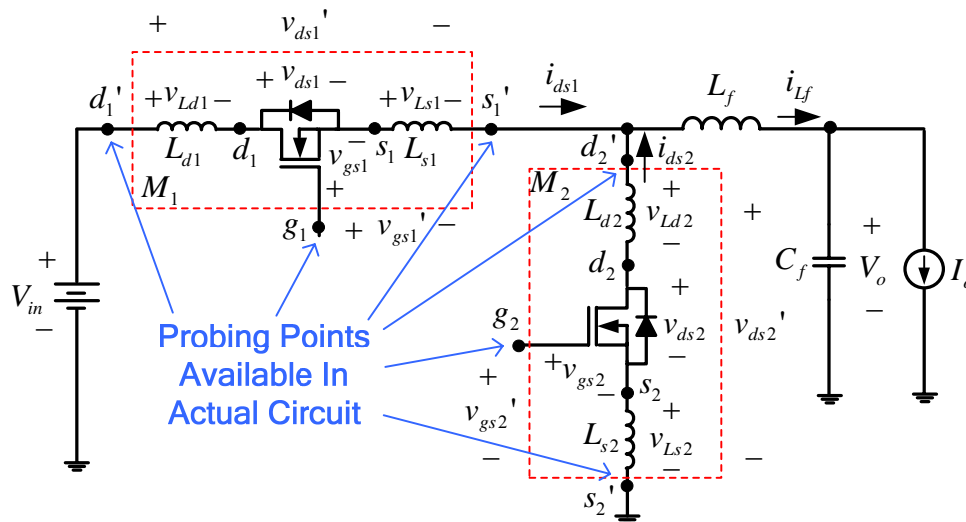


Figure 5.1 Synchronous buck voltage regulator with parasitic inductances

During the switching transitions, the HS MOSFET operates in the saturation (linear) mode as a dependent current source simultaneously supporting the current through the device and voltage across it. At turn on and turn off, the gate-source voltage, v_{gs1} , is held at the plateau voltage, V_{pl} , by the feedback mechanism provided by the voltage across the common source inductance, v_{Ls1} .

Simulation waveforms are illustrated in Figure 5.2 for a buck voltage regulator at 12V input, 30A load, 8V drive voltage and 1MHz switching frequency. The top curves are the HS MOSFET switch current, i_{ds1} and actual drain-to-source voltage, v_{ds1} . The second set of curves are the v_{gs1} (Actual) and v_{gs1}' (Measured; $v_{gs1}' = v_{gs1} + v_{Ls1}$) waveforms, which are included to demonstrate that measuring v_{gs1}' in the lab provides an inaccurate representation of the switching times. The bottom curve is the power loss in the MOSFET, $P_{M1} = v_{ds1}i_{ds1}$. Typical, parasitic inductance values for common package types are provided by the semiconductor manufacturers in application notes [45]-[46] and range from approximately 250pH-1nH, depending on the package type. Matched inductances of 500pH each for the four inductances were used in the simulation.

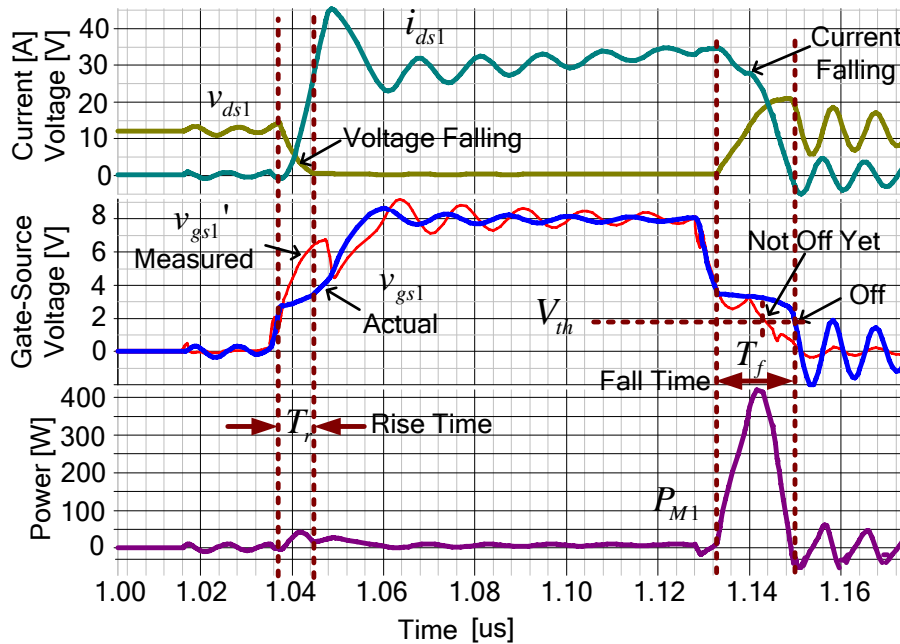


Figure 5.2 Synchronous buck voltage regulator HS MOSFET waveforms (top: actual drain-source voltage, v_{ds1} and drain current, i_{ds1} ; middle: measured gate-source voltage, v_{gs1}' and actual gate-source voltage (bold), v_{gs1} ; bottom: HS MOSFET power, $v_{ds1}i_{ds1}$)

As can be observed from the circuit in Figure 5.1, at turn on, as the HS MOSFET current increases, v_{Ls1} is positive in the direction noted, so this voltage subtracts from the V_{cc} voltage applied to the gate, enabling $v_{gs1} = V_{pl}$ while the MOSFET operates in the saturation mode. At the

same time, the four parasitic inductances provide a current snubbing effect, which virtually eliminates turn on switching loss enabling a near zero current switching (ZCS) turn on. During this transition, the rise time, T_r , is dictated by the gate driver's ability to charge the MOSFET gate capacitances (C_{iss} from V_{th} to V_{pl} and C_{gd} to V_{in}), which is the time for v_{ds1} to fall to zero. Then, it is assumed that this time is independent of the time it takes i_{ds1} to rise to its final value equal to the buck inductor current. i.e. after T_r , i_{ds1} can be less than the buck inductor current.

At turn off, as the HS MOSFET current decreases, v_{Ls1} is negative in the direction noted Figure 5.1, so this voltage subtracts from the low impedance source voltage (ideally zero volts) applied to the gate enabling $v_{gs1}=V_{pl}$ while the MOSFET operates in the saturation mode. During this transition, the fall time, T_f , is the time for the HS MOSFET current to fall from the buck inductor current to zero. This time is dictated by both the gate driver's ability to discharge the MOSFET gate capacitances (C_{gd} from V_{in} , and C_{iss} from V_{pl} to V_{th}) and by the four parasitic inductances, which prolong the time for i_{ds1} to fall to zero by limiting the di_{ds}/dt .

As alluded to in the two paragraphs above, the MOSFET and trace parasitic inductances have vastly different effects at turn on and turn off. At turn on, the inductances provide a current snubbing effect, which decreases turn on switching loss. At turn off, the inductances increase the turn off loss by prolonging T_f . In addition, as load current increases, T_f increases, so turn off losses increase proportionally to I_o^2 (proportional to I_o and $T_f(I_o)$). In contrast, at turn on, the load current magnitude has ideally no effect on the T_r . Therefore, in real circuits, turn off loss is much greater than turn on loss.

Another important point to note from Figure 5.1 and Figure 5.2 is that in a real circuit, the board mounted packaged inductances are distributed within the MOSFET devices. Therefore, when probing in the lab, one only has access to the external terminals, g_1 , s_1' and d_1' for the HS MOSFET and g_2 , s_2' and d_2' for the SR. However, the actual nodes that provide waveform

information relevant to the switching loss are at the unavailable internal nodes s_I and d_I for the HS MOSFET. Using the plateau portion of the measured gate-source voltage, v_{gsI}' to determine the switching loss times is misleading since the induced voltage across L_{sI} is included. Probing v_{gsI}' in the lab, one would observe a negligible T_r at turn on, and a turn off T_f less than one half of the actual T_f . The actual v_{gsI} waveform, which cannot be measured in a real circuit, more clearly illustrates the plateau portions in the rise and fall times.

To demonstrate the effects of load current and common source inductance, experimental testing was done at a reduced frequency of 200kHz, with the source connection cut and a wire inserted in the common source path to measure the MOSFET current. Measurement waveforms are illustrated in Figure 5.3, and Figure 5.4, where the load current has been increased from 0A to 5A. With this method, the inductance of the wire (approximately 20nH) is much greater than the approximate total package inductance of 1nH, so the package inductance can be neglected allowing for measurement of v_{gsI} and v_{dsI} . As stated previously, it is noted that as load current increases from 0 to 5A, T_r remains nearly unchanged from 20ns to 22ns, but T_f increases significantly from 48ns to 96ns. In addition, at a constant load current of 5A, as illustrated in Figure 5.5, as L_{sI} increases to 30nH (using a longer 3 inch wire), T_r remains relatively unchanged from 22ns to 24ns, while T_f further increases from 96ns to 160ns.

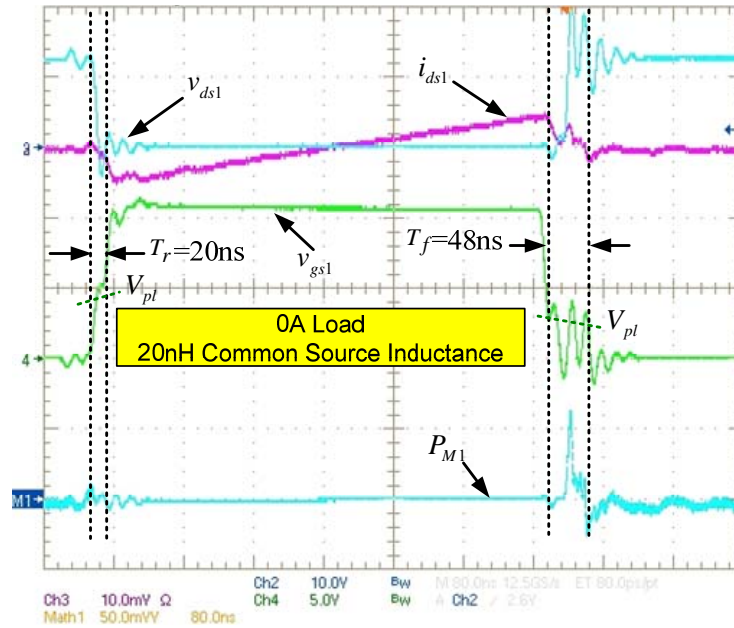


Figure 5.3 Switching waveforms at 0A load and 20nH common source inductance (80ns/div; v_{ds1} : 10V/div; i_{ds1} : 5A/div; v_{gs1} : 5V/div; P_{M1} : 50W/div)

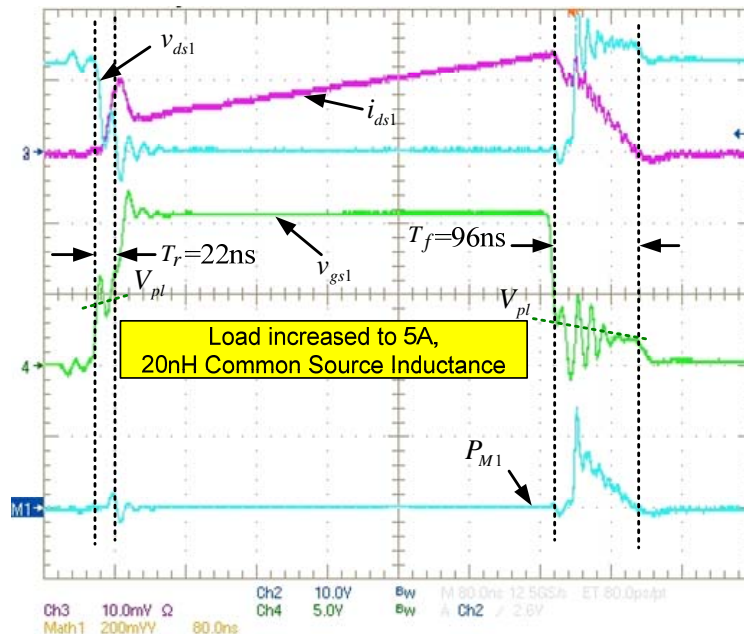


Figure 5.4 Switching waveforms at 5A load and 20nH common source inductance (80ns/div; v_{ds1} : 10V/div; i_{ds1} : 5A/div; v_{gs1} : 5V/div; P_{M1} : 200W/div)

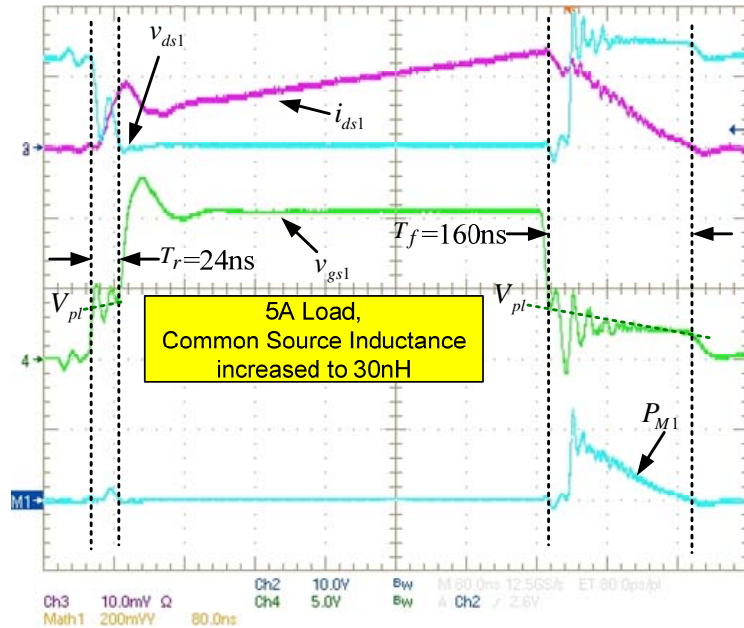


Figure 5.5 Switching waveforms at 5A load with 30nH common source inductance (80ns/div; v_{ds1} : 10V/div; i_{ds1} : 5A/div; v_{gs1} : 5V/div; P_{M1} : 200W/div)

From knowledge of the circuit operation and observation of the experimental results presented, three important observations and conclusions can be made:

- 1) In a practical synchronous buck voltage regulator, turn off loss is much greater than turn on loss since the circuit inductances provide a current snubbing effect, which decreases and virtually eliminates turn on switching loss, but increases the turn off loss by prolonging T_f .
- 2) T_r is dictated by the time for the voltage to fall to zero and is independent of the final value of the current. In addition, load current has negligible impact on T_r , while common source inductance has only a small impact, since as L_{s1} increases, the current di_{ds}/dt decreases.
- 3) T_f is dictated by the time for the current to fall to zero. Load current, common source inductance and other circuit parasitic inductances (i.e. L_{d1} , L_{s2} , and L_{d2}) increase T_f .

5.3 Proposed Switching Loss Model

Typical switching waveforms for a synchronous buck VR are illustrated in Figure 5.6. The proposed model uses the piecewise linear approximations (noted with thicker bold lines) of the switching waveforms in Figure 5.6. Turn on switching loss occurs during T_r and turn off switching loss occurs during T_f . The key to the model is prediction of the turn on current, I_{on} , the rise and fall times, T_r and T_f , the reverse recovery current, I_{rr} , the magnitude of the rising current slope, $\Delta i_{ds}/\Delta t$, and the current drop, Δi_{lf} , when v_{ds1} rises to V_{in} at turn off. The goal of the proposed model is to calculate the switching loss with respect to load current, driver supply voltage, driver gate current and total circuit inductance in a simple manner.

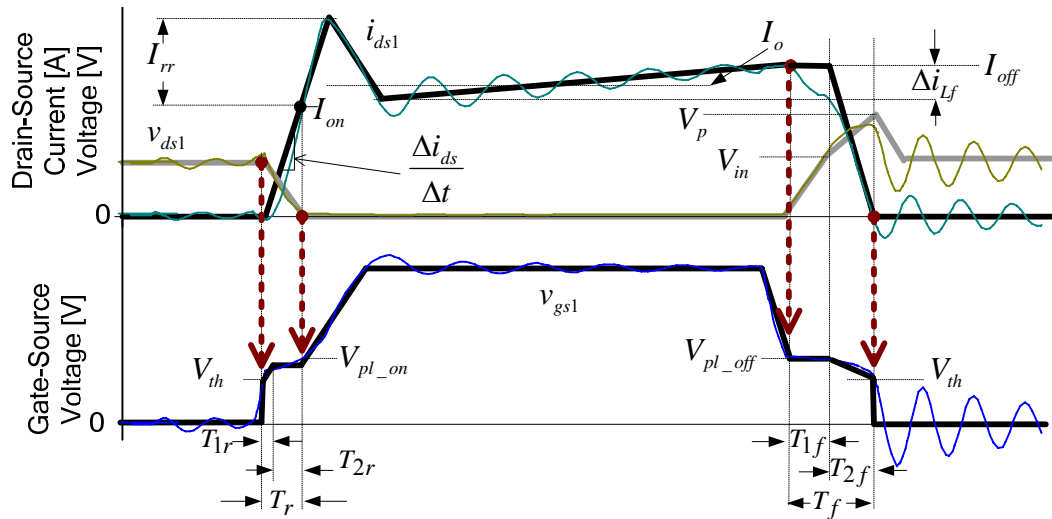


Figure 5.6 Synchronous buck HS MOSFET waveforms with piecewise linear approximations of these waveforms in bold

The MOSFET parasitic capacitances are required in the model. They are estimated using the effective values [19] as follows in (5.1)-(5.3) using datasheet specification values for V_{ds1_spec} , C_{rss1_spec} , and C_{iss1_spec} . The C_{ds1} capacitor of the synchronous buck HS MOSFET is neglected in the proposed model.

$$C_{gd1} = 2C_{rss1_spec} \sqrt{\frac{V_{ds1_spec}}{V_{in}}} \quad (5.1)$$

$$C_{iss1} = C_{iss1_spec} \quad (5.2)$$

$$C_{gs1} = C_{iss1} - C_{gd1} \quad (5.3)$$

In the following three sub-sections, derivations of the model for the turn on, turn off and the total switching loss are presented.

5.3.1 Turn On Switching Loss Model

Piecewise linear turn on waveforms of i_{ds1} , v_{ds1} , v_{gs1} and the power loss in M_1 , P_{M1} , are provided in Figure 5.7. These waveforms and knowledge of the circuit operation are used extensively in this sub-section in order to derive the turn on loss, P_{on} .

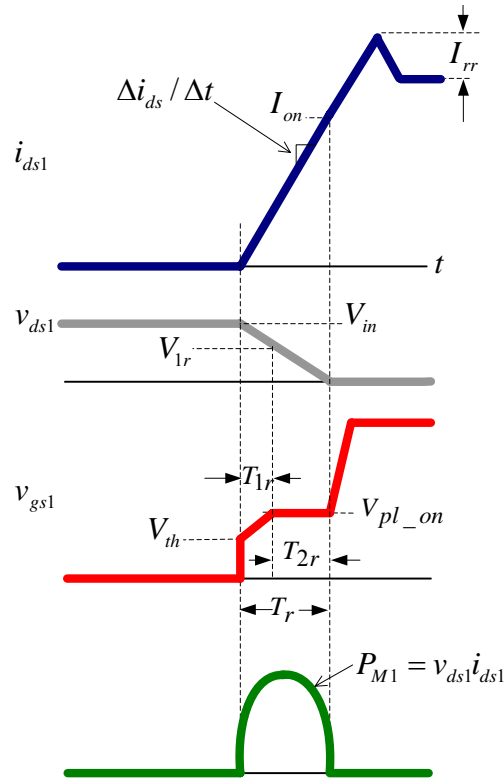


Figure 5.7 Synchronous buck HS MOSFET waveforms at turn on with piecewise linear approximations

By definition, P_{on} , is derived using the simple integral in (5.4), representing the average

power over one switching period.

$$P_{on} = f_s \int_0^{T_r} v_{ds1} i_{ds} dt \quad (5.4)$$

Using the piecewise linear geometry for the voltage and current waveforms at turn on in Figure 5.7, v_{ds1} is given by (5.5) and i_{ds} can be expressed by (5.6), allowing P_{on} to be given by (5.7), which evaluates to the expression given in (5.8).

$$v_{ds1} = V_{in} - \frac{V_{in}}{T_r} t \quad (5.5)$$

$$i_{ds} = \frac{I_{on}}{T_r} t \quad (5.6)$$

$$P_{on} = f_s \int_0^{T_r} \left[\left(\frac{I_{on}}{T_r} t \right) \left(V_{in} - \frac{V_{in}}{T_r} t \right) \right] dt \quad (5.7)$$

$$P_{on} = \frac{1}{6} V_{in} I_{on} T_r f_s \quad (5.8)$$

The power loss in (5.8) is the product of V_{in} , I_{on} , f_s and T_r . The two parameters that are key to accurate prediction of P_{on} are the current at turn on, I_{on} and T_r . The turn on current, I_{on} is the HS MOSFET drain current when $v_{ds1}=0$. The remainder of this sub-section provides a simple procedure to calculate I_{on} and T_r , to enable calculation of P_{on} .

As discussed in section 5.2, T_r is dictated by the gate driver's ability to charge the MOSFET gate capacitances, which is the time for v_{ds1} to fall to zero. This time is assumed independent of the time it takes i_{ds1} to rise to its final value. Under this assumption, T_r consists of two intervals, T_{1r} and T_{2r} which are discussed in the following sub-sections.

5.3.1.1 Rise Time Interval T_{1r} : Charging HS MOSFET C_{gs1} and C_{gd1} Gate Capacitances

The HS MOSFET equivalent circuit during T_{1r} is given in Figure 5.8. The gate resistance, R_r , represents the total series resistance in the gate drive path. i.e. $R_r = R_{hi} + R_{ext} + R_g$, where R_{hi} is the resistance of the driver switch, R_{ext} is any external resistance and R_g represents the internal gate

resistance of the MOSFET.

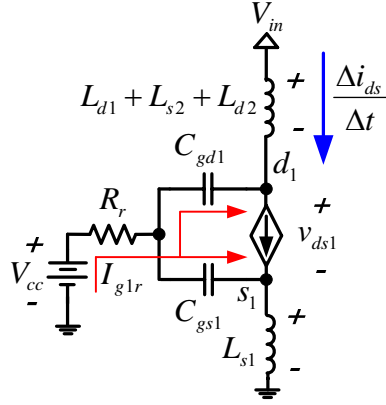


Figure 5.8 Synchronous buck HS MOSFET equivalent circuit during T_{1r}

During T_{1r} , the C_{gs1} capacitance is charged from V_{th} to V_{pl_on} , while the gate side of C_{gd1} charges from V_{th} to V_{pl_on} and the drain side of the C_{gd1} capacitance discharges from V_{in} to V_{1r} . Therefore, the change in voltage across C_{gd1} during T_{1r} is $[(V_{in}-V_{1r})+(V_{pl_on}-V_{th})]$. Then, T_{1r} is given by (5.9), assuming an average gate charging current I_{g1r} . V_{pl_on} represents the plateau voltage at turn on and is given by (5.10), where Δi_{Lf} represents the buck output inductor ripple current. Since the peak MOSFET current at turn on is lower than at turn off, the plateau voltage at turn on differs slightly than at turn off. In (5.9), $\Delta V_{gsr} = V_{pl_on} - V_{th}$.

$$T_{1r} = \frac{C_{gs1}\Delta V_{gsr} + C_{gd1}[\Delta V_{gsr} + (V_{in} - V_{1r})]}{I_{g1r}} \quad (5.9)$$

$$V_{pl_on} = V_{th} + \frac{I_o - 0.5\Delta i_{Lf}}{g_{fs}} \quad (5.10)$$

The drain-source voltage during T_{1r} is given by (5.11), where $L_{loop} = L_{s1} + L_{d1} + L_{s2} + L_{d2}$.

$$v_{ds1} = V_{in} - L_{loop} \frac{di_{ds1}}{dt} \quad (5.11)$$

Neglecting the gate current through the inductances, the rate of change of drain current in (5.11) is given by (5.12), which is approximated by (5.14) using (5.13) and the piecewise linear approximation of the gate-source voltage waveform during T_{1r} .

$$\frac{di_{ds1}}{dt} = \frac{dg_{fs}(v_{gs1} - V_{th})}{dt} = \frac{g_{fs} dv_{gs1}}{dt} \quad (5.12)$$

$$\frac{di_{ds}}{dt} \approx \frac{\Delta i_{ds}}{\Delta t} \quad (5.13)$$

$$\frac{\Delta i_{ds}}{\Delta t} = \frac{g_{fs} \Delta v_{gs1}}{\Delta t} = \frac{g_{fs} \Delta V_{gsr}}{T_{1r}} \quad (5.14)$$

Using (5.12)- (5.14), the intermediate voltage, V_{1r} is given by (5.15).

$$V_{1r} = V_{in} - L_{loop} \frac{g_{fs} \Delta V_{gsr}}{T_{1r}} \quad (5.15)$$

The driver equivalent circuit during T_{1r} is illustrated in Figure 5.9. During this time interval, it is assumed that v_{gs1} is the average value of the plateau, V_{pl_on} , and threshold voltages, V_{th} . In addition, in the proposed model, the slope of the drain current is assumed constant; therefore the voltage $v_{Ls1} = L_{s1} \Delta i_{ds} / \Delta t$ is constant, so the L_{s1} inductance is replaced by an ideal voltage source in the drive circuit. The average gate current, during T_{1r} , using the linearized v_{gs1} waveform is given by (5.16).

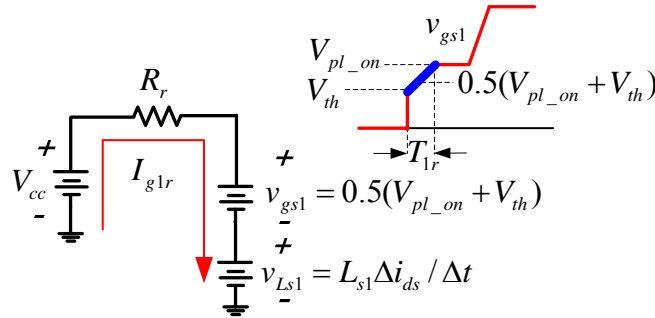


Figure 5.9 Driver equivalent circuit during T_{1r}

$$I_{gr} = \frac{V_{cc} - 0.5(V_{pl_on} + V_{th}) - L_{s1} \frac{\Delta i_{ds}}{\Delta t}}{R_r} \quad (5.16)$$

Using (5.9), and (5.14)-(5.16), solving for T_{1r} yields (5.17), where $V_{gs1r} = 0.5(V_{pl_on} + V_{th})$.

$$T_{1r} = \frac{\Delta V_{gsr} (L_{s1} g_{fs} + R_r C_{iss1}) + \sqrt{[\Delta V_{gsr} (L_{s1} g_{fs} + R_r C_{iss1})]^2 + 4\Delta V_{gsr} (V_{cc} - V_{gs1r}) R_r C_{gd1} L_{loop} g_{fs}}}{2V_{gs1r}} \quad (5.17)$$

5.3.1.2 Rise Time Interval T_{2r} : Charging the HS MOSFET C_{gd1} Gate Capacitance

The HS MOSFET equivalent circuit during T_{2r} is given in Figure 5.10.

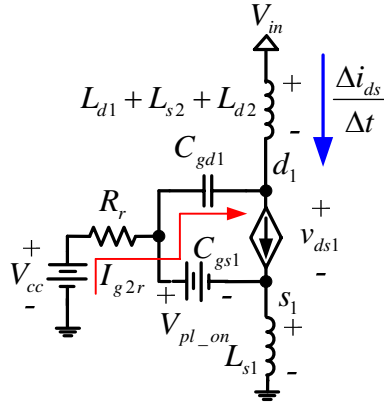


Figure 5.10 Synchronous buck HS MOSFET equivalent circuit during T_{2r}

During T_{2r} , the gate voltage of the C_{gd1} capacitance remains constant at V_{pl_on} , while the drain node of C_{gd1} is discharged by current I_{g2r} , allowing T_{2r} to be given by (5.18).

$$T_{2r} = \frac{C_{gd1} V_{1r}}{I_{g2r}} \quad (5.18)$$

The driver equivalent circuit during T_{2r} is illustrated in Figure 5.11. Due to the assumed constant $\Delta i_{ds}/\Delta t$, the L_{s1} inductance is replaced by an ideal voltage source. Under these assumptions, the gate current is given by (5.19).

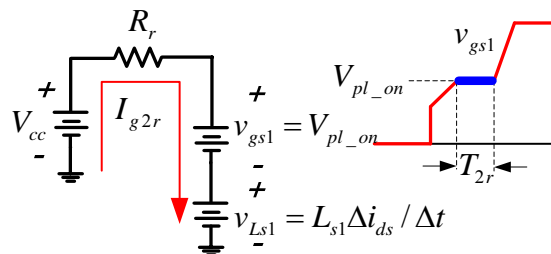


Figure 5.11 Driver equivalent circuit during T_{2r}

$$I_{g2r} = \frac{V_{cc} - V_{pl_on} - L_{s1} \frac{\Delta i_{ds}}{\Delta t}}{R_r} \quad (5.19)$$

Using (5.14), (5.15) (5.18) and (5.19), solving for T_{2r} yields (5.20).

$$T_{2r} = \frac{R_r C_{gd1} \left(V_{in} - L_{loop} g_{fs} \frac{\Delta V_{gsr}}{T_{1r}} \right)}{V_{cc} - V_{pl_on} - L_{s1} g_{fs} \frac{\Delta V_{gsr}}{T_{1r}}} \quad (5.20)$$

The total T_r is the sum of T_{1r} and T_{2r} as given by (5.21). The total turn on switching loss can be calculated using (3.2), (5.26) and (5.21).

$$T_r = T_{1r} + T_{2r} \quad (5.21)$$

The final step to determine the turn on loss is to estimate the current I_{on} at the end of T_r . Depending on the load current and parasitic inductances, calculating I_{on} can require estimation of the reverse recovery current, I_{rr} of the SR MOSFET. The waveform in Figure 5.12 is used to estimate I_{rr} . When the HS MOSFET turns on, the SR body diode cannot reverse block, so the SR current goes negative and the HS current spikes by the same magnitude. The total reverse recovery time is T_{rr} . The rising slope magnitude is $\Delta i_{ds}/\Delta t$ and the reverse recovery charge is Q_{rr} , which represents the shaded area as given by (5.22). Using the geometry, the reverse recovery current as a function of T_{rr} is given by (5.23). Then, eliminating T_{rr} from (5.22) and (5.23), (5.25) is derived, which represents I_{rr} as a function of Q_{rr} and the known slope. In addition, since reverse recovery charge increases with load current, Q_{rr} is approximated using (5.24), where Q_{rr_spec} and I_{rr_spec} are the datasheet specification values.

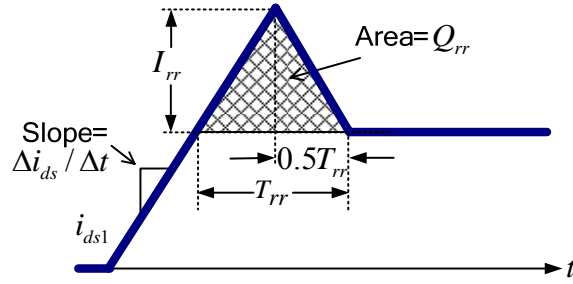


Figure 5.12 Synchronous buck HS MOSFET current waveform approximation during reverse recovery at turn on

$$Q_{rr} = \frac{1}{2} I_{rr} T_{rr} \quad (5.22)$$

$$I_{rr} = \frac{\Delta i_{ds}}{\Delta t} \frac{1}{2} T_{rr} \quad (5.23)$$

$$Q_{rr} = \frac{Q_{rr_spec}}{I_{rr_spec}} I_o \quad (5.24)$$

$$I_{rr} = \sqrt{\frac{\Delta i_{ds}}{\Delta t} Q_{rr}} \quad (5.25)$$

Since the rise time is dictated by the time for the HS MOSFET voltage, v_{ds1} , to fall to zero, the current at the end of T_r can be at any value equal to, or less than the inductor current plus the reverse recovery current. (i.e. I_{on} is not necessarily equal to the inductor current, as in the conventional model [19], or the inductor current plus the reverse recovery current). There are three cases for I_{on} as illustrated in Figure 5.13.

The first and most common case is illustrated in Figure 5.13(a) where I_{on} is less than the peak of the turn on current waveform at the end of T_r . This case occurs under heavy load conditions and/or with typical, or large values of parasitic inductances which limit the $\Delta i_{ds}/\Delta t$. In this case, the turn on current is determined by the slope of the current at turn on multiplied by T_r , as given by the first condition in (5.26).

$$\begin{aligned}
I_{on} &= \frac{\Delta i_{ds}}{\Delta t} T_r \quad \text{if} \quad \frac{\Delta i_{ds}}{\Delta t} T_r < I_o - 0.5\Delta i_{Lf} + I_{rr} \\
&= I_o - 0.5\Delta i_{Lf} + I_{rr} \quad \text{otherwise}
\end{aligned}
\tag{5.26}$$

The first condition holds true as long as the calculated value is less than the inductor current ($I_o - 0.5\Delta i_{Lf}$) plus I_{rr} , which leads to the second and third conditions in Figure 5.13(b) and Figure 5.13 (c).

Under light load and/or conditions where the parasitic inductances are small, using the current slope times T_r would yield a turn on current greater than the peak current and somewhere on the dotted line extensions in Figure 5.13(b) and Figure 5.13(c). In this case, the current is capped at maximum value of the inductor current plus reverse recovery current as given by the second condition in (5.26). The third case, illustrated in Figure 5.13(c), occurs under very light load conditions, and/or when the parasitic inductances are very small. To simplify the model, this case is neglected and if it occurs, the second case in Figure 5.13(b) is used as given by the second condition in (5.26).

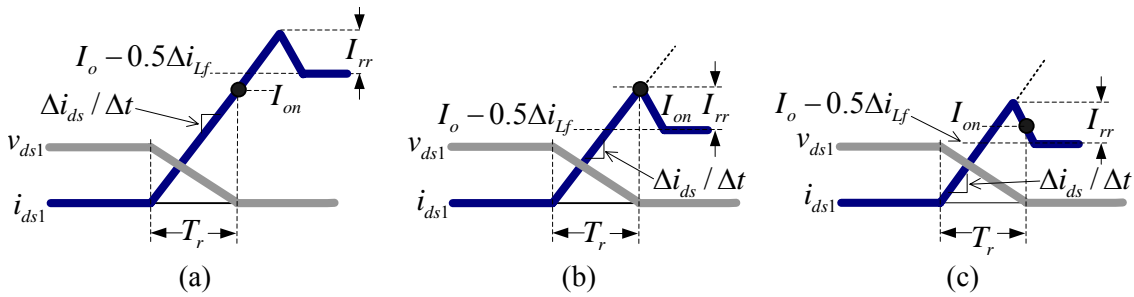


Figure 5.13 Three possible cases of turn on current when $V_{ds1}=0$: (a) I_{on} less than I_{ds1} peak value, (b) I_{on} is equal to the I_{ds1} peak value, (c) I_{on} occurs after the I_{ds1} peak value

5.3.2 Turn Off Switching Loss Model

Piecewise linear turn off waveforms of i_{ds1} , v_{ds1} , v_{gs1} and the power loss in M_I , P_{M_I} , are provided in Figure 5.14. These waveforms and knowledge of the circuit operation are used extensively in this sub-section in order to derive the turn off loss, P_{off} . The turn off transition

consists of two intervals, T_{1f} and T_{2f} .

During T_{1f} , the Miller capacitor, C_{gd1} is discharged while v_{gs1} remains at V_{pl_off} and i_{ds1} is assumed to remain constant. In a real circuit, it is noted that i_{ds1} begins to fall during T_{1f} , however the current slope is limited due to the discharging of the C_{gd2} and C_{ds2} capacitors of the SR. During this interval, v_{ds1} increases from zero to V_{in} . Therefore, from the geometry, the turn off power loss, P_{1off} , during T_{1f} is given by (5.27).

$$P_{1off} = \frac{1}{2} V_{in} I_{off} T_{1f} f_s \quad (5.27)$$

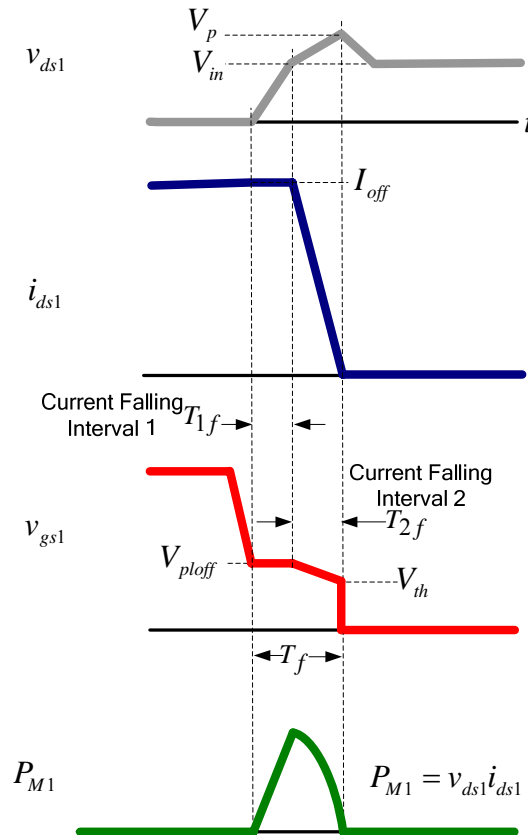


Figure 5.14 Synchronous buck HS MOSFET waveforms at turn off with piecewise linear approximations

During T_{2f} , C_{gs1} is discharged from V_{pl_off} to V_{th} , while the gate node of C_{gd1} is also discharged

from V_{pl_off} to V_{th} and the drain node of C_{gd1} is charged from V_{in} to the peak voltage at turn off, V_p . During this interval, i_{ds1} falls from I_{off} to zero, while v_{ds1} rises from V_{in} to V_p . Using a simple integral following the procedure presented in section 5.3.1, the turn off loss during T_{2f} is approximated as P_{2off} , given by (5.28).

$$P_{2off} = \left(\frac{1}{6}(V_p - V_{in})I_{off} + \frac{1}{2}V_{in}I_{off} \right) T_{2f} f_s \quad (5.28)$$

The total turn off loss, P_{off} , is the sum of P_{1off} and P_{2off} as given by (5.29).

$$P_{off} = P_{1off} + P_{2off} \quad (5.29)$$

The parameters that are key to accurate prediction of the turn off loss are the HS MOSFET current at turn off, I_{off} , the intervals T_{1f} , and T_{2f} , and the peak overshoot voltage of v_{ds1} , V_p . The turn off current is the load current, I_o , plus half of the filter inductor peak-to-peak ripple current, Δi_{Lf} , as given by (5.30).

$$I_{off} = I_o + \frac{1}{2}\Delta i_{Lf} \quad (5.30)$$

The plateau voltage at turn off, V_{pl_off} , is given by (5.32). It differs slightly from V_{pl_on} at turn on due to the larger switch current during the transition.

$$V_{pl_off} = V_{th} + \frac{I_o + 0.5\Delta i_{Lf}}{g_{fs}} \quad (5.31)$$

The turn off loss estimated using (5.29) is a function of T_f . During T_f , the current falls from I_{off} to zero and v_{ds1} rises from zero to V_p . It is a function of the driver's capability to discharge C_{gd1} and C_{iss1} , but in addition, it is a function of circuit parasitic inductances which limit the current falling slope and therefore, the falling time.

5.3.2.1 Fall Time Interval T_{1f} : Discharging the HS MOSFET C_{gd1} Gate Capacitance

The HS MOSFET equivalent circuit during T_{1f} is given in Figure 5.15. Since i_{ds1} remains constant at I_{off} , the $\Delta i_{ds}/\Delta t=0$, so the parasitic inductors can be neglected. T_{1f} is the time required

to discharge the C_{gd1} capacitance by gate current I_{g1f} as given by (5.32).

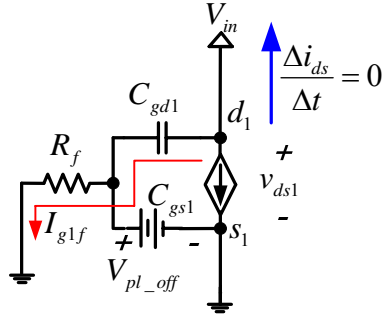


Figure 5.15 Synchronous buck HS MOSFET equivalent circuit during T_{1f}

$$T_{1f} = \frac{C_{gd1} V_{in}}{I_{g1f}} \quad (5.32)$$

The driver equivalent circuit during T_{1f} is illustrated in Figure 5.16. During this time interval, it is assumed that v_{gs1} remains constant at the plateau, V_{pl_off} . With this assumption, the gate current is easily derived as given by (5.33) where $R_f = R_{lo} + R_{ext} + R_g$, and V_{pl_off} is given by (5.31).

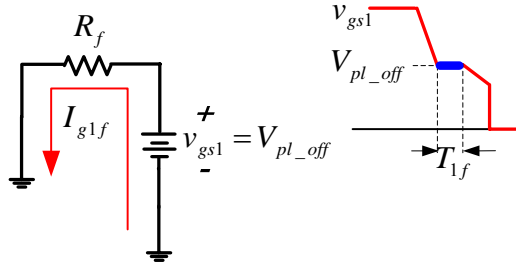


Figure 5.16 Driver equivalent circuit during T_{1f}

$$I_{g1f} = \frac{V_{pl_off}}{R_f} \quad (5.33)$$

Using (5.32) and (5.33), T_{1f} is given by (5.34).

$$T_{1f} = \frac{C_{gd1} V_{in} R_f}{V_{pl_off}} \quad (5.34)$$

5.3.2.2 Fall Time Interval T_{2f} : Current Falling and Discharging the HS MOSFET C_{gs1} and C_{gd1} Gate Capacitances

The HS MOSFET equivalent circuit during T_{2f} is given in Figure 5.17. During T_{2f} , the C_{gs1} capacitance is discharged from V_{pl_off} voltage to V_{th} , while the voltage at the drain side of the C_{gd1} capacitance charges from V_{in} to V_p and the voltage at the gate side of C_{gd1} discharges from V_{pl_off} to V_{th} . Therefore, the change in voltage across C_{gd1} during T_{2f} is $[(V_p - V_{in}) + (V_{pl_off} - V_{th})]$. Then, T_{2f} is given by (5.35), where $\Delta V_{gsf} = V_{pl_off} - V_{th}$.

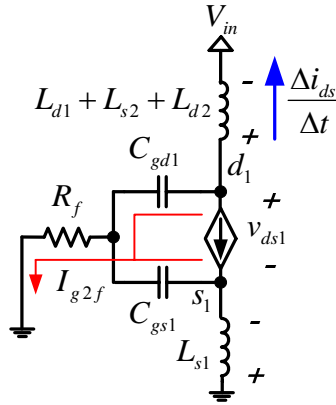


Figure 5.17 Synchronous buck HS MOSFET equivalent circuit during T_{2f}

$$T_{2f} = \frac{C_{gs1} \Delta V_{gsf} + C_{gd1} [(V_p - V_{in}) + \Delta V_{gsf}]}{I_{g2f}} \quad (5.35)$$

The drain-source voltage during T_{2f} is given by (5.36), where $L_{loop} = L_{s1} + L_{d1} + L_{s2} + L_{d2}$.

$$v_{ds} = V_{in} + L_{loop} \frac{di_{ds1}}{dt} \quad (5.36)$$

Following the approach of the approximations made in (5.12) and (5.13), the peak overshoot voltage, V_p is given by (5.37).

$$V_p = V_{in} + L_{loop} \frac{g_{fs} \Delta V_{gsf}}{T_{2f}} \quad (5.37)$$

The driver equivalent circuit during T_{2f} is illustrated in Figure 5.18. During this time interval, it is assumed that v_{gs1} is the average value of the plateau, V_{pl_off} , and threshold voltages,

V_{th} . As above, the L_{s1} inductance is replaced by an ideal voltage source, where the di_{ds}/dt is assumed constant at $g_{fs}\Delta V_{gsf}/T_{2f}$. With these assumptions, the average gate current during T_{2f} , using the linearized v_{gs1} waveform is given by (5.38).

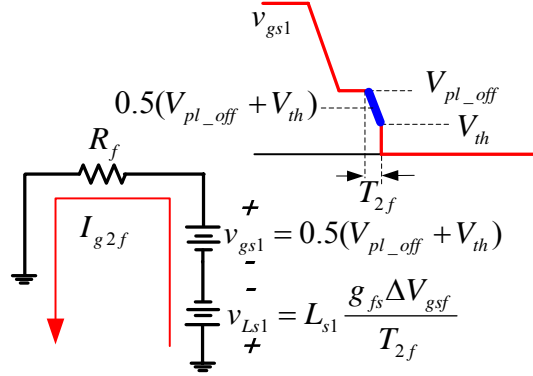


Figure 5.18 Driver equivalent circuit during T_{2f}

$$I_{g2f} = \frac{\frac{1}{2}(V_{pl} + V_{th}) - L_{s1} \frac{g_{fs} \Delta V_{gsf}}{T_{2f}}}{R_f} \quad (5.38)$$

Using (5.35), (5.37) and (5.38), solving for T_{2f} yields (5.39), where $V_{gs2f} = 0.5(V_{pl_off} + V_{th})$.

$$T_{2f} = \frac{\Delta V_{gs2f} (L_{s1} g_{fs} + R_f C_{iss1}) + \sqrt{\Delta V_{gs2f}^2 [L_{s1} g_{fs} + R_f C_{iss1}]^2 + 4 \Delta V_{gs2f} V_{gs2f} R_f C_{gd1} L_{loop} g_{fs}}}{2V_{gs2f}} \quad (5.39)$$

T_f is the sum of T_{1f} and T_{2f} as given by (5.40). The total turn off switching loss can be calculated using (5.27)-(5.31), (5.34), (5.37), (5.39) and (5.40).

$$T_f = T_{1f} + T_{2f} \quad (5.40)$$

5.3.3 Total Switching Loss Model

The total switching loss, given by (5.41), is the sum of the turn on loss, P_{on} , given by (5.8) and turn off loss, P_{off} , given by (5.29).

$$P_{tot_sw} = P_{on} + P_{off} \quad (5.41)$$

5.4 Extension to Current Source Drive Model

The proposed model can be extended to current source drivers presented in [11],[12],[47]-[50]. These drivers are designed to operate with nearly constant current supplied to the power MOSFET gate. The advantage of this class of drivers is that they eliminate the back voltage v_{Ls1} in the gate circuit that reduces the gate current in conventional voltage source gate drivers.

With current source drive, determining the rise and fall time intervals is very simple. In this case, the gate current expressions, I_{g1r} (5.16), I_{g2r} (5.19), I_{g1f} (5.33) and I_{g2f} (5.38) can all be replaced by a constant gate current with magnitude I_g . At turn on, T_{1r} in (5.17) becomes (5.42) and T_{2r} in (5.20) becomes (5.43).

$$T_{1r} = \frac{C_{iss1} + \sqrt{(\Delta V_{gsr} C_{iss1})^2 + 4I_g \Delta V_{gsr} C_{gd1} L_{loop} g_{fs}}}{2I_g} \quad (5.42)$$

$$T_{2r} = \frac{C_{gd1} \left(V_{in} - L_{loop} g_{fs} \frac{\Delta V_{gsr}}{T_{1r}} \right)}{I_g} \quad (5.43)$$

At turn off, T_{1f} in (5.34) becomes (5.44) and T_{2r} in (5.39) becomes (5.45).

$$T_{1f} = \frac{C_{gd1} V_{in}}{I_g} \quad (5.44)$$

$$T_{2f} = \frac{\Delta V_{gsf} C_{iss1} + \sqrt{(\Delta V_{gsf} C_{iss1})^2 + 4I_g \Delta V_{gsf} C_{gd1} L_{loop} g_{fs}}}{2I_g} \quad (5.45)$$

The total turn on switching loss can be calculated using (5.8),(5.21),(5.26),(5.42) and (5.43). The total turn off switching loss can be calculated using (5.27)-(5.31),(5.37),(5.40),(5.44) and (5.45). The total switching loss, given by (5.41), is the sum of the turn on loss, P_{on} , given by (5.8) and turn off loss, P_{off} , given by (5.29).

5.5 Model Verification

The analytical switching loss model with a voltage source drive was compared to SIMetrix Spice simulation and the conventional model in [19].

Simulation results were conducted at 12V input, 1MHz switching frequency, and 10A peak-to-peak buck output inductor ripple (100nH), $R_{hi}=2\Omega$, $R_{lo}=2\Omega$, $R_g=1\Omega$, $R_{ext}=0\Omega$. Results are included in the following sub-sections for both models. MOSFET parameters: M_1 : Si7860DP, $g_{fs}=60S$, $V_{th}=2V$, $C_{iss1_spec}=1800pF$ (@ $V_{ds1_spec}=15V$), $C_{oss1_spec}=600pF$ (@ $V_{ds1_spec}=15V$), $C_{rssl_spec}=200pF$ (@ $V_{ds1_spec}=15V$) and M_2 : Si7336ADP SR, $Q_{rr_spec}=30nC$, $I_{rr_spec}=25A$.

5.5.1 Voltage Source Drive Model Verification

Curves of total switching loss as a function of: (a) load current, (b) driver supply voltage and (c) common source inductance (assuming matched inductances; i.e. $L_{s1}=L_{d1}=L_{s2}=L_{d2}$) for the proposed model, Spice simulation and the conventional model are given in Figure 5.19(a)-(c). The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.5W for all conditions. In Figure 5.19, it is noted that the conventional model does a very poor job predicting the total switching loss in all three cases, but in particular as total circuit inductance increases. Specifically, at 1000pH in Figure 5.19(c), the conventional model predicts 2.0W loss, while the Spice results indicate total switching loss of 6.3W – a difference of 4.3W. The results also show that the total switching loss can be reduced by increasing V_{cc} . However, for $V_{cc}>8V$, the reduction is not significant.

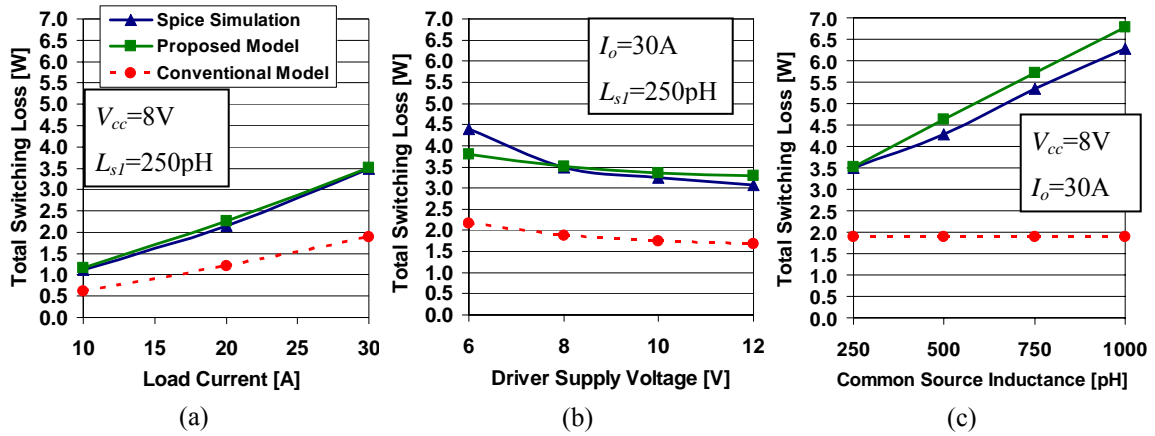


Figure 5.19 Total switching loss at 1MHz, 12V input as a function of: (a) load current ($V_{cc}=8V$, $L_{sl}=250pH$), (b) driver supply voltage ($I_o=30A$, $L_{sl}=250pH$) and (c) common source inductance ($V_{cc}=8V$, $I_o=30A$)

Curves of the turn on and turn off switching loss components loss as a function of (a) load current, (b) driver supply voltage and (c) common source inductance for the proposed model, Spice simulation and the conventional model are given in Figure 5.20(a)-(c) and Figure 5.21(a)-(c), respectively. The proposed model follows the trends of the Spice simulation results. In particular, the proposed model correctly predicts that the turn off loss increases with common source inductance since T_f increases significantly with L_{sl} . In the conventional model, turn off switching loss remains constant with common source inductance leading to an error in predicted loss of over 4.6W at 1000pH in Figure 5.21(c). The results also show that turn on loss decreases with V_{cc} , as expected since increasing V_{cc} provides increasing driver source current. In contrast, the turn off loss remains constant with V_{cc} , since the driver sink current is determined by V_{pl_off} .

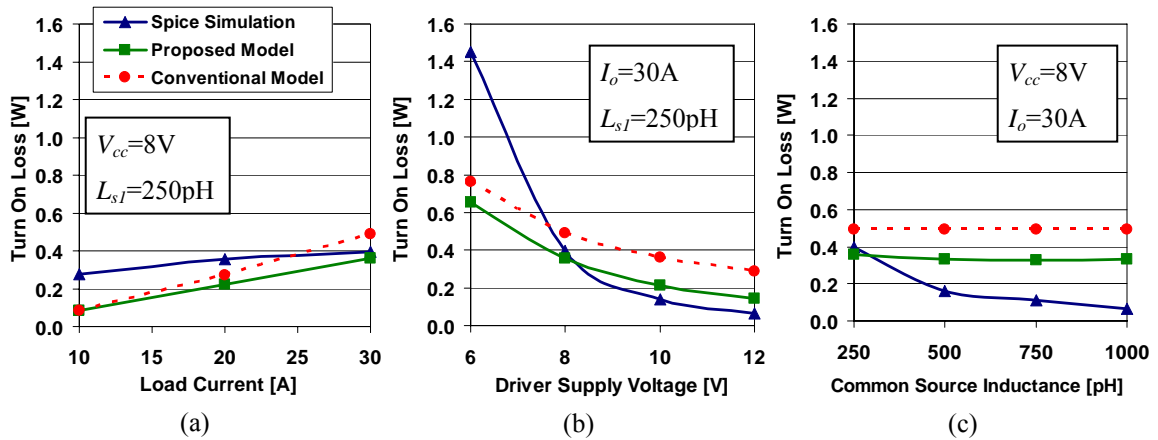


Figure 5.20 Turn on switching loss at 1MHz, 12V input as a function of: (a) load current ($V_{cc}=8V$, $L_{s1}=250pH$), (b) driver supply voltage ($I_o=30A$, $L_{s1}=250pH$) and (c) common source inductance ($V_{cc}=8V$, $I_o=30A$)

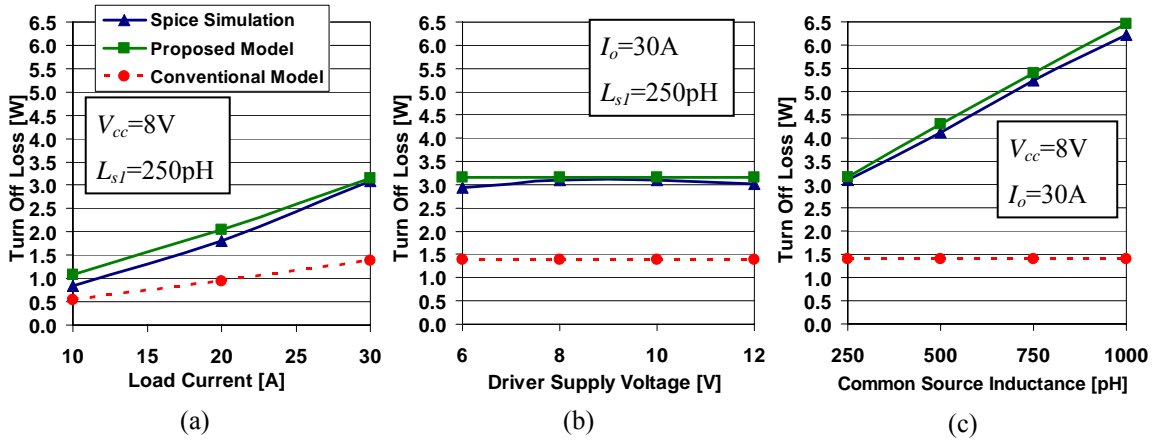


Figure 5.21 Turn off switching loss at 1MHz, 12V input as a function of: (a) load current ($V_{cc}=8V$, $L_{s1}=250pH$), (b) driver supply voltage ($I_o=30A$, $L_{s1}=250pH$) and (c) common source inductance ($V_{cc}=8V$, $I_o=30A$)

5.5.2 Current Source Drive Model Verification

Curves of total switching loss as a function of: (a) load current, (b) driver supply current and (c) common source inductance (assuming matched inductances; i.e. $L_{s1}=L_{d1}=L_{s2}=L_{d2}$) for the proposed model, Spice simulation and the conventional model are given in Figure 5.22(a)-(c). The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.5W under all loss conditions. In Figure 5.22, it is

noted that the conventional model does a poor job predicting the total switching loss in all three cases, but in particular as total circuit inductance increases.

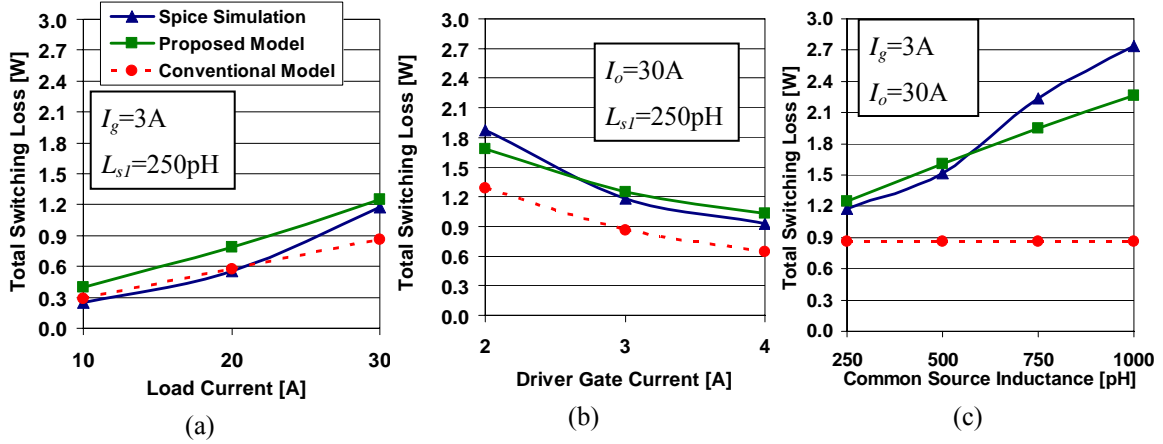


Figure 5.22 Total switching loss at 1MHz, 12V input as a function of: (a) load current ($I_g=3A$, $L_{sI}=250pH$), (b) driver supply current ($I_o=30A$, $L_{sI}=250pH$) and (c) common source inductance ($I_g=3A$, $I_o=30A$)

Curves of the turn on and turn off switching loss components loss as a function of: (a) load current, (b) driver supply current and (c) common source inductance for the proposed model, Spice simulation and the conventional model are given in Figure 5.23(a)-(c) and Figure 5.24(a)-(c). In all cases, the proposed model follows the trends of the Spice simulation results. In particular, it is noted that the proposed model predicted turn on loss decreases with increasing common source inductance, while the turn on loss remains constant for the conventional model. Furthermore, the model correctly predicts that the turn off loss increases with common source inductance. In the conventional model, turn off switching loss remains constant with common source inductance leading to an error in predicted loss of over 2W at 1000pH in Figure 5.24(c). It is also noted that the total switching loss is reduced significantly with current source drive to 1.2W (at $I_o=30A$, $I_g=3A$ and $L_{sI}=250pH$), compared to 3.5W (at $I_o=30A$, $V_{cc}=8V$ and $L_{sI}=250pH$) with conventional voltage source drive.

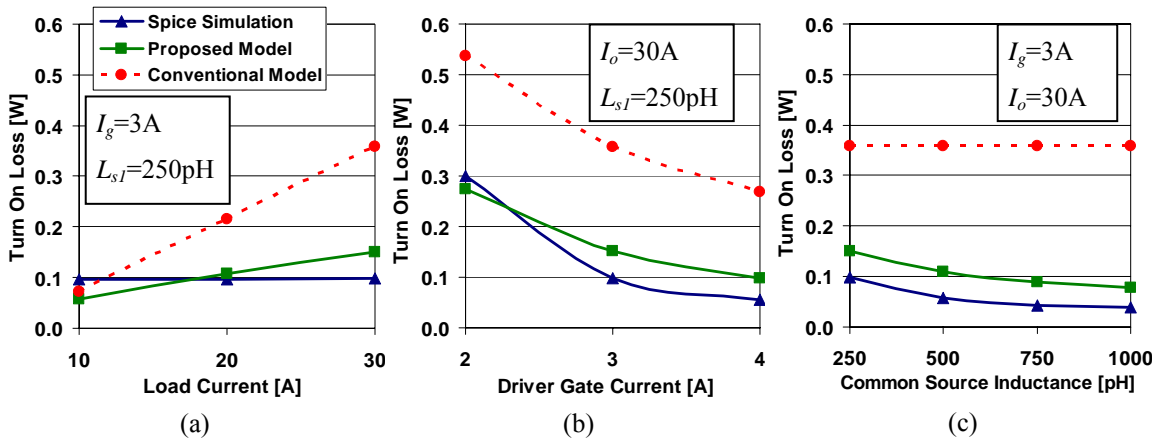


Figure 5.23 Turn on switching loss at 1MHz, 12V input as a function of: (a) load current ($I_g=3A$, $L_{s,l}=250pH$), (b) driver supply current ($I_o=30A$, $L_{s,l}=250pH$) and (c) common source inductance ($I_g=3A$, $I_o=30A$)

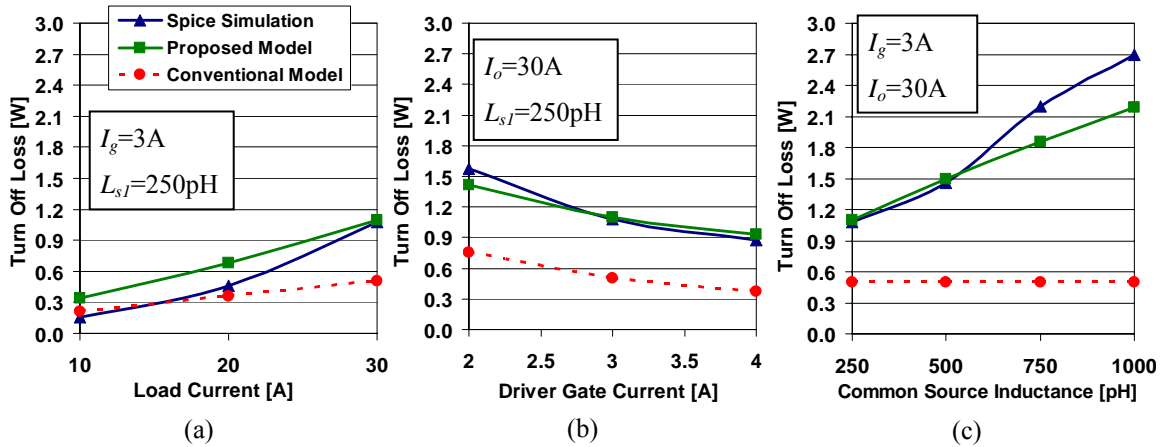


Figure 5.24 Turn off switching loss at 1MHz, 12V input as a function of: (a) load current ($I_g=3A$, $L_{s,l}=250pH$), (b) driver supply current ($I_o=30A$, $L_{s,l}=250pH$) and (c) common source inductance ($I_g=3A$, $I_o=30A$)

5.6 Experimental Results

Experimental results were presented in section 5.2 to aid in demonstrating the switching loss characteristics as load and common source inductance change. These results were presented at low frequency with a large inductance wire introduced in series between the source and common point on the driver in order to measure the HS MOSFET current and demonstrate the trends. However, since probing the MOSFET current is impractical in a real voltage regulator with good

layout, therefore, the actual switching loss in the prototype cannot be measured, so a direct comparison between the modeled switching loss and actual switching loss cannot be made.

Given the constraints on measuring actual switching loss, another method to gauge the accuracy of the proposed model is to use it in a loss analysis file that estimates the switching loss, other loss and total loss for a synchronous buck voltage regulator and compare it to the total loss in the real circuit. This analysis has been completed for both voltage source drive and current source drive and the total loss in the design file has been compared to the total measured loss of the circuit by subtracting the load power from the input power. These comparisons are included in the following sub-sections.

Circuit parameters: 1MHz switching frequency; 12V input; 1.3V output; 330nH buck inductor; $V_{cc}=10V$; IRF6617 HS MOSFET: $g_{fs}=39S$, $V_{th}=1.85V$, $C_{rss1_spec}=160pF$ (@ $V_{ds1_spec}=15V$), $C_{oss_spec1}=450pF$ (@ $V_{ds1_spec}=15V$), $C_{iss1_spec}=1300pF$ (@ $V_{ds1_spec}=15V$); and IRF6691 SR MOSFET; $L_{s1}=L_{d1}=L_{s2}=L_{d2}=500pH$ (model). Driver parameters: UCC27222 driver (experimental); $R_{hi}=1.8\Omega$, $R_{lo}=1.8\Omega$, $R_g=1\Omega$, $R_{ext}=0\Omega$ (model). Current source driver parameters: 3A gate current, 68nH inductor for the HS MOSFET, 1.3A gate current, 307nH inductor for the SR, NDS351AN driver switches.

5.6.1 Experimental Validation of the Voltage Source Drive Model

The estimated synchronous buck VR losses and model predicted switching loss as a function of load current is compared to the experimentally measured loss in Figure 5.25 for the voltage source driver. Good agreement is achieved between the loss predicted by the model and the actual loss of the voltage regulator, with the accuracy within 0.7W over the entire load range.

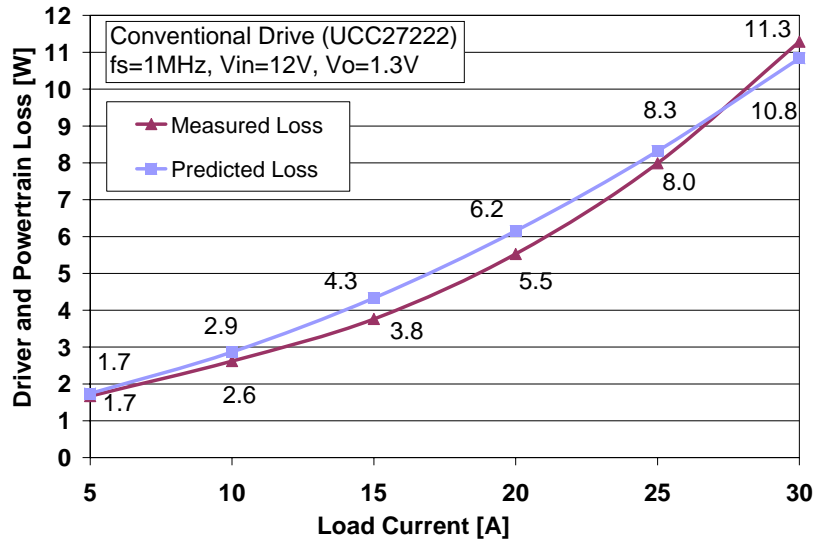


Figure 5.25 Comparison of total loss predicted and measured for voltage source drive (UCC27222, $f_s=1\text{MHz}$, $V_{in}=12\text{V}$ and $V_o=1.3\text{V}$)

A loss breakdown of the estimated losses used to generate the model predicted loss in Figure 5.25 is given in Figure 5.26 for 25A load current. The only losses that can be experimentally measured are the gate and driving power and the input power, which includes the remaining losses (i.e. all except gate and driving) in Figure 5.26.

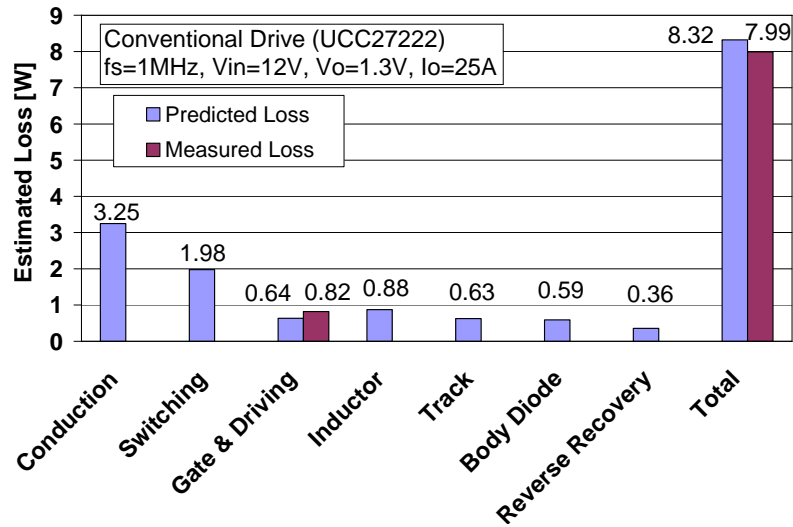


Figure 5.26 Loss breakdown of the losses predicted and comparison to the measured gate and total losses for voltage source drive (UCC27222, $f_s=1\text{MHz}$, $V_{in}=12\text{V}$ and $V_o=1.3\text{V}$)

5.6.2 Experimental Validation of the Current Source Drive Model

The estimated synchronous buck VR losses and model predicted switching loss as a function of load current is compared to the experimentally measured loss in Figure 5.27 for the current source driver. Good agreement is achieved between the loss predicted by the model and the actual loss of the voltage regulator, with the accuracy within 1W over the entire load range.

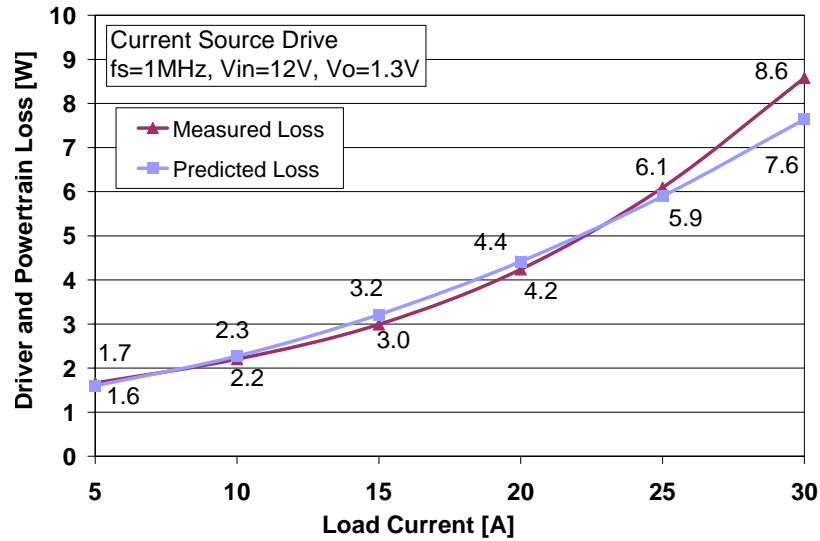


Figure 5.27 Comparison of total loss predicted and measured for current source drive ($f_s=1\text{MHz}$, $V_{in}=12\text{V}$ and $V_o=1.3\text{V}$)

A loss breakdown of the estimated losses used to generate the model predicted loss in Figure 5.27 is given in Figure 5.28 for 25A load current.

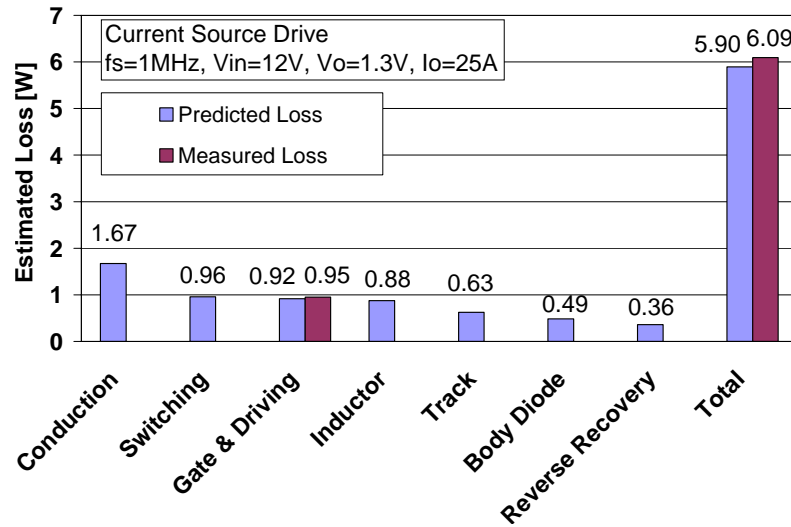


Figure 5.28 Loss breakdown of the losses predicted and comparison to the measured gate and total losses for current source drive ($f_s=1\text{MHz}$, $V_{in}=12\text{V}$ and $V_o=1.3\text{V}$)

5.7 Conclusions

The switching loss characteristics and behavior in a high frequency synchronous buck VR have been reviewed. The key points to note are: 1) T_r at turn on is dictated by the voltage falling time, which is dictated by the MOSFET parasitic capacitances and current driving capability of the driver, 2) T_f at turn off is dictated by the current falling time, which is dictated by the MOSFET parasitic capacitances and current driving capability of the driver and by the circuit parasitic inductances, 3) The parasitic inductances act as a current snubber at turn on to reduce turn on loss, but prolong T_f to increase turn off loss.

Following the demonstrated switching loss characteristics, a new practical analytical switching loss model has been proposed for voltage source drivers and current source drivers. The model can accurately predict the switching loss in a high frequency synchronous buck voltage regulator using relatively simple closed-form equations. This enables engineers to use a spreadsheet design file to estimate losses in their designs. The proposed model uses piecewise linear approximations of the actual v_{ds1} and i_{ds1} switching waveforms. The linearized v_{ds1} and i_{ds1}

switching waveforms are then used to provide simple expressions for the turn on and turn off loss. Neglected in other models, the reverse recovery current is included in the turn on switching loss calculation. Circuit parasitic inductances are included in the rise and fall time calculations.

To verify the proposed model, the voltage source drive and current source drive versions were compared to Spice simulation results. It was demonstrated that the proposed model follows the trends in turn on and turn off switching loss for variations in load current, driver supply voltage, driver supply current and total circuit inductance. The accuracy of the proposed models was demonstrated to be within 0.5W between the calculated and simulated values for the voltage source driver and within 0.5W for the current source driver. Following the simulation results, the proposed model was used in a loss analysis file to accurately predict the total circuit loss for both the voltage and current source drivers. The total predicted circuit loss was within 0.7W of the measured loss for the voltage source driver and within 1.0W of the measured loss for the current source driver operating in a synchronous buck VR at 12V input, 1.3V output and 1MHz switching frequency.

Chapter 6

Frequency Dithering Control for Resonant Converters

6.1 Introduction

It is desirable to implement converter control with digital techniques in order to be able to avoid using high frequency analog components and more importantly to implement complex control algorithms, provide adaptability, programmability and reduce sensitivity to process and parameter variations. Furthermore, since resonant power conversion techniques are best suited for high frequency applications in the MHz in order to minimize switching loss, therefore, digital control techniques are required for resonant converters. However, the choice of available control techniques for resonant converters is different than that for PWM type converters. With variable frequency control, the output voltage is controlled by the switching frequency. With phase-shift control [24], the output voltage is controlled by the phase shift between bridge legs in a full-bridge topology. With asymmetrical control [22],[23], the duty cycle is used to control the output voltage.

The phase-shift technique is generally not ideal for variable input applications since ZVS is not always achieved. In contrast, the variable frequency and asymmetrical PWM techniques can be better suited for variable input applications, but the asymmetrical technique suffers from three drawbacks: 1) with analog control, the controller requires a comparator, which introduces significant delay for 10MHz switching frequency operation, 2) it can only be used with a half-bridge type inverter, and 3) intellectual property issues limit its application. Given this information, a control method is required for variable frequency resonant converters that can be implemented digitally with suitable resolution at realistically achievable digital clock frequencies under 200MHz.

This chapter proposes a control method that can achieve these objectives by exploiting the non-linearity inherent in resonant power conversion along with dithering. The proposed control method is frequency dithering control.

In section 6.2, the basic idea of frequency dithering is presented. A resolution analysis is presented in section 6.3 and simulation results are presented in section 6.4. The conclusions are presented in section 6.5.

6.2 Basic Idea of Frequency Dithering

The basic idea of frequency dithering control is to regulate the output voltage by averaging pre-determined sets of frequencies that can differ by an amount equal to, or greater than one least significant bit (LSB). One LSB is the frequency difference between the highest and second highest frequencies in a frequency set. For example, for a frequency set of three frequencies of increasing magnitude, f_1 , f_2 and f_3 , one LSB corresponds to $\Delta f_{LSB} = f_3 - f_2$.

With greater than one LSB dither, if a controller can only generate three frequencies, f_1 , f_2 and f_3 (e.g. 6MHz, 7MHz and 8MHz) for a given frequency range, then there are seven unique frequency combinations out of a possible twenty-seven, as shown in Table 6.1. Other frequency sets, such as $\{f_1, f_2, f_1\}$ are redundant (i.e. $\{f_1, f_2, f_1\}$ is redundant with $\{f_1, f_1, f_2\}$). However, with one LSB dither, there are only seven unique frequency combinations shown in the right hand column of Table 6.1. This reduced number of usable sequences is clear in Table 6.1, where frequency sets $\{f_1, f_1, f_3\}$, $\{f_1, f_2, f_3\}$ and $\{f_1, f_3, f_3\}$ cannot be used with LSB dither. Non dithered sequences in Table 6.1 are highlighted.

Table 6.1 Comparison of proposed dither sequences and LSB dither sequences

Proposed Unique Dither Sequences	LSB Dither Sequences
$\{f1, f1, f1\}$	$\{f1, f1, f1\}$
$\{f1, f1, f2\}$	$\{f1, f1, f2\}$
$\{f1, f1, f3\}$	
$\{f1, f2, f2\}$	$\{f1, f2, f2\}$
$\{f1, f2, f3\}$	
$\{f2, f2, f2\}$	$\{f2, f2, f2\}$
$\{f1, f3, f3\}$	
$\{f2, f2, f3\}$	$\{f2, f2, f3\}$
$\{f2, f3, f3\}$	$\{f2, f3, f3\}$
$\{f3, f3, f3\}$	$\{f3, f3, f3\}$

The advantage of dithering by more than one LSB is that the resolution of the output voltage can be improved greater than it can for one LSB dither. In the example given, the improvement is a factor greater than three ($10\text{sequences}/3\text{frequencies}=3.3$) while not increasing the controller clock frequency. With one LSB dither, the resolution is only improved by a factor slightly greater than two ($7\text{sequences}/3\text{frequencies}=2.3$).

If we assume that Δf is constant for the frequency set ($\Delta f=f3-f2=f2-f1$), then it can be shown that set pairs $\{f1, f1, f3\}$ and $\{f1, f2, f2\}$, $\{f1, f2, f3\}$ and $\{f2, f2, f2\}$, and $\{f1, f3, f3\}$ and $\{f2, f2, f3\}$ will have the same average frequencies for each set in each pair. However, due to the non-linearity of the DC gain of resonant converters, these sets will not generate the same output voltages. This behaviour can be understood by examining Figure 6.1, which is a plot of the DC gain of an isolated Full-Bridge LCC type resonant converter (circuit topology given in Figure 6.4). The x-axis represents the switching frequency, f_s , normalized with respect to the series resonant frequency. The y-axis represents the DC gain (i.e. input voltage-to-DC output voltage ratio, V_o/V_{in}). The curve is symmetrical about the dotted line, however in order to minimize frequency dependent losses, these converters are usually operated in the ZVS region on the right side of the dotted line. Furthermore, since DC-DC converters are intended to operate with fixed output voltages, it is very clear that the frequency can be adjusted as the input voltage changes in

order to regulate the output voltage. Varying the frequency can also compensate for load current changes. The non-linearity is very clear on the right side of the curve.

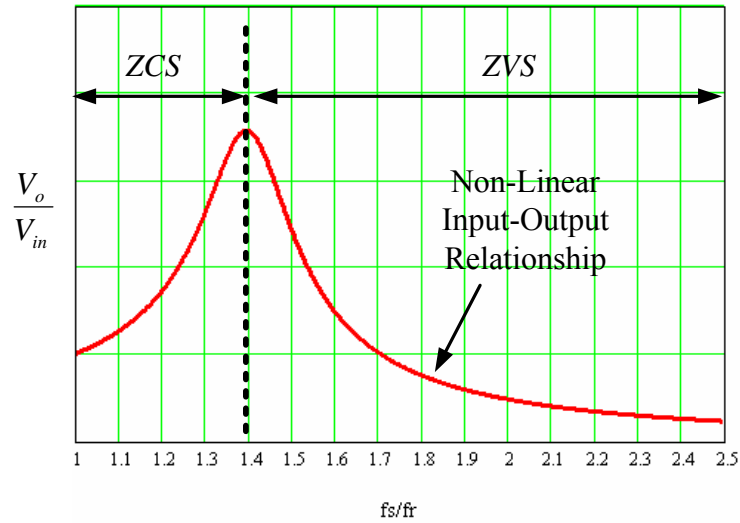


Figure 6.1 Typical DC gain relationship for an LCC resonant converter

A significant advantage of the proposed method is that frequency sets with the same average frequency will not produce the same output voltages, so the proposed method can achieve higher resolution, or operate at a lower clock frequency than PWM dithering. This behaviour can be observed in Figure 6.2. With one LSB dither, the output voltage data points, represented by circles, are evenly spread. However, by using frequency dithering greater than one LSB, additional data points are obtained, represented by the asterisks, so that the output voltage characteristic has clusters of points near the LSB dither points.

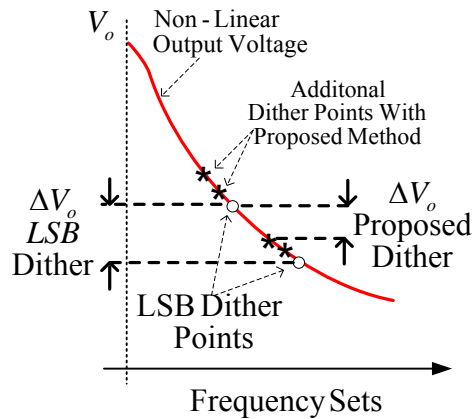


Figure 6.2 Output voltage characteristic

When dithering by amounts greater than the LSB, the additional frequency sets contain individual frequencies that are greater than and lower than those in the LSB sequences. e.g. With LSB dither, set {10MHz, 10MHz, 10MHz, 10.5MHz} has an average frequency of 10.125MHz, and the corresponding additional set with greater than LSB dither is {9.5MHz, 10MHz, 10MHz, 11MHz} with an average value of 10.125MHz. In this case, the set dithered by an amount greater than one LSB yields a higher output voltage than the LSB dither set. This behaviour occurs due to the non-linearity of the resonant converter resonant tank. Since the slope of the converter gain is steeper at the lowest frequency, in this case 9.5MHz, and flattest for the highest frequency, 11MHz, therefore the 9.5MHz frequency tends to increase the output voltage by an amount slightly greater than that with LSB dither. This behaviour yields the additional data points, marked by asterisks, clustered above the LSB dither points in Figure 6.2. Given this analysis, it is clear that the proposed method can achieve greater resolution (smaller ΔV_o) than one LSB dither.

6.3 Resolution Analysis

Since resonant converters are non-linear, solving resolution calculations is much more complex than for PWM converters. In order to calculate the required resolution, we need to obtain the frequency equivalent version of (2.23). For a resonant converter, the output voltage is

a complex function of frequency. For example, using fundamental analysis, for a full-bridge converter with a turns ratio of $n:1$ and an LCC resonant tank, the output voltage is given by (6.1), where f is the relative frequency of resonant frequency-to-switching frequency (f_s/f_r); L_s is the series inductance; C_s is the series capacitance; C_p is the parallel capacitance and Q is the quality factor of the load, which is given by (6.2).

$$|V_o(f)| = \frac{8V_{in}}{n\pi^2} \left| \frac{1}{1 + \frac{L_s}{L_m} \left(1 - \frac{1}{f^2}\right) + \frac{C_p}{C_s} (1 - f^2) + jQ \left(f - \frac{1}{f}\right)} \right| \quad (6.1)$$

$$Q = \frac{16f_r L_s I_o}{n^2 \pi V_o} \quad (6.2)$$

In order to determine the resolution and the number of bits required for the ADC, we need to determine $1/\Delta f$. Assuming ΔV_o is small, we can calculate the digital resolution requirement by differentiating $|V_o(f)|$ with respect to f , evaluating at $f=f_{min}$ and then dividing both sides by the known required output voltage resolution (e.g. 10mV), ΔV_o , as given by (6.3).

$$\frac{1}{\Delta f} \approx \frac{1}{df} \approx \left. \frac{d|V_o(f)|}{df} \right|_{f=f_{min}} \frac{1}{\Delta V_o} \quad (6.3)$$

The number of bits required for the ADC, N_{ADC} , is given by (6.4).

$$N_{ADC} = \log_2 \left(\frac{1}{\Delta f} \right) = \log_2 \left(\left. \frac{d|V_o(f)|}{df} \right|_{f=f_{min}} \frac{1}{\Delta V_o} \right) \quad (6.4)$$

In order to avoid limit cycling [41], the number of bits required for the DFM, is at least one bit greater than the ADC, so N_{DFM} is given by (6.5).

$$N_{DFM} = N_{ADC} + 1 \quad (6.5)$$

Therefore, in order to achieve the desired output voltage resolution, the clock frequency requirement, f_{clock} , is given by (6.6).

$$f_{clock} = 2^{N_{DFM}} f_s \quad (6.6)$$

Since (6.1) is non-linear, the resolution is non-linear. In order to meet the resolution specification for the load, the resolution requirement should be designed to meet the specification in the worst case, which occurs around the point of greatest slope of the DC gain characteristic.

A typical set of curves of the DC gain for an LCC resonant full-bridge is given in Figure 6.3. The two curves are given for the no load (right curve) and full load (left curve). For a given Δf , the worst case ΔV_o , occurs around the point of greatest slope, which occurs at low line (35V input) and no load (Q_{NL}). This is clear in the figure since $\Delta V_{o_NL} > \Delta V_{o_FL}$. Therefore, N_{ADC} should be selected to meet the ΔV_o specification for this condition, which occurs at the minimum steady-state frequency, f_{min} , minimum input voltage and no load.

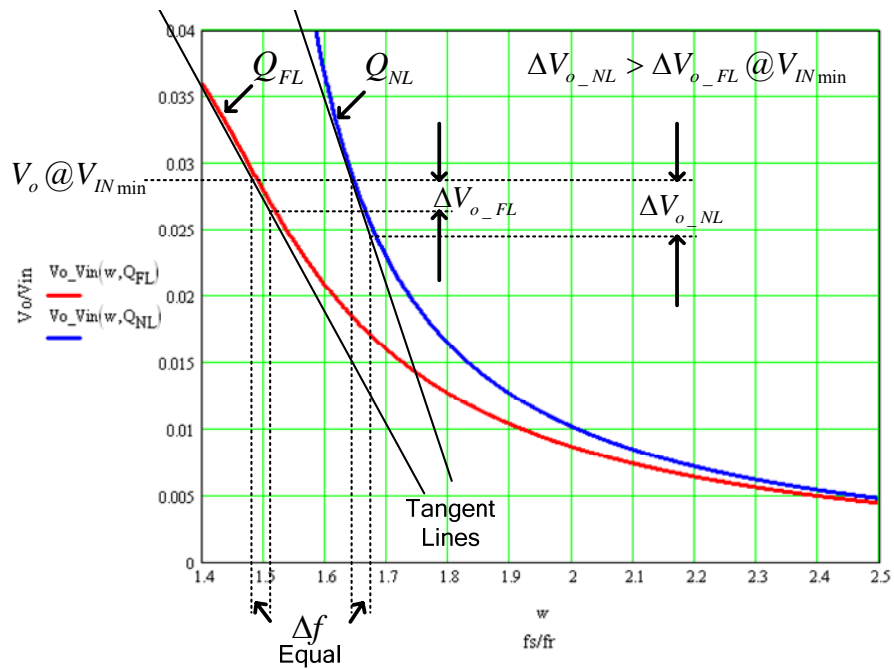


Figure 6.3 Typical curves for the DC gain of an LCC resonant full-bridge illustrating the worst case resolution at low line and no load

6.4 Simulation Results

PSIM 5.0 was used to simulate the proposed frequency dithering technique. PSIM is a power simulation software package produced by Powersim [60]. The objective of the simulation is to demonstrate that the output voltage can be controlled using the proposed technique.

The circuit used in the simulation is given in Figure 6.4. The topology is a full-bridge LCC resonant converter with current doubler rectifier. The series resonant frequency is 6.1MHz. Square wave voltage sources of varying duty cycles and delay elements were used to generate the dithered frequencies for frequency sets consisting of four frequencies between 9MHz and 11.5MHz at 0.5MHz intervals. For example, a typical set would be {10MHz, 10MHz, 10MHz, 10.5MHz}.

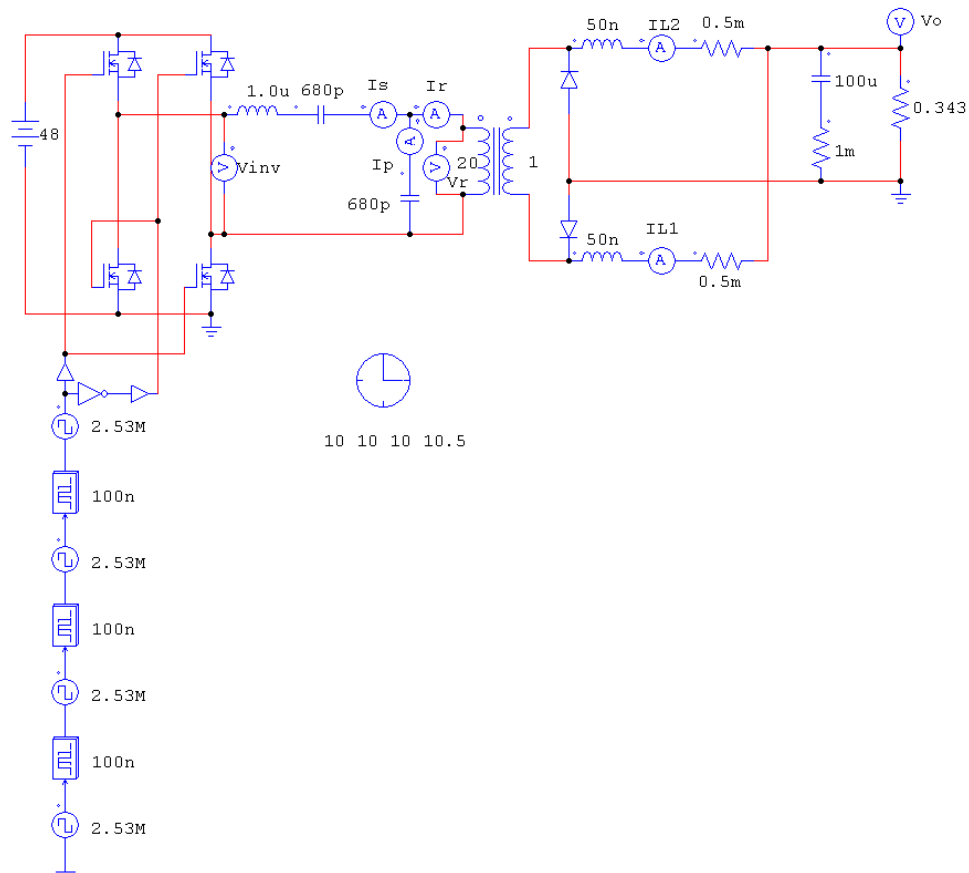


Figure 6.4 Simulation schematic for the proposed frequency dithering technique

The open loop steady-state waveforms for the frequency set {10MHz, 10MHz, 10MHz, 10.5MHz} are given in Figure 6.5. The waveforms include the output voltage, inverter output voltage, series resonant current and filter inductor currents. Since the series resonant current lags the inverter output voltage, ZVS can be achieved. It is also noted, that an ideal nominal duty cycle of 50% is used at all times in the proposed algorithm. The circuit was simulated at full load and 48V input. It is clear that this frequency set can regulate the output voltage near 1.2V. The most apparent ripple content occurs at a frequency equal to approximately one quarter of the average frequency in the set, which is 2.53MHz in this example. However, it is noted that the amplitude of this ripple is quite small at 1.3mV peak-to-peak.

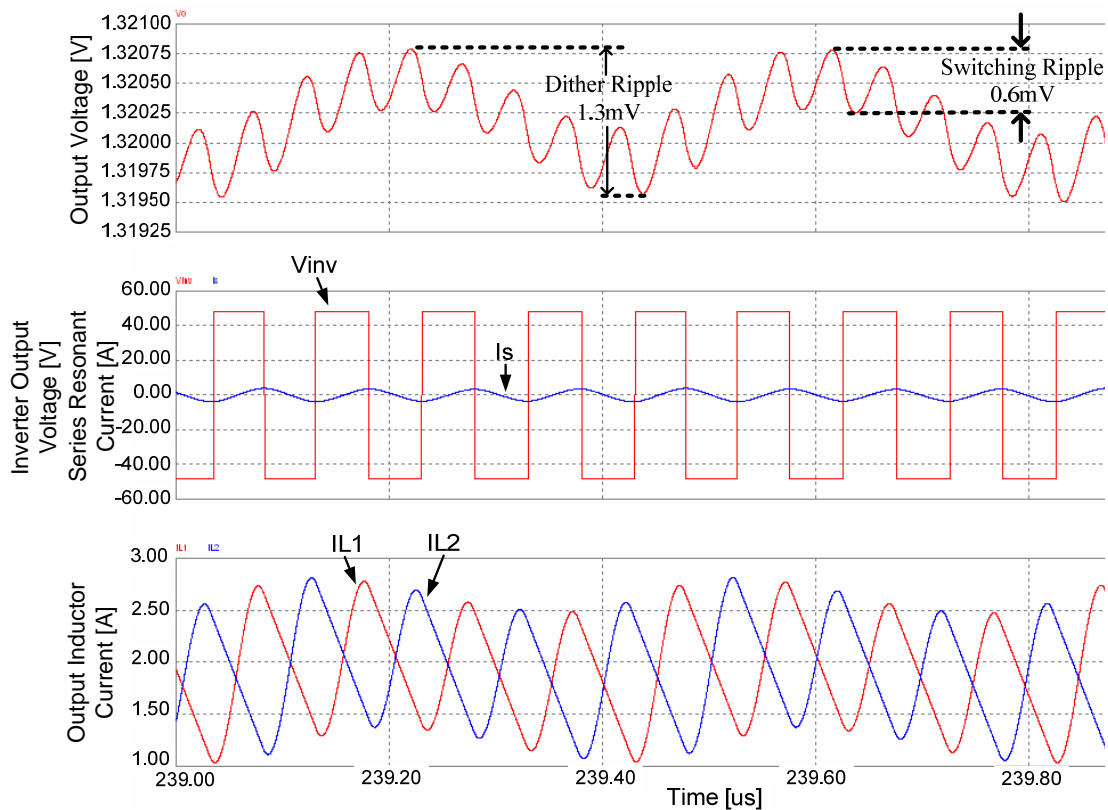


Figure 6.5 Waveforms of the dither sequence {10MHz, 10MHz, 10MHz, 10.5MHz} (top: output voltage, second: inverter output voltage and series resonant current; ZVS can be maintained, third: filter inductor currents); dither ripple content is 1.3mV pp at 2.53MHz and switching ripple is 0.6mV

The impact of the low frequency content due to the dithering is minimal in all waveforms except for the output voltage. This is expected since the resonant tank filters the low frequency content and inverter high frequency harmonics while allowing the switching frequency content to pass through. However, since the output filter is a double-pole low-pass filter, it attenuates the high frequency switching content better than the lower frequency dither content. As a result of this problem, a larger output capacitance is required in order to filter the dither frequency content. Fortunately, this is not a significant problem since additional output capacitance is usually required to meet the dynamic requirements. It is also noted that the dither frequency content is minimal for the volt-seconds applied to the output filter inductors, which allows the inductor to be sized according to the lowest switching frequency in the dither sequence. This result is beneficial for both the converter size and dynamic response.

Curves of the output voltage regulation from the simulation are given in Figure 6.6 for 10% load (3.5A) and in Figure 6.7 for full load at 35A. The two curves on each graph represent the minimum input voltage condition, 35V (circles) and the maximum input voltage condition of 75V (triangles). The curves follow the shape of that given in Figure 6.1. It is clear that the output voltage can be regulated at 1.2V for all load and input conditions.

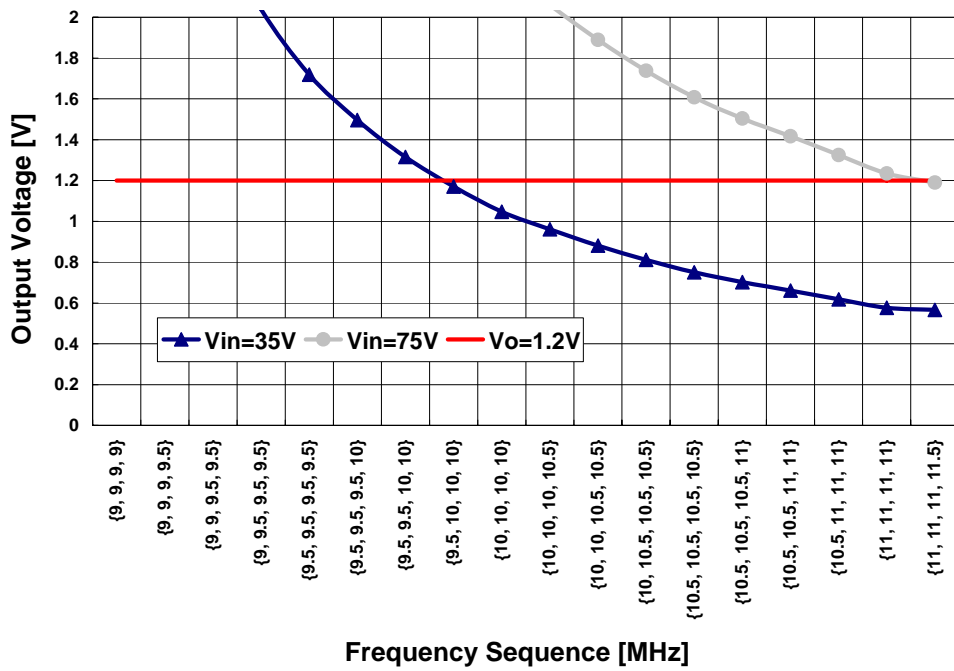


Figure 6.6 Open loop output voltage curves for 35V and 75V input at 10% load (3.5A); $L_s=1\mu\text{H}$, $C_s=680\text{pF}$, $C_p=680\text{pF}$, $n=20:1$, 10% load= $1.2\text{V}/3.5\text{A}=0.0343\text{ohms}$

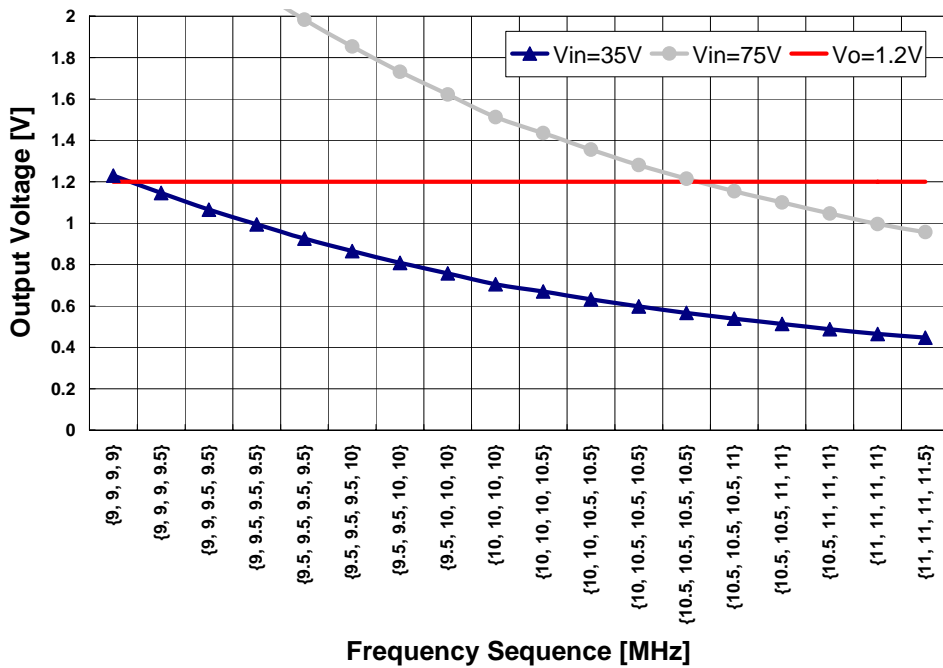


Figure 6.7 Open loop output voltage curves for 35V and 75V input at full load (35A); $L_s=1\mu\text{H}$, $C_s=680\text{pF}$, $C_p=680\text{pF}$, $n=20:1$, 10% load= $1.2\text{V}/35\text{A}=0.343\text{ohms}$

6.5 Conclusions

At 10MHz switching frequencies resonant converters must be used to minimize switching loss. However, it is difficult to design a low cost voltage controlled oscillator for variable frequency control, or a low cost comparator for phase-shift and asymmetrical controllers. Therefore, a new variable frequency control method for resonant converters has been proposed that is suitable for future high switching frequency applications at 10MHz. The proposed method can be implemented digitally in order to take advantage of the numerous benefits of digital control. The method uses frequency dithering to reduce the clock frequency demands of the digital controller. Using frequency dithering to regulate the output voltage of resonant converters enables the use of dithering by amounts greater than one LSB by exploiting the non-linear DC gain characteristic of resonant converters.

An analysis has been presented in order to determine the resolution of the proposed method. In addition, simulation results have been presented in order to demonstrate that the proposed method can regulate the output voltage over a wide input voltage and load current range.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

In the future, most low power DC-DC switching converters for communications and computers will operate at switching frequencies in the 1-10MHz range in order to achieve greater power density and improved transient response. To meet the next generation requirements of these applications, four new ideas have been proposed in this thesis.

7.1.1 A Current Source Gate Driver Achieving Switching Loss Reduction and Gate Energy Recovery at 1MHz

The first contribution is a new current source gate drive circuit for ground referenced power MOSFETs. The proposed circuit achieves quick turn on and turn off transition times to reduce switching loss in power MOSFETS. In addition, it can recover a portion of the QV gate energy normally dissipated in a conventional driver. The circuit consists of four controlled switches and a small inductor (100nH or less, typical). The driver can operate effectively over a wide range of duty cycles while providing a near constant gate current. The driver provides superior performance in comparison to conventional voltage source drivers and solves the problems of existing resonant gate drivers. Demonstrated loss reduction of 24.8% are presented at 5V input and 10V output at 5A load current in comparison to a conventional voltage source driver for a boost converter switching at 1MHz.

The content of this chapter is subject to patent pending for U.S. patent number US 2006/0170043 A1 and International patent number WO 2006/079219 A1. This body of work is in press in the following journals:

[1] W. Eberle, Z. Zhang, Y.F. Liu and P.C. Sen, "A Current Source Gate Driver Achieving

Switching Loss Savings and Gate Energy Recovery at 1-MHz,” IEEE Trans. Power Electron., TPEL-2007-05-0257.

[2] W. Eberle, Y.F. Liu and P.C. Sen, “A Novel High Efficiency Resonant Gate Driver with Efficient Energy Recovery and Low Circulating Current” IEEE Trans Industrial Electron., TIE00485-2005.

7.1.2 A High Efficiency MHz Synchronous Buck Voltage Regulator with Current Source Gate Driver

The second contribution is a new high efficiency 1MHz synchronous buck voltage regulator using an improved current source driver. The proposed circuit achieves quick turn on and turn off transition times to reduce switching loss in the high side MOSFET of a synchronous buck converter. The driver circuit consists of two sets of four control switches and two small current source inductors and it can drive both the high side and synchronous MOSFETs in a synchronous buck voltage regulator. A complex programmable logic device was used to generate the gating waveforms and a pulsed latch level shift circuit was presented to drive the gate voltages of the driver switches. The level shift circuit permits the use of driver supply voltages greater than logic level, which can reduce conduction losses. Experimental results demonstrate a loss reduction of 21.9% at 1.5V output, 24% at 1.3V output, 34% at 1.2V output and 27.6% at 1.0V output in comparison to an identical synchronous buck voltage regulator with conventional driver at 12V input voltage, 30A load current and 1MHz switching frequency. In addition, it was demonstrated that if implemented in a 120A multiphase VR, the proposed driver would eliminate one of the required buck phases, yielding a significant potential cost savings.

The content of this chapter is subject to patent pending in the U.S. for patent number US 2006/0170043 A1 and International patent number WO 2006/079219 A1. This work has been published at the 2007 Power Electronics Specialists Conference and has been submitted to the

7.1.3 A Practical and Accurate Switching Loss Model for Buck Voltage Regulators

In the third contribution, a new practical analytical switching loss model was proposed for voltage source drivers and current source drivers. The model accurately predicts the switching loss in a high frequency synchronous buck voltage regulator using relatively simple closed-form equations. The model enables engineers to use a spreadsheet design file to estimate losses in their synchronous buck voltage regulator designs. Neglected in other models, the reverse recovery current is included in the turn on switching loss calculation. Circuit parasitic inductances are included in the rise and fall time calculations. Simulation and experimental results demonstrate the accuracy of the proposed models.

The content of this chapter has been accepted for publication at the 2008 Applied Power Electronics Conference and has been submitted to the IEEE Transactions on Power Electronics.

7.1.4 Frequency Dithering Control for Resonant Converters

The final contribution is a new variable frequency digital control method for resonant converters, which is suitable for future applications switching at 10MHz. At 10MHz switching frequencies resonant converters must be used to minimize switching loss. With analog control, it is difficult to design a low cost voltage controlled oscillator for variable frequency control, or a low cost comparator for phase-shift and asymmetrical controllers. Therefore, a new variable frequency digital control method for resonant converters has been proposed that is suitable for future high switching frequency applications at 10MHz. The method uses frequency dithering to reduce the clock frequency demands of the digital controller. Using frequency dithering to regulate the output voltage of resonant converters enables the use of dithering by amounts greater than one LSB by exploiting the non-linear DC gain characteristic of resonant converters.

Simulation results demonstrate that the proposed method can regulate the output voltage over a wide input voltage and load current range.

7.2 Future Work

This sub-section outlines the possible future work for the thesis topics.

7.2.1 Current Source Gate Drivers

The proposed current source drivers in Chapters 3 and 4 have been implemented discretely. In order to be widely adopted by the power electronics marketplace, the drivers will need to be integrated into single discrete driver integrated circuits. This includes combining the logic, level shift circuits, dead time control and driver MOSFETS into a single package. In addition, for some applications, including MHz switching frequency synchronous buck voltage regulators, it might be possible to integrate the high side MOSFET driver inductor into the driver package, so potential inductor integration could be explored.

7.2.2 Switching Loss Modeling

The proposed switching loss model has been presented for high frequency synchronous buck converters. Since other non-isolated soft switching topologies have been proposed for voltage regulator applications, the switching loss model could be extended to these topologies to quickly and accurately predict the turn off loss for these topologies. In addition, the proposed model could be extended to isolated converter topologies, such as the active clamp forward and phase shift full-bridge, which are popular in telecommunications applications.

7.2.3 Frequency Dithering Control

The frequency dithering control method proposed is open-loop. In order to properly regulate the output voltage for a DC-DC converter, an algorithm must be developed to generate the

frequency sequences using the output voltage as the feedback variable.

Additional work will be required to further analyze the frequency-to-output voltage relation to determine the dithering requirements to achieve the required output voltage resolution. In addition, the low frequency dither content should be completely characterized, including its impact on the converter design.

In order to implement the proposed method, hardware design and component selection is necessary. To implement the method digitally, a Field Programmable Gate Array (FPGA) will be required and an ADC will have to be chosen.

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