

PHASE GENERATION AND MANIPULATION IN CMOS
INTEGRATED CIRCUITS

by

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Abstract

In this thesis three circuits are presented that demonstrate the creation and manipulation of various phases over a large bandwidth. Many systems demand the interoperability of various circuit blocks over a large frequency range in order to minimize costs. In addition, the use of low resistivity silicon facilitates a further reduction in costs. The circuits presented in this thesis demonstrate both these key concepts by using the conventional CMOS process in addition to operating over large bandwidths which is ideal for inclusion in any number of standard wireless systems.

A new novel balun is proposed that achieves wideband performance through the use of an external compensating capacitor to counter the effects of parasitic capacitances that reduce its effective bandwidth. An input stage common gate amplifier is then used to improve the return loss and provide additional gain. The fabricated active balun using the proposed circuit shows that the device performs with a 7.5 GHz bandwidth. In addition an excellent 16 dB return loss, -5.8 dBm compression point and 12 mW power consumption are also reported.

Following this, an inductorless quadrature oscillator is proposed using an artificial resonator composed of conventional OTA circuits in order to increase the tuning range. The measured tuning range was found to be 100 MHz. This circuit demonstrates the ability to use a synthetic resonator circuit as a method of achieving wide tuning. The measured phase noise of -97.7 dBc/Hz is on par with other inductorless oscillators found in literature.

Finally a wideband feedback quadrature generator is presented. Existing circuits

do not provide a wide frequency of operation and in addition are highly susceptible to variances in component values used. The result is that the fabricated system will not operate at its intended operating frequency. In order to mitigate this problem a RC-CR network was used in conjunction with two variable gain amplifiers that uses a feedback network to actively compensate the amplitude imbalance over a large frequency range. This new design first is of its kind and the resulting circuit is measured to have over a 4 GHz bandwidth while maintaining a ± 1 dB amplitude balance.

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Nomenclature

AC	Alternating Current
AWGN	Additive White Gaussian Noise
ADS	Advanced Design Simulator
BER	Bit Error Rate
C-band	Microwave devices operating between 1 to 2 GHz
CR	Capacitor-Resistor
CD	Common Drain amplifier
CG	Common Gate amplifier
CS	Common Source amplifier
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DC	Direct Current
DUT	Device under test
FFT	Fast Fourier Transform
FOM	Figure of Merit
GaAs	Gallium Arsenide
GSG	Ground signal ground
GSGSG	Ground signal ground signal ground
I	In phase
Im	Imaginary
IF	Intermediate Frequency

InP	Indium Phosphide
IRR	Image Rejection Ratio
LHP	Left Hand Plane
L-band	Microwave devices operating between 2 to 4 GHz
LO	Local Oscillator
MEMS	Micro-Electro-Mechanical Systems
MIM	Metal Insulator Metal
MMIC	Microwave Monolithic Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor Field Effect Transistor
OTA	Operational transconductance amplifier
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PMOS	P-type Metal Oxide Semiconductor Field Effect Transistor
PN	P-type N-type
Q	Quadrature Phase
QPSK	Quadrature Phase Shift Keying
RC	Resistor-Capacitor
Re	Real
RF	Radio Frequency
RHP	Right Hand Plane
S-band	Microwave devices operating between 4 to 8 GHz
S-Parameters	Scattering Parameters
Si	Silicon
SiGe	Silicon Germanium
SoC	System on Chip
SOLT	Short-open-load-through

VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
WiFi	Wireless Fidelity
A_d	Differential gain
C	Capacitor
C_{gc}	Gate to channel capacitance
C_{gd}	Gate to drain capacitance
C_{gs}	Gate to source capacitance
C_{ov}	Overlap capacitance
$\langle \delta\phi_{free}^2(\Omega) \rangle$	Oscillator's free running phase noise
$\langle \delta\phi_{inj}^2(\Omega) \rangle$	Stable oscillator's stand alone phase noise
$\langle \delta\phi_{lock}^2(\Omega) \rangle$	Phase noise of injection locked oscillator
ε	Amplitude error
ε_{ox}	Permittivity of the silicon oxide
ε_s	Energy spent per symbol
G	Ratio of output power over input power
g_m	Transconductance
I_D	DC Drain current
i_{out}	Output current
$\lambda/4$	Quarter wavelength
L	Inductor
L	Length of transistor
L_{eff}	Effective length of transistor
$L(f)$	Phase noise
$N_o/2$	Noise spectral density
P_c	Carrier power

P_n	Noise power
P_s	Probability of error
P_{sig}	Output signal power
$\Delta\phi$	Phase error
P_{1dB}	1 dB compression point
Φ_{detune}	Detuning phase
Q	Quality Factor
$Q(\dots)$	Gaussian probability distribution
R	Resistor
R_D	Resistance at the drain
R'_D	Equivalent resistance at the drain
R_L	Load resistance
r_o	Output resistance
R_p	Parasitic resistance
R_S	Resistance at the source
R'_S	Equivalent resistance at the source
t_{ox}	Thickness of silicon oxide
V_A	Early voltage
V_{DD}	DC drain voltage
V_{GS}	DC Gate to source voltage (large signal)
V_{gs}	AC Gate to source voltage (small signal)
V_{SS}	DC source voltage
v_{in}	AC voltage at the input (small signal)
v_o	AC voltage at the output (small signal)
V_t	Threshold voltage
W	Width of transistor
$\Delta\varpi$	Locking bandwidth

ω_o	Oscillation frequency
Z_{gd}	Gate to drain impedance
Z_{gs}	Gate to source impedance
Z_{in}	Input impedance
Z_o	Characteristic impedance

Chapter 1

Introduction

1.1 General Introduction

In many microwave systems there is a constant concern about the creation of a precise phase. This is especially true in many phase shift keying systems. The requirement of a precise phase will directly affect the bit error rates of any received or transmitted signal. In addition, for the creation of a balanced signal, a precise 180° phase is required. There exist many circuits that produce the required phases, but they deliver limited frequency performance far below expectations.

Conventional microwave circuit designs have historically depended on microstrip and coplanar waveguide circuits such as the Marchand balun and the branch line coupler to deliver the required phase. However the use of these devices are difficult to apply in integrated circuits at the radio frequency range because of their large wavelength. Furthermore the increasing trend of incorporating both digital and analog system onto a single die in order to produce a system on chip (SoC) system have motivated the use of low resistivity silicon substrates. Consequently the use of these lossy silicon substrates reduce the performance of microstrip and coplanar waveguide circuits and further discourage their application.

As a result, the use of lumped element circuits have been increasingly relied upon.

There exists several circuits for use in both quadrature generation and baluns, however they are limited to a specific frequency point. In addition, loose tolerances in the resistor values often results in a circuit designed for one specific frequency point to be manufactured at another.

In the area of wireless communications, various communication systems have developed a wide assortment of frequencies that are used to transmit data. It is often desired to produce circuits that can function over a variety of frequency ranges to facilitate a reduction in costs. This is because only one component needs to be designed which then can be placed into any system regardless of its frequency of operation.

Consider the quadrature phase shift keying demodulator (QPSK) depicted in Figure 1.1. The typical mixers used in this system are the Gilbert cell multiplier. The Gilbert cell requires both a differential local oscillator (LO) and radio frequency (RF) inputs. In order to produce a differential input, a balun is required. Furthermore it would be convenient for the designer to be able to use the same component for the balun at both the RF to IF conversion and at the IF to baseband conversion.

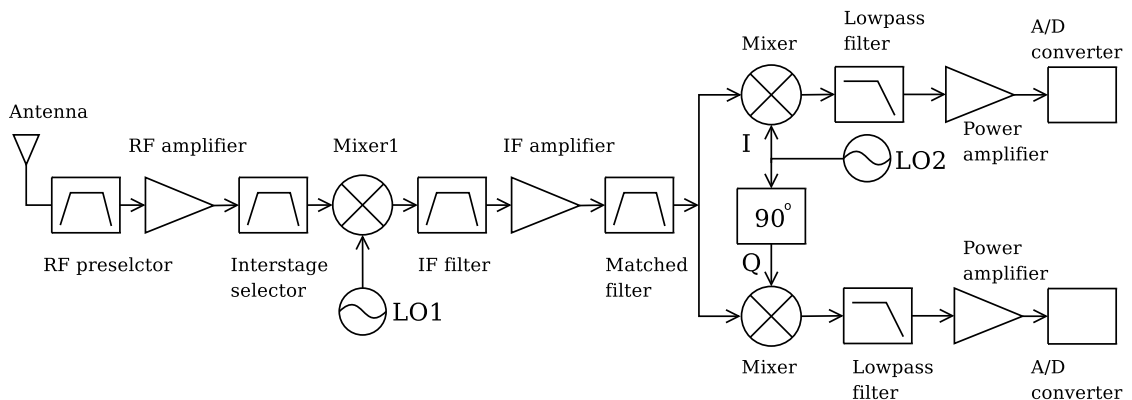


Figure 1.1: Block diagram of a basic QPSK demodulator[1]

Chapter 3 introduces a wideband balun that is able to function over a wide frequency range and can be used to convert the single ended inputs for both sets of

mixers. In particular, the use of a compensating capacitor allows this balun to function over a 7.5 GHz frequency bandwidth while minimizing the amplitude imbalance to ± 1 dB and the phase imbalance to 8° . This device also operates at a reasonably high input power of -5.8 dBm in addition to a low insertion loss of -16 dB. Because of the ability for the balun to function effectively at both at the L, S and C bands this device can for example facilitate its usage in both cellular communications (which operate at the C band) and all the WiFi protocols (which operate at both the S and C bands).

The system in Figure 1.1 also requires the use of a quadrature generator in order to demodulate the received signal. Chapter 4 introduces an inductorless quadrature voltage controlled oscillator for use in such a system. This quadrature oscillator does not contain the conventional inductor capacitor resonator tank but instead contains a synthetic resonator tank created using operation transconductance amplifiers (OTA) which allow a significant reduction in the size of the fabricated device. In addition the ability to easily tune the tail currents of the transistors allows this device to function over a large frequency range. In simulation, the bandwidth of operation was shown to be over 1.4 GHz. The phase noise of the device was determined to be -97.7 dBc/Hz which is comparable to other inductorless oscillators in literature.

If an oscillator is already available in a system, then the feedback quadrature generator introduced in Chapter 5 can be used instead to generate the quadrature phase shift. This new quadrature generator introduced here uses a feedback network to compensate for any amplitude imbalance. The measured results show that this device has over a 4 GHz bandwidth, significantly improving its performance over the conventional RC-CR network.

It is clear that in this classic example of a QPSK demodulator that if all of these components function over a large bandwidth then they can function regardless of what RF, IF or baseband frequency is used.

1.2 Thesis Organization

This thesis is organized as follows:

Chapter 2 is composed of the literature review which provides a broad coverage in a wide range of papers providing both an introduction and background material pertaining to phase generation in addition to demonstrating the need for the circuits described in this thesis. Finally the literature review introduces several comparable circuits found in literature for each of the designs featured, displaying both their strengths and weaknesses.

Chapter 3 introduces a common type of balun and describes its deficiencies. An equivalent model is then produced demonstrating the ability to insert a compensating capacitor in order to significantly improve its bandwidth. The models are then verified through a circuit simulator and finally through experimental results.

Following this, a quadrature inductorless oscillator will be introduced in Chapter 4. This circuit is crucial in any quadrature phase shift keying design. The simulated results produce a large tuning bandwidth in addition to the quadrature phase. The measured results closely match the simulated results, however because of stability issues, the circuit produces less bandwidth than is predicted in simulation.

Finally Chapter 5 is presented where a circuit that uses an existing Capacitor-Resistor Resistor-Capacitor network followed by a feedback loop that actively compensates for the amplitude imbalance. In this manner, the bandwidth of the circuit can be increased significantly. This completely new feedback circuit that uses a unique amplitude detector produces measured results that allow the compensating network to significantly improve the bandwidth of the original circuit.

Chapter 6 concludes with a summary of the results as well as highlights the benefits that are produced by the circuits presented in this thesis. Future work on this subject with regards to variations, extensions and enhancements in the designs are also presented.

Chapter 2

Literature Review

2.1 Introduction

Phase generation is important in many microwave designs and the need to provide an accurate phase and amplitude is crucial. This chapter provides background knowledge on this subject as well as discuss several existing designs found in recent literature for each of the circuits presented in this thesis. In addition material from the literature will be presented demonstrating the need for such circuits and showing the existing design's particular deficiencies and areas of improvements that can be made.

2.2 Balun Circuits

The general concept of a balun is to convert a balanced signal into an unbalanced one or vice versa. This is of particular importance in many transceiver designs. In general baluns are placed in two categories: active and passive. Active baluns are advantageous because they have lower loss and are significantly smaller to implement onto an monolithic microwave integrated circuit (MMIC) design. On the other hand, passive baluns do not consume any power, but are physically larger. In the trend to integrate all the components onto a single chip in order to minimize cost, the industry

is moving away from the microstrip hybrid discrete component circuits. Today passive baluns can only be economically viable in millimeter-wave integrated circuits where the wavelength is sufficiently small.

2.2.1 Passive Baluns

The simplest balun is shown in Figure 2.1a), consists of a transformer which is excited at one side and the output is taken differentially. Another type is the lumped lattice passive balun is shown in Figure 2.1b) [2]. This device performs its function by shifting the input by both $+90^\circ$ and -90° producing the balanced signal at the output. Because of the reactive components, the inherent frequency bandwidth is limited. Similar devices can be constructed on microstrip PCBs by substituting the lumped element with its equivalent microstrip/co-planar waveguide (CPW) components in order to improve its power handling [3].

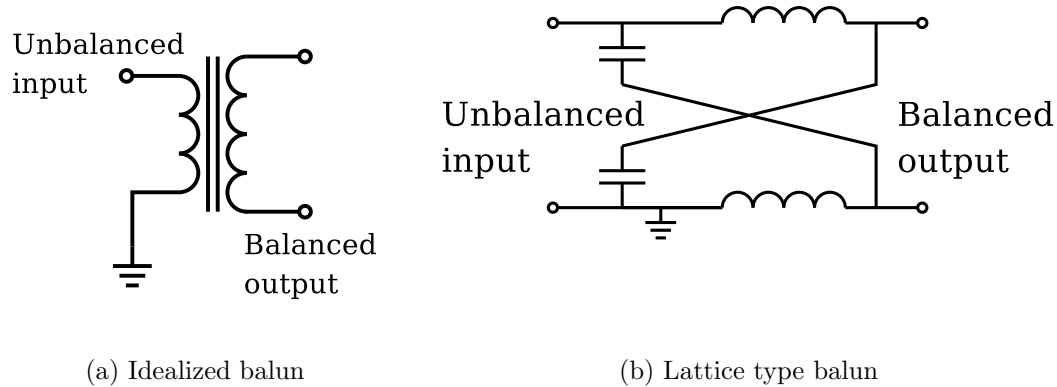


Figure 2.1: Various Passive balun designs a) Transformer balun design with one terminal grounded on output to create an unbalanced signal b) LC lumped element network used to create $\pm 90^\circ$ phase shifts

Yet another type of passive balun is the Marchand balun which is based on the idealized balun and is shown in Figure 2.2 [4][5]. It is one of the most popular planar baluns because of its ease of implementation and simple concept. The basic circuit consists of two couplers: The input is excited through port 1, and the differential

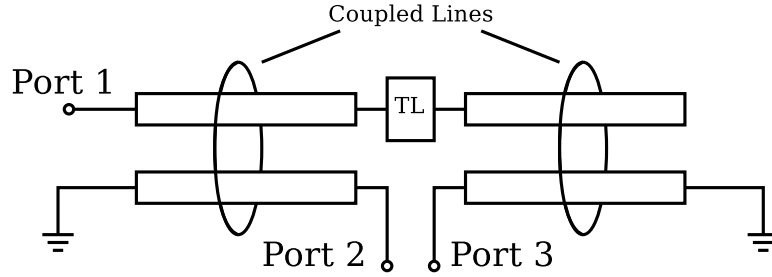


Figure 2.2: Marchand microstrip balun

outputs are taken out of ports 2 and 3. The directional couplers used in this design prove to be very restrictive in terms of the bandwidth and such designs have been reported to yield bandwidths of over 12% at 3 GHz [7].

Part of the problem with achieving a wideband balun is the requirement of producing the correct even and odd mode impedances. Even and odd mode impedances occur in a coupled line where there are three conductors, as is in any coupler design (in this case there are two conductors and a ground plane). If there exists a current flow in the same direction and magnitude through the two conductors, then there will be an electric field from the conductors to the ground as seen in Figure 2.3a). However if there is current flow in opposite directions then there exists not only electric fields to ground, but also between the conductors as seen in Figure 2.3b). Thus there can be an equivalent impedance between the ground and the conductors (including the fringing fields) that can be found in even mode excitation and also an equivalent impedance between both the conductors to the ground in addition to the impedance between each line forming the odd mode impedance [8].

In many coupler designs, there is a mismatch between the two impedances producing a slightly higher phase velocity in the odd mode [7]. This mismatch significantly reduces the available phase and amplitude balance, thus diminishing the bandwidth. In order to reduce the mismatch, research suggests the implementation of thicker substrates or introduce wider conductors to increase the even mode impedance [9].

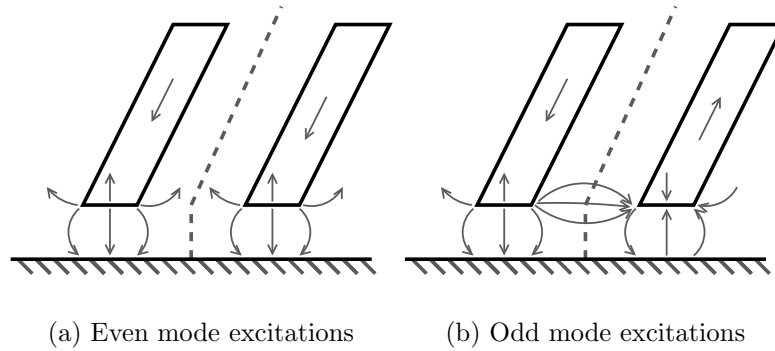


Figure 2.3: Electric field lines for even and odd mode excitations on a coupled line [8]

In addition, slow-wave coupling structures can be used or dielectric overlays on the couplers [10]. Other types of couplers such as the Lange and spiral are more successful at producing a more matched phase velocity and have been shown to produce up to 30% of its bandwidth [11][12]. These baluns produce excellent amplitude and phase balance characteristics, however they are difficult to implement onto MMIC substrates because of their large size as they typically range from 1 to 2 mm².

There are several ways in which to implement the various microstrip and lumped element baluns mentioned above. The method of using printed circuit boards (PCB) in conventional microstrip designs are orders of magnitude larger than any MMIC designs. Thus most literature focuses on implementing passive baluns on MMIC substrates. Their structures are still very large in comparison to active devices. Typical microwave integrated circuit designs are favored to be implemented on classical “analog” technology (i.e. SiGe, GaAs, InP etc.). However for solid system on chip (SoC) integration, low resistivity silicon is preferred due to its ability to integrate with digital circuits. The pitfall of using low resistivity silicon results in much lower performance especially with regards to any passive structure (microstrip, CPW, spiral inductors etc.). This is due to the lossy substrates that produce a low resistive path to ground. Other substrates are able to bypass this problem with the use of either

higher resistivity substrates or isolation techniques such as silicon on insulator (SOI).

Some literature has even suggested the removal of part of the substrate in order to improve the performance, albeit at an increased cost [13][14]. The circuits presented in this thesis will deal exclusively with low resistivity silicon in order to minimize costs. As a result inductors, microstrip and CPW type components are avoided and will rely mostly on lumped elements such as capacitors, resistors and active devices.

2.2.2 Active Baluns

Several types of active balun configurations are found in the literature. For the most part, the designs consist of a combination of a common source and another amplifier such as the source follower or common gate. Figure 2.4a) depicts the generalized active balun schematic and b) describes the schematic of an active balun found in [15]. By leveraging the 180° phase shift produced by the common source and providing some type of gain/loss match with another amplifier, a balanced signal from the outputs of the two amplifiers can be achieved.

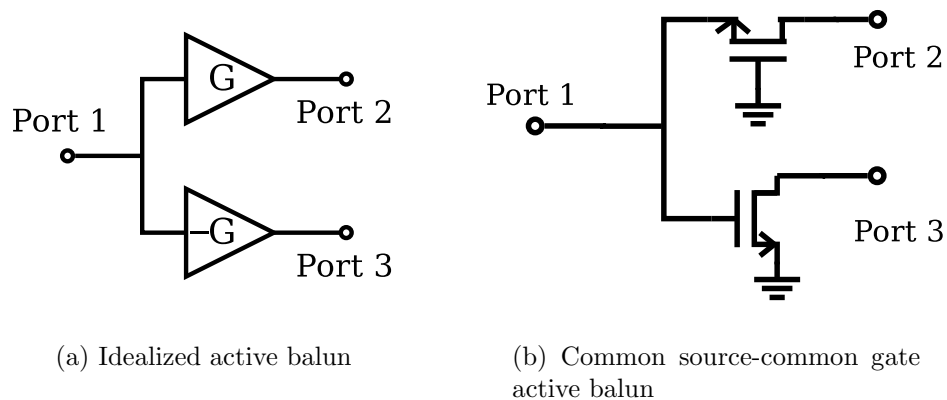


Figure 2.4: Schematic of various active baluns

The balun encounters difficulties in producing a broadband amplitude and phase balance because inherent in the design is the use of two amplifiers that will never produce a constant phase and amplitude without tuning. In addition the devices's

phase and amplitude decrease at the different rates in both amplifiers with respect to frequency. As a result, either iterations of the design or an active tuning element is required to equalize the gains of both amplifiers in order to produce the proper amplitude and phase balance. As predicted literature shows that these amplifiers produce sub-par bandwidths. Several baluns are able to produce larger bandwidths using various compensating techniques or more exotic substrates. On average in literature, the sizes are never larger than 0.75 mm^2 [15][16][17][18]. However this figure includes all of the bonding pads and the bypass capacitors and if these items are excluded (as they are often unnecessary when integrated within a circuit) then the device shrinks even further.

2.3 Quadrature Generation

Quadrature generation is the process of generating two orthogonal sinusoidal signals (i.e. out of phase by 90°). This is important in many systems and in this section two examples of the need for a quadrature generator are presented both in the transmitting side and from the receiving side of a transceiver of a communication system. In addition, examples of the implementations of quadrature generators are presented.

Quadrature Phase Shift Keying Modulator

A typical quadrature phase shift keying (QPSK) modulator system is depicted in Figure 2.5. The basic principle of this modulation scheme is to modulate the carrier with four different phases. This is accomplished with the use of a 90° phase shifter in combination with a local oscillator. The two signals (I and Q) are then mixed with two specially formatted digital streams d_1 and d_2 . The specially formatted data streams uses $+\sqrt{\varepsilon_s/2}$ and $-\sqrt{\varepsilon_s/2}$ instead of the typical digital 1's and 0's. Where ε_s is the energy spent per symbol. The result of the mixing with the digital signal is that two phases (0° and 180° for I and 90° and 270° for Q) will be produced at the

output of each mixer. These signals are then put through an analog adder and then upconverted using the conventional heterodyne architecture (the details of this and other elements within the QPSK have been omitted for clarity).

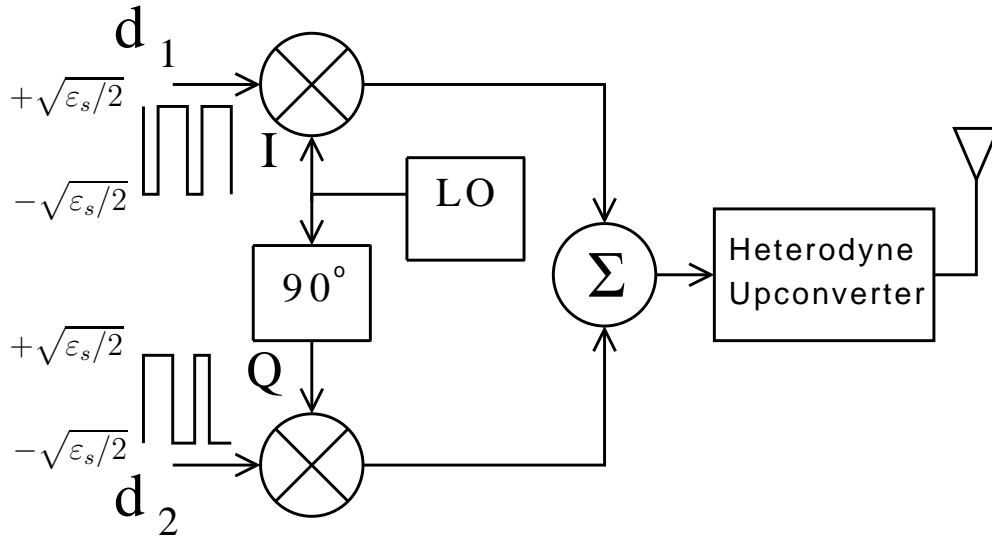


Figure 2.5: Block diagram of a QPSK modulator

The analog adder performs a vector addition and produces the final four phases that can be seen in the constellation diagram shown in Figure 2.6a). The final output consisting of any one of the four phases that are sent are a linear combination of the vector addition and have phases: 45° , 135° , 225° and 315° . The constellation diagram depicts the binary representation of each symbol along with its associated phase. The real and imaginary axes provides a convenient boundary for the detection regions.

As the signal is transmitted through space and demodulated, the signal is subjected to many types of interference. The demodulator will compare the received signal to the same constellation and attempt to determine the original signal. In the presence of ideal additive white gaussian noise (AWGN), the probability of error P_s ,

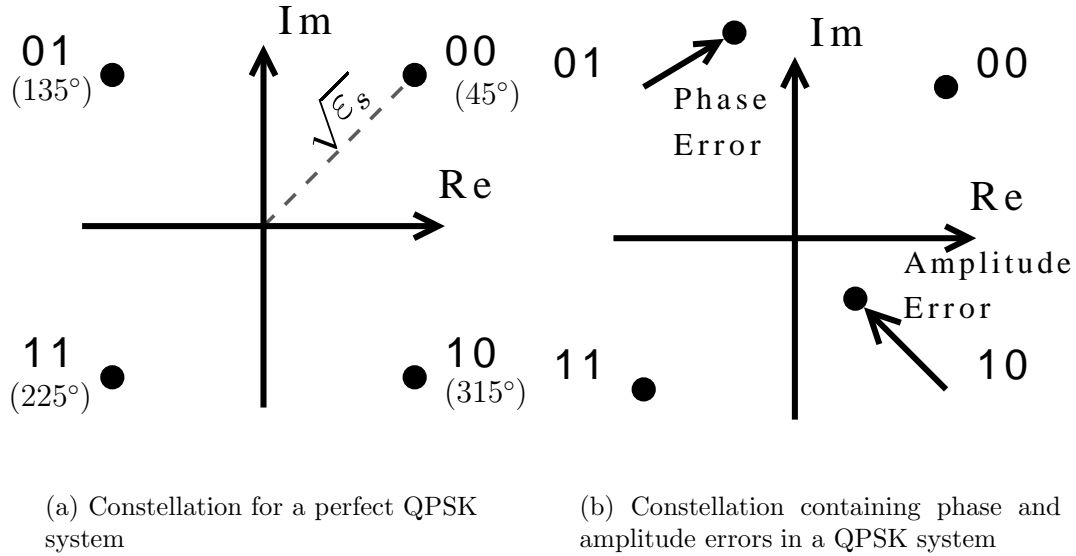


Figure 2.6: Constellation diagram for a QPSK system

can be found to be Equation 2.1 [19].

$$P_s = 2Q\left(\sqrt{\frac{\varepsilon_s}{N_o}}\right) - Q^2\left(\sqrt{\frac{\varepsilon_s}{N_o}}\right) \quad (2.1)$$

$N_o/2$ is the noise spectral density, ε_s is the energy per symbol and $Q(\dots)$ is the Gaussian probability function. The larger the distance between each constellation point in Figure 2.6, the smaller the probability that there will be an error. That is, the larger the distance between the two points, the harder it will be for noise to “push” the signal into the next detection region. The rate of which errors occur is called the bit error rate (BER) and is directly affected by the energy spent per symbol ε_s . Increasing the power levels is not without consequences as this will increase the power consumption.

As mentioned previously, an oscillator followed by a quadrature generator is needed to generate the required signals. This can be accomplished either by using an oscillator followed by a 90° phase shifter or using a more complex quadrature oscillator that produces the required 90° phase internally. Regardless of which method is

employed, the issue is that there must be a precise phase and equal amplitude signal produced by the quadrature generator. If either the phase or magnitude is incorrect, then the resulting constellations will not be in their optimal positions. Consider Figure 2.6b) which depicts an example of both the occurrence of an improper amplitude and phase produced at the output. The probability of symbol detection P_s will be significantly reduced and correspondingly an increase in BER.

Quadrature Phase Shift Keying Demodulator

In all superheterodyne systems for the demodulator, whenever the RF signal is down-converted to the intermediate frequency (IF), if improper filtering is employed, an image signal from another channel will also be produced at the IF. To counter this effect, a pre-selector filter is employed to filter out the other channels. The use of a pre-selector filter is often fixed (to reduce costs) and as a result, a high IF is typically used in order that its image does not fall into the band. In systems in which this is not possible to have a high IF, an active filter is then used to track with the LO in order to suppress the image.

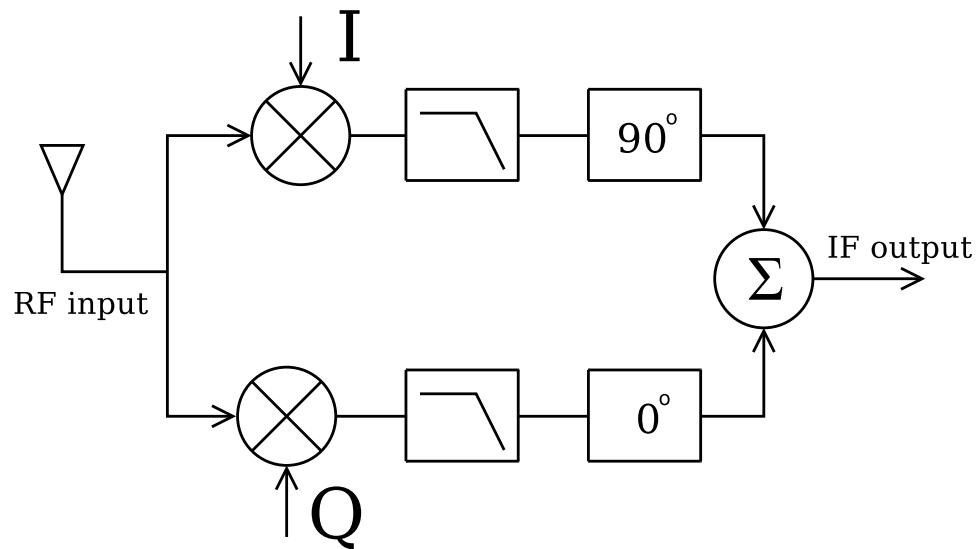


Figure 2.7: Block diagram of an image reject QPSK demodulator[5]

The difficulty with higher IF mixers and filters is that they are more difficult to design and implement. As mentioned previously, a fixed passive pre-selector filter is often used. If this is supplemented with an active pre-selector filter in combination with a low IF instead, this will allow the system to tune over a large bandwidth. However it is often difficult to build an active filter with sufficient cutoff or dynamic range for this purpose [20].

The image reject receiver is one such system that is able to produce an image free output. This allows the designer to forgo any pre-selector filter or be concerned about downconverting higher IF components. The basic image reject receiver employs the use of a quadrature generator. Figure 2.7 depicts the block diagram of this system. The reliance of the system to reject the image is heavily dependent on the quadrature generator producing the proper amplitude and phase.

$$IRR \simeq \frac{4}{(\Delta\phi)^2 + \varepsilon^2} \quad (2.2)$$

The image rejection ratio (IRR) seen in Equation 2.2 determines the effects of improper amplitude and phase [5]. The ε and $\Delta\phi$ terms are the amplitude and phase error respectively.

2.3.1 Quadrature Generator Circuits

RC-CR Networks

From the above two examples, it is clear that there is a need for accurate quadrature phase generators. One such example of a quadrature generator is the RC-CR network found in Figure 2.8. A detailed analysis is found in Section 5.2.2, however it is sufficient to say that the circuit suffers from a very narrow bandwidth and is highly sensitive to the values of resistor and capacitor used.

The single frequency of operation can be found to be Equation 2.3. In the CMOS

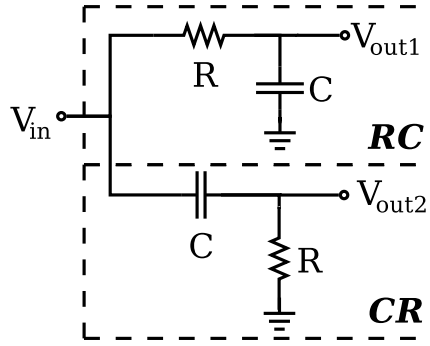


Figure 2.8: Schematic of RC-CR network

process the fabricated components can frequently be inaccurate and the nature of the highly sensitive component values in this circuit presents a significant problem.

$$\omega = \frac{1}{RC} \quad (2.3)$$

Polyphase Networks

The RC-CR network mentioned is one such example of quadrature generators, other examples of quadrature generators also suffer from insufficient bandwidth due to their ability to keep a proper phase and constant amplitude. The employment of a more complex offshoot is a polyphase network shown in Figure 2.9a). The polyphase filter has the ability to take a distorted quadrature signal and improve its phase properties. This is accomplished by placing a differential signal at I_{in+} and I_{in-} and grounding Q_{in+} and Q_{in-} . The output of this circuit will now produce all four phases (0° , 90° , 180° and 270°) [5][21][22].

In order to clarify the network, the schematic has been rearranged to form Figure 2.9b). It is clear now that the polyphase filter is essentially the RC-CR circuit placed in a loop. As a result, it exhibits the same issues with low bandwidth. However, it is possible to cascade multiple stages of this circuit with staggered resistor and capacitor values to increase the bandwidth. If a two stage polyphase filter is

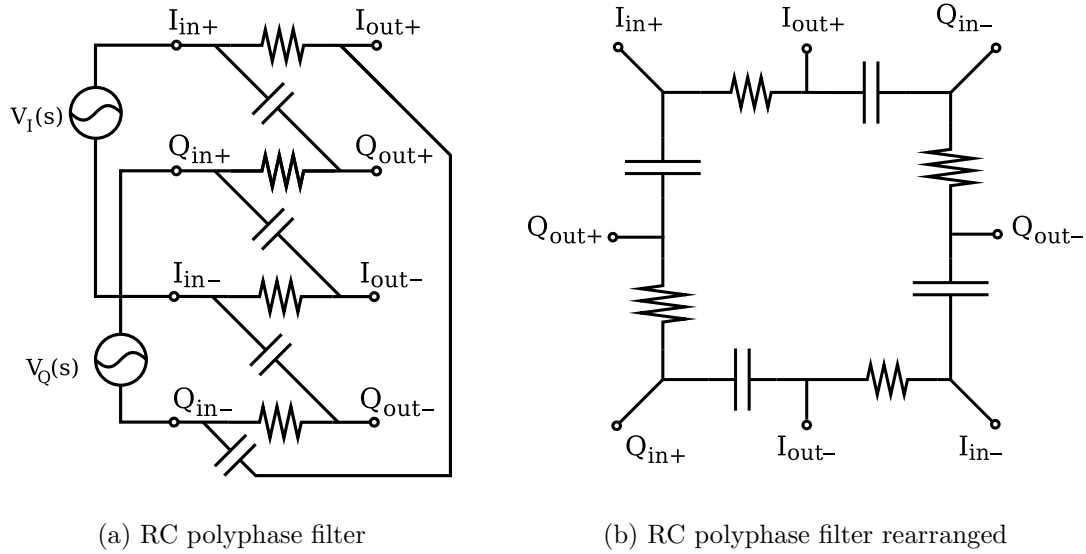


Figure 2.9: Schematic of a single stage polyphase filter [5][20]

employed, then the transfer function is found to be Equation 2.4. From a dual stage circuit, a $\pm 20\%$ bandwidth from the center frequency can be obtained (assuming a corresponding 0.2 dB gain imbalance) [5]. Because of the inherent larger bandwidth, the polyphase circuits are much less susceptible to inaccurately fabricated components.

$$\frac{V_Q(s)}{V_I(s)} = \frac{Q_{out+} - Q_{out-}}{I_{out+} - I_{out-}} = \frac{s(R_1C_1 + R_2C_2)}{1 - s^2(R_1R_2C_1C_2)} \quad (2.4)$$

The issue with these types of RC networks is that there is significant attenuation along with noise introduced into the system through the resistor. In addition, the polyphase filter networks suffers from additional losses and noise when cascading additional stages.

2.3.2 Branch Line Coupler

One example of a quadrature generator using microstrip lines is the branch line coupler depicted in Figure 2.10 [8]. The device consists of $\lambda/4$ length lines that have a $Z_o/\sqrt{2}$ characteristic impedance. The resulting output ports (Ports 2 and 3) produce

a quadrature phase. Similar to the lumped element quadrature generators, this device also suffers from a narrow amplitude and phase balance limiting the device to about 26% of its bandwidth.

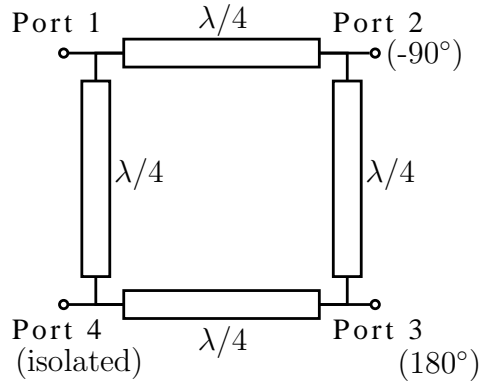


Figure 2.10: A microstrip branch line coupler

2.4 Oscillator Circuits

In this section a few oscillators of both the single and quadrature phase variety will be presented in order to provide background knowledge for the inductorless quadrature voltage controlled oscillator introduced in Chapter 4. Examples of inductor and inductorless oscillators will be presented and their strengths and weaknesses contrasted.

2.4.1 Colpitts Oscillator

One frequently cited and used oscillator is the Colpitts [8][23][24]. The device consists of an LC tank coupled with an amplifier that restores the stray energy lost through the tank. In this example shown in Figure 2.11a) the amplifier used is a common drain configuration, however other types of amplifiers can easily be substituted.

The transfer function for the LC tank can be found in Equation 2.5. The R_p term denotes the equivalent series parasitic resistance associated with both the inductor's wire resistance and losses to the substrate. It is noted that the added parasitic

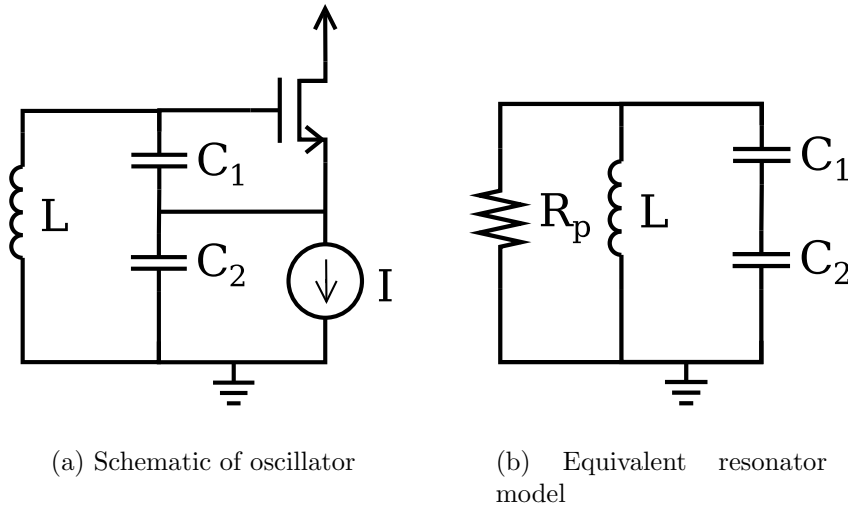


Figure 2.11: Schematic of common source Colpitts oscillator

resistance and capacitance from the transistor has been neglected here for simplicity.

$$T(s) = \frac{Ls + R_p}{s^2 + \frac{R_p}{L} + \frac{1}{LC}} \quad (2.5)$$

$$\omega_o = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}} \quad (2.6)$$

$$Q = \frac{\sqrt{L/C}}{R_p} \quad (2.7)$$

The equation for the LC tank's resonating frequency is found in 2.6. It is clear that an adjustment of the capacitor or inductor values can easily change the resulting frequency of oscillation. In many cases, a varactor is supplemented in place of the capacitor to allow for the changing of ω_o . The quality (Q) factor is shown in Equation 2.7.

If a high Q inductor (which in turn produces a high Q resonator) is used, then the resulting phase noise can be very low. The Q derived here is heavily dependent on R_p . It then follows that by reducing the series resistance, Q will increase.

While there are ways to reduce both the parasitic capacitance and resistances

such as using thick metal layers, the end result for silicon is that their inductors are still less competitive in comparison to off chip resonators. Regardless, many inductor type oscillators are still implemented on chip because of the cost efficiency, however their inductors typically consume large areas and are not well suited for minimalistic designs.

2.4.2 Voltage Controlled Oscillators

Varactor Tuning

The Colpitts is just one example of an oscillator, other configurations such as the Pierce and Hartly apply similar principles of an LC tank followed by a transistor used to recover any resistive losses. Because most oscillators are based on the LC tank, the frequency is directly dependent on the capacitor and inductor values, any variation in the manufacturing process will alter the oscillating frequency. One such way to mitigate these consequences is to use a varactor to tune the oscillator back to the desired frequency [25][26]. The added benefit is that the use of a varactor allows the oscillator to become tunable. The basic differential inversion mode varactor consists of two transistors with their gates tied together to form the tuning port and the source and drain regions tied together at each end to form the differential ports. The gate voltage changes the amount of electrons that are formed under the gate. This in turn changes the capacitance seen from the gate to the source and drain. The schematic for this varactor shown in Figure 2.12a).

The device was laid out in Cadence and simulated in SpectreRF and the results are depicted in Figure 2.12b). It is clear that three things are inherently undesirable from the results. First, there exists a large amount of resistance that scales lineally with the device size. This is directly proportional to the quality factor, which will in turn will increase the phase noise of the oscillator. Secondly is that the resistance changes as a function of applied voltage. This is a particular issue as it will change

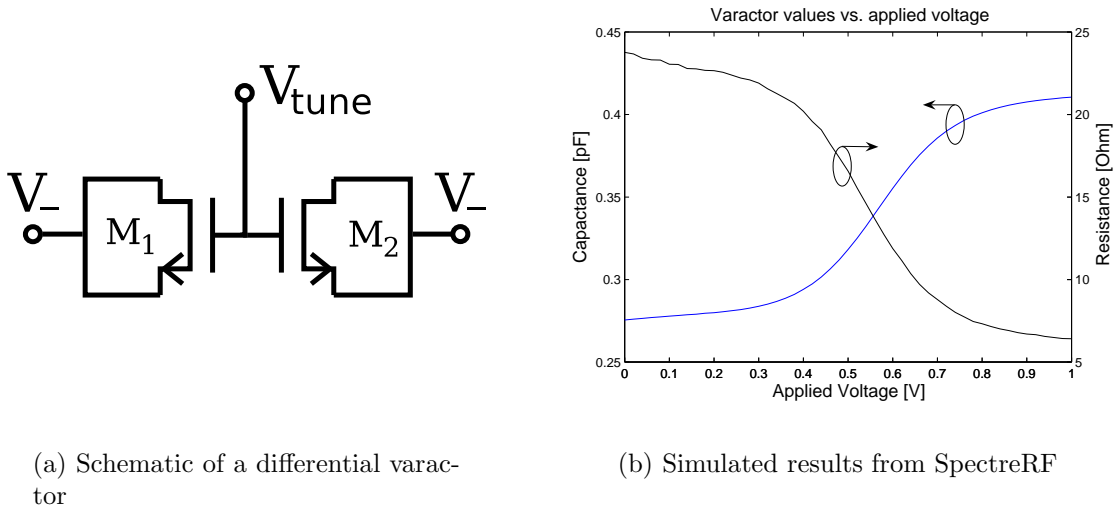


Figure 2.12: Schematic and simulated results from a 24 fingers \times $2.5 \mu\text{m} \div 60 \mu\text{m}$ wide inversion mode CMOS varactor at 2 GHz

the conditions of the oscillator whenever the varactor is tuned. Even if the oscillation conditions remain the same, the changes in resistance will change the phase noise and will make the device very difficult to characterize. Lastly, the device suffers from a very small tuning range. The device simulated here is particularly large but can only tune less than 0.15 pF. A similar approach is the use of varactor diodes instead of varactors based on MOS transistors however their quality generally produces worse performance [27].

To accommodate for the small tuning range, some investigators have used a switched network in which a number of inductors along with the varactors are used. In [28], they use four separate inductors to coarsely tune the frequency followed by the use of varactors to finely tune the frequency in between. In this way, they can have a bandwidth of over 26% at 1.6 GHz.

A more exotic (and costly) approach would be the use of Micro-Electro-Mechanical Systems (MEMS) technology to accurately move two plates closer together in a parallel plate capacitor in order to tune the voltage. Recent trends have started to incorporate MEMS technology onto existing silicon processes allowing both to coexist,

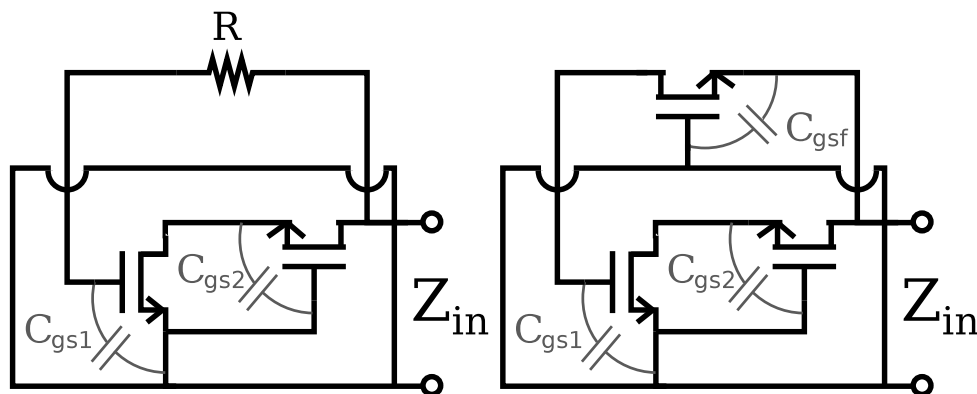
however the slightly larger tuning range does not justify the extra costs [29].

Active Synthetic Inductors

Regardless of which approach is used to vary the capacitance, the use of variable capacitors provide very little tuning range. One approach to this problem is the use of active synthesized inductors [30][31][32]. The ability to synthesize inductors through the use of transistors allows the VCO to operate over a much larger tuning range. The general idea of an active inductor is the use of a negative feedback network to generate the required transfer function of an equivalent inductor. Some examples of active inductors are found in Figure 2.13. The corresponding equations for the device's input impedance are found in Equations 2.8 and 2.9. Where g_m is the transconductance of the transistors.

$$Z_{in} = \frac{1}{g_m} + j \frac{C_{gs} R}{g_m} \quad (2.8)$$

$$Z_{in} = j \frac{C_{gs}}{g_m g_{mf}} \quad (2.9)$$



(a) Resistor feedback implementation

(b) Common gate feedback implementation

Figure 2.13: Some examples of active inductors

However the tradeoff to such inductors are the phase noise degradation as a result of the use of transistors. Depending on the circuit and the system, the higher phase noise may be an acceptable compromise to the smaller silicon area required for an active inductor versus a passive one.

2.4.3 Quadrature Oscillators

Instead of using an oscillator coupled with a quadrature generator, another option is the use of a quadrature oscillator. Two of the most popular ways in which to make a quadrature oscillator are the use of a dual integrator oscillator or a cross coupled oscillator [33][34].

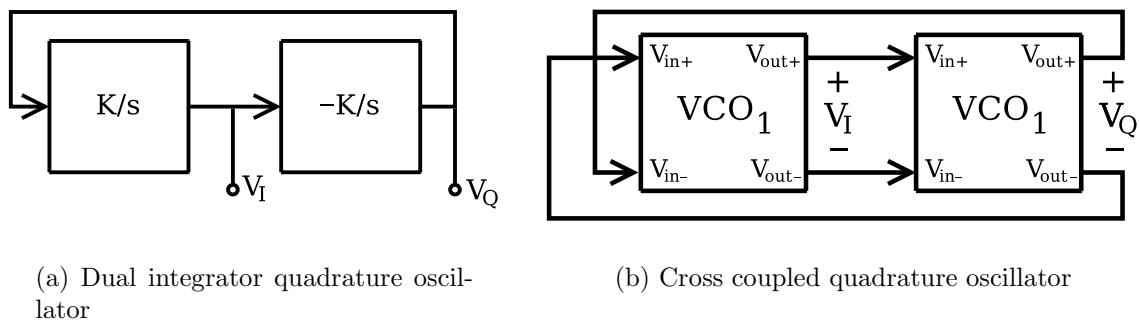


Figure 2.14: Various types of quadrature oscillators

Dual integrator quadrature oscillator

The dual integrator oscillator is shown in Figure 2.14a) [35]. The integrator essentially performs a 90° phase shift allowing an in-phase and quadrature output to be produced. Because this device depends on an active filter based integrator, there are unmodeled parasitics that tend to produce an unstable circuit producing an unreliable oscillation frequency [5].

Cross coupled quadrature oscillator

A dual cross coupler consists of two separate oscillators that are cross coupled to each other and is depicted in Figure 2.14b). In this way, each oscillator is synchronized from each other at an exact 90° phase [36][37][38]. The issue with these types of oscillators is that there are two VCOs. Both the effective area and power consumption of this circuit will be doubled just to produce the quadrature phase. The trade-off of higher noise and very tight bandwidth (thus tuning) considerations may be considered acceptable.

It is clear that neither configuration offers superior performance to their single phase counterparts. As a result many times a circuit will contain a high quality compact single phase oscillator in conjunction with a quadrature generator.

2.5 Conclusions

This chapter has provided examples from recent literature on various circuits relating to phase generation. Examples of existing balun circuits both of the active and passive varieties were presented. Passive baluns were shown to consume large areas while active baluns consumed more power and had a generally smaller bandwidth. Background knowledge was given to stress the need for accurate phase generators for modulators and demodulators such as a QPSK modulator and the image rejection QPSK demodulator. Examples of both the single phase Colpitts, dual integrator loop and cross coupled quadrature oscillators were presented. Implementations of various quadrature generators such as the RC-CR, polyphase and branch line coupler were also presented demonstrating their limited bandwidth. Lastly an implementation of active synthetic inductors for use in oscillators was discussed and the resulting low Q versus lower area consumption was discussed.

Chapter 3

Capacitor Compensated Balun

3.1 Introduction

A device that produces a balanced signal from an unbalanced one is called a balun. As discussed previously in Section 2.2, baluns play a crucial role in many microwave and RF circuits. Several designs were discussed and one of the chief requirements was to keep the amplitude and phase balance as close to ideal as possible. While the baluns discussed previously were able to satisfy those criteria, their bandwidths are typically very narrow. In addition to this, passive structures are typically too large to create in MMIC implementations. This is seen in the Marchand balun found in Figure 2.2 which requires sections of $\lambda/4$ transmission lines. This translates to 7.25 mm at 3 GHz, far too large for a silicon MMIC. A transformer type balun can be implemented in MMIC designs, however its operation is typically quite limited [39][40]. Their loss due to low Q inductors as well as the large area required makes them an unattractive option. Thus for most MMIC designs in the DC to 30 GHz range, active baluns are a very good solution. In this section we discuss a single transistor balun and its limited bandwidth caused by parasitics. The design is then improved upon by inserting a compensating capacitor to significantly increasing its operational bandwidth.

3.2 Single Transistor Balun

A common type of balun is a single transistor balun shown in Figure 3.1. The input signal is applied to the gate and the output is taken from both the drain (v_{o1}) and the source (v_{o2}). The circuit can be viewed as a typical common source amplifier if the output at the source is ignored and as a common drain amplifier if the source output is ignored. The transfer function for a common source amplifier has a 180° phase offset relative to the input, while the transfer function of a common drain is 0° phase offset relative to the input. The resulting two output signals are correspondingly 180° from each other, thus producing a balanced signal from an unbalanced one.

The generalized equations for the two outputs (not including parasitics) are found in Equations 3.1 and 3.2. These equations assume that C_1 , C_2 , C_3 and R_1 are sufficiently large and can be ignored because they are used for DC blocking or as an RF bias choke, thus leaving the RF signal unaffected.

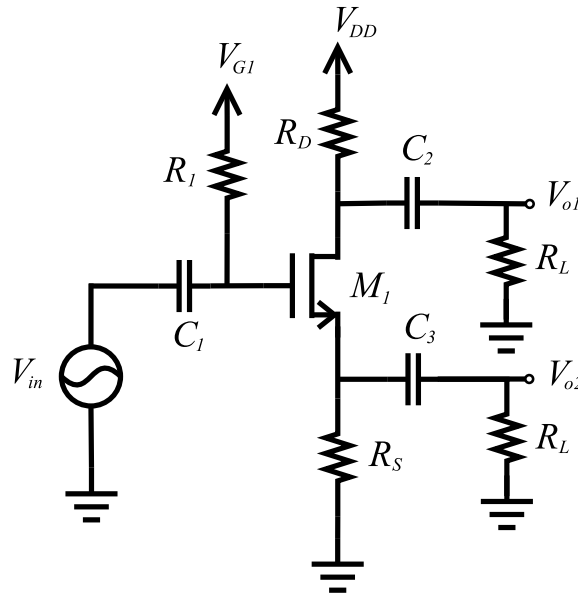


Figure 3.1: Single Transistor Balun Schematic

$$\frac{v_{o1}}{v_{in}} = \frac{-g_m R'_D}{1 + g_m R'_S} \quad (3.1)$$

$$\frac{v_{o2}}{v_{in}} = \frac{g_m R'_S}{1 + g_m R'_S} \quad (3.2)$$

The parasitics in the MOSFET model are ignored here for the time being in order to simplify analysis and determine the circuit's performance in an ideal setting. For this circuit in order to simplify the equations, a substitution was made: $R'_S = R_S \parallel R_L$ and $R'_D = R_D \parallel R_L$.

In order to make this circuit symmetrical and produce a zero amplitude difference between the two outputs, R_S is set equal to R_D . This results in $R'_S = R'_D$, and Equations 3.1 and 3.2 reduces to $\frac{v_{o1}}{v_{in}} = \frac{-v_{o2}}{v_{in}}$. From this, it is clear that since Equations 3.1 and 3.2 have no frequency component, the device will have perfect amplitude balance and perfect phase balance (as $\frac{v_{o1}}{v_{in}} = \frac{-v_{o2}}{v_{in}}$) across the whole bandwidth. However, due to capacitances from the gate to the source (C_{gs}) and from the gate to the drain (C_{gd}) that were not included in this equation the bandwidth of this circuit is reduced dramatically. As these capacitances become substantial at higher frequencies and the resulting phase will increase past 180° . These effects are explored more indepth in the following section.

3.2.1 Transistor Modeling

In order to gather a more accurate picture of the circuit, a more precise transistor model is required. The classic model of a typical MOSFET is shown in Figure 3.2 a).

We begin by exploring the associated capacitances in this model. For this device, the manufacturer has chosen to use the common “self aligned” process. In this method, the polysilicon material at the gate is deposited first, followed by the doping of the source and drain regions. The process is called self aligned because the whole area between the source and drain (including the polysilicon gate) is doped and the polysilicon essentially “shields” the gate region underneath, thus preserving

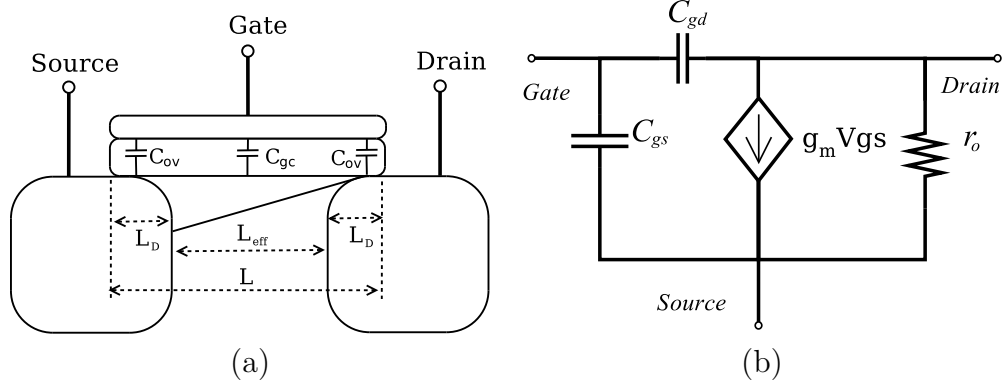


Figure 3.2: Simplified a) Physical MOSFET model and b) MOSFET schematic equivalent model displaying crucial parasitics

its doping type.

However even though the gate region is shielded, the source and drain region's dopants still diffuse laterally into it. This lateral diffusion creates an overlap between the source and drain to the gate. As a result a small capacitance is produced from this overlap and is shown in Figure 3.2b) as C_{ov} . The overlap capacitance is consequently a function of the overlap area L_D , width of transistor W , thickness of the oxide t_{ox} , and the permittivity of the oxide ϵ_{ox} . Their relationships in determining the capacitances are equated in Equation 3.3 [23][24].

$$C_{ov} = \frac{\epsilon_{ox}}{t_{ox}} W L_D \quad (3.3)$$

$$C_{gc} = \frac{\epsilon_{ox}}{t_{ox}} W L_{eff} \quad (3.4)$$

$$C_{gs} = \frac{2}{3} C_{gc} + C_{ov} \quad (3.5)$$

$$C_{gd} = C_{ov} \quad (3.6)$$

$$r_o = \frac{|V_A|}{I_D} \quad (3.7)$$

Figure 3.2 and Equations 3.5 and 3.6 are only valid for the saturation region as the shape of the channel dictates the associated capacitances. However because the circuits discussed here are all in the saturation region, this model is considered valid.

Note that r_o in Equation 3.7 from Figure 3.2 is omitted in many of the analyzes in this Chapter. This is because r_o is typically very large for typical biasing conditions for the balun circuit discussed in this Chapter. In addition these equations are rough approximations and ignore certain factors such as the effects of the substrate.

Apart from the overlap capacitance, there is also the capacitance between the gate and the conductive channel C_{gc} . Its function is expressed in Equation 3.4. L_{eff} is the effective gate length (what is left after the diffusion of the source and drain areas).

The total capacitance of the gate to source C_{gs} is then given in 3.5. This is a combination of both the gate and channel capacitance. As the channel does not form around the gate region to the drain, the only capacitance for the drain is the overlap capacitance caused by the laterally diffused drain as discussed previously. The resulting C_{gd} is seen in Equation 3.6.

3.2.2 Miller Capacitance

In order to provide a better model of this circuit, the previously ignored effects of C_{gs} and C_{ds} are now needed to be incorporated into the transfer function. However the capacitance from the drain to the gate makes this circuit difficult to analyze. Miller's theorem describes a way in which the capacitance across the input to the output of an amplifier can be separated[41]. Consider an example of the Miller capacitance found in Figure 3.3 where the capacitor C in a generic amplifier is separated into its approximate capacitances. The corresponding equations are expressed in Equation 3.9 and 3.10. For Equation 3.8, K describes the gain between the input and output.

$$K = \frac{v_2}{v_1} \quad (3.8)$$

$$C_1 = C(1 - K) \quad (3.9)$$

$$C_2 = C\left(1 - \frac{1}{K}\right) \quad (3.10)$$

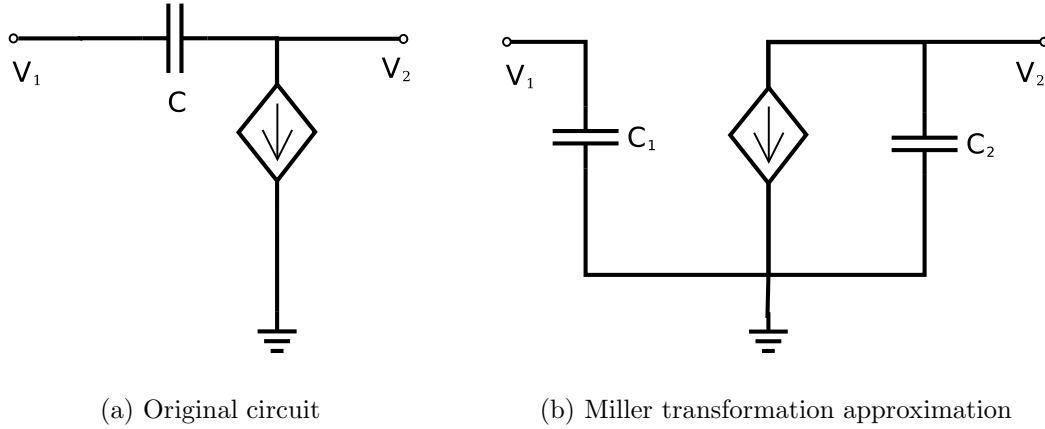


Figure 3.3: Example of a circuit where Miller's theorem is applied to separate the capacitance .

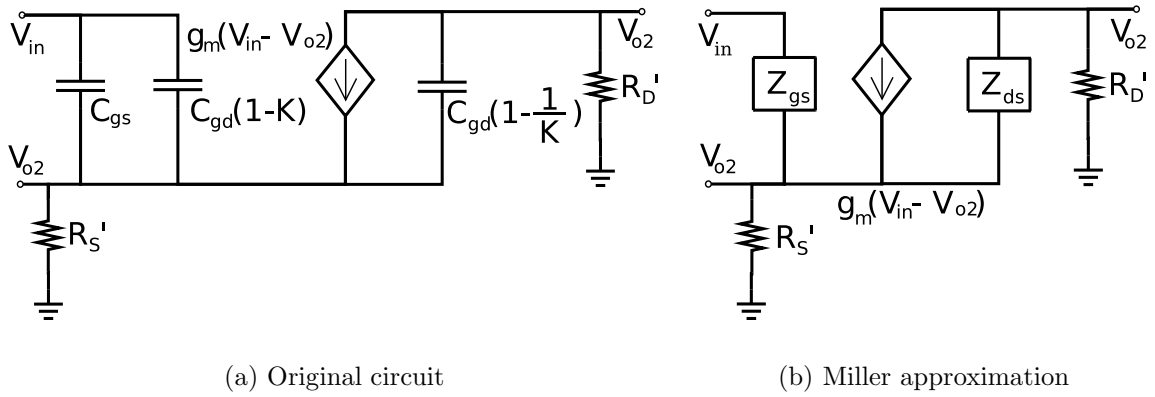


Figure 3.4: The original and approximate circuit model for the balun

Typically, the Miller theorem is used to describe the parasitic effects of C_{gd} . At higher frequencies, C_{gd} represents a major problem owing to the results of the Miller transformation showing us that the capacitance across the gate and source is now C_{gd} multiplied by a factor of $\sim K$ (if K is negative and sufficiently large as in the case of a common source configuration). The larger the total gate to source capacitance is, (in general this is the gate to source capacitance plus the resulting capacitance from the Miller transformation) the more current is shunted to ground at high frequencies, thus reducing the effective input voltage. This then in turn reduces the resulting output

voltage. Because of this extra capacitance producing a shunting effect through the Miller transformation, C_1 from Figure 3.3b) is often called the Miller capacitance. The Miller transformation is only valid for determining forward gain and input impedance. As this transformation will only be used to calculate the forward gain for the balun, this approximation is considered valid.

While the Miller capacitance is significant if the gain is large, this is not the case in the balun circuit discussed in this chapter. This is due to the dual output configuration of this balun. The gain is less than unity and the Miller capacitance effect on the gain in this circuit are minimal.

Although the Miller effect is not pronounced in this circuit and as a result does not produce significant shunting effect at high frequencies, the reason why it is introduced here is because the effects of C_{gs} and C_{gd} are more serious when looking at the phase difference between the two outputs. If Miller's theorem is applied to the balun circuit depicted in Figure 3.1, the circuit is then transformed into Figure 3.4a). In this case, K is the gain from v_{o2} to v_{in} . This was derived earlier in Equation 3.2.

$$Z_{gs} = \frac{-j}{\omega(C_{gs} + C_{gd}(1 - K))} \quad (3.11)$$

$$Z_{ds} = \frac{-j}{\omega(C_{gd}(1 - \frac{1}{K}))} \quad (3.12)$$

The circuit is then further simplified using the substitution expressed in Equation 3.11 and 3.12 by combining the capacitances and resistances that are in parallel in order to aid in the analysis, the resulting circuit is shown in Figure 3.4b).

Performing circuit analysis on Figure 3.4b), the initial expression is found to be Equations 3.13 and 3.14.

$$\frac{v_{o1}}{R'_D} = \frac{v_{o1} - v_{o2}}{Z_{ds}} + g_m(v_{in} - v_{o2}) \quad (3.13)$$

$$\frac{v_{o2}}{R'_S} = \frac{v_{in} - v_{o2}}{Z_{gs}} + g_m(v_{in} - v_{o2}) + \frac{v_{o1} - v_{o2}}{Z_{ds}} \quad (3.14)$$

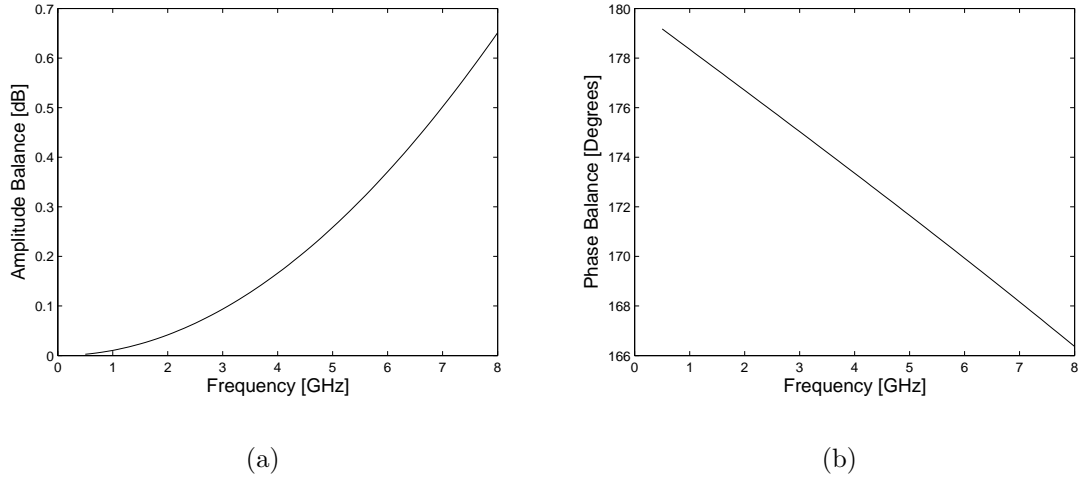


Figure 3.5: Transfer function of the a) Amplitude balance and b) Phase balance

Rearranging these two equations to form the gain of both outputs we arrive at Equations 3.15 and 3.16. Those equations are then plotted in Matlab and the results are depicted in Figure 3.5.

$$\frac{v_{o2}}{v_{in}} = \frac{Z_{ds}^2 + R'_D Z_{ds} + g_m Z_{gs} Z_{ds}^2 + g_m R'_D Z_{gs} Z_{ds} - g_m R'_D Z_{gs} Z_{ds}}{R'_S Z_{ds} Z_{gs} + R'_S Z_{ds}^2 + R'_D R'_S Z_{ds} + g_m R'_S Z_{gs} Z_{ds}^2 + Z_{gs} Z_{ds}^2 + R'_D Z_{gs} Z_{ds}} \quad (3.15)$$

$$\frac{v_{o1}}{v_{in}} = \frac{v_{o2} R'_D - g_m R'_D Z_{ds} + g_m R'_D Z_{ds} v_{o2}}{Z_{ds} + R'_D} \quad (3.16)$$

The amplitude balance is defined here as the ratio of the two output powers in decibels. The phase balance is defined as the difference in phase between the two signals in degrees. Ideally the phase balance should be at 180° and the amplitude balance should be at 0 dB. Equations 3.1 and 3.2 shows that the phase balance is frequency dependent and exhibits an excessive amount of roll-off at high frequencies. It is obvious that the previously ignored drain and source capacitance in those equations are quite substantial when incorporated into the transfer function. Further comparisons with circuit level simulations will be provided and discussed in the next section.

3.3 Circuit Description

3.3.1 Compensating Capacitor

From the previous section it is clear that the current one transistor balun is unusable. For this reason in order to increase the bandwidth something must be done to force the phase back to 180° . A cascode configuration was explored, and although it reduces the effect of the Miller capacitance, it does not eliminate the effects of C_{gs} . A reactive element placed somewhere in the circuit is sought that will move the phase back on track at higher frequencies, but also proportionally compensate less at lower frequencies.

In order to produce such a schematic, consider the circuit in Figure 3.6a): if a capacitor C_c is placed in parallel with a resistor R , then the transfer function is shown to be Equation 3.17. The phase of this function is then derived to be Equation 3.18. The resulting plot of the transfer function with and without C_c is seen in Figure 3.6b).

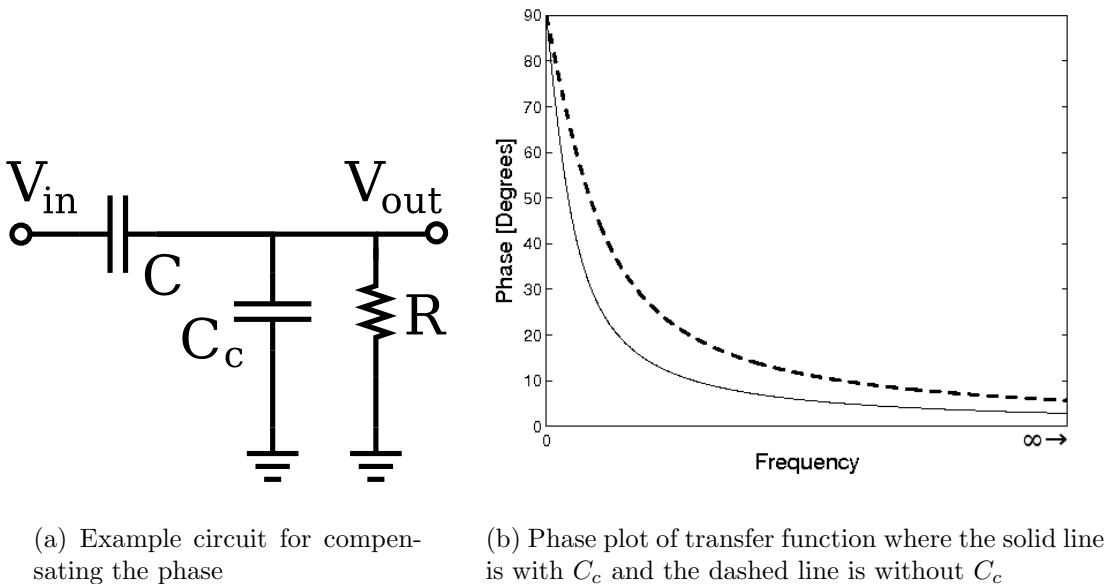


Figure 3.6: Effects of C_c on a simple RC circuit

The solid line shows that for some value of C_c , the phase with respect to the input will

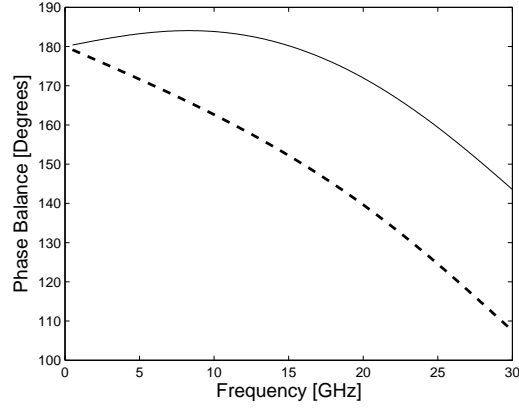


Figure 3.7: Balun circuit simulated over a large bandwidth. The dashed line is the original circuit and the solid line is the circuit with the compensating capacitor.

be reduced compared to the original circuit without C_c . Note that at low frequencies, the amount of change due to C_c is very little, but the difference C_c makes in phase increases and then decreases again. If we now refer back to the circuit in Figure 3.6a) it is evident that it is similar to the capacitor and resistive network at the input/output of v_{o2} in the balun circuit depicted in Figure 3.4.

$$\frac{v_{out}}{v_{in}} = T(s) = \frac{\omega^2 R^2 C(C + C_c) + j\omega CR}{1 + (\omega R(C + C_c))^2} \quad (3.17)$$

$$\phi = \tan^{-1} \left(\frac{\omega CR}{\omega^2 R^2 C(C + C_c)} \right) = \tan^{-1} \left(\frac{1}{\omega R(C + C_c)} \right) \quad (3.18)$$

A parallel is drawn if C is now equated to Z_{gs} and R is equated to R'_D . This parallel gives a good indication of the effect that C_c will introduce.

The aforementioned compensating capacitor C_c , is then implemented in parallel with R'_S at the source to ground. The schematic for this new design is shown in Figure 3.8. Note the addition of the compensating capacitor C_c .

As previously mentioned, the effectiveness of the compensating capacitor tapers off at very high frequencies. This is seen in Figure 3.7 in which the transfer function with the compensating capacitor depicted as a solid line is simulated. It is clear

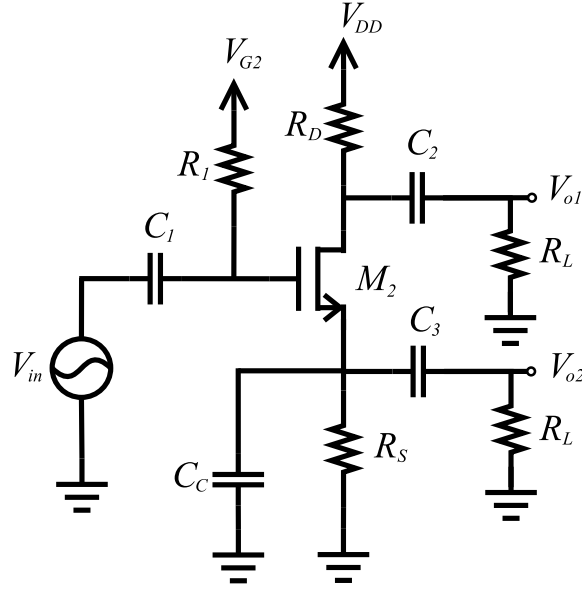


Figure 3.8: Schematic of the capacitor compensated single transistor balun

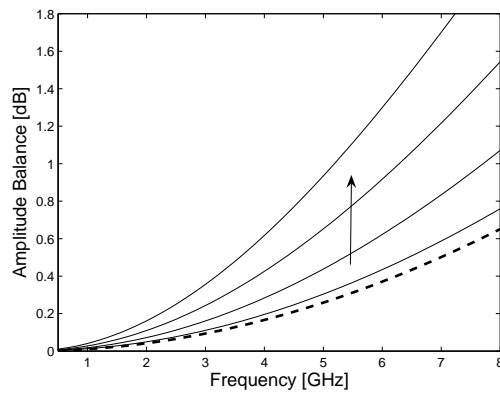
that C_c overcompensates at mid frequencies and then under-compensates at high frequencies. Thus any sized C_c has a limit to the bandwidth in terms of phase that can be compensated. Note that the phase mentioned here is only the phase between v_{in} and v_{o2} and not the total phase balance. However any reduction of the phase in v_{o2} with respect to v_{in} , will also reduce the overall phase between both outputs.

In producing the final set of equations, it is noted that Equations 3.1 and 3.2 are still valid, along with the assumption that C_1 , C_2 , C_3 and R_1 are sufficiently large. Again R_S is set equal to R_D to preserve symmetry. However because of the extra C_c , R'_S and R'_D are now different as C_c is placed in parallel with R'_S . As before, r_o is ignored as its value is assumed to be sufficiently large. The whole set of equations are adjusted to reflect the changes and reproduced as Equations 3.19.

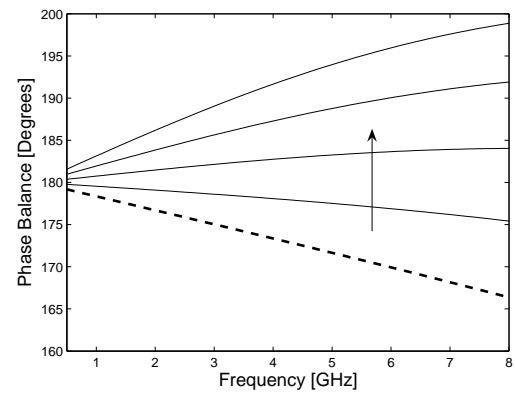
$$\begin{aligned}
R'_S &= R_S \parallel R_L \parallel \frac{-j}{\omega C_c} = \frac{R_S R_L}{j\omega C_c R_S + j\omega C_c R_L + 1} \\
R'_D &= R_D \parallel R_L = \frac{R_D R_L}{R_D + R_L} \\
K &= \frac{v_{o1}}{v_{in}} = \frac{-g_m R'_D}{1 + g_m R'_S} \\
Z_{gs} &= \frac{-j}{\omega(C_{gs} + C_{gd}(1 - K))} \\
Z_{ds} &= \frac{-j}{\omega(C_{gd}(1 - \frac{1}{K}))} \\
\frac{v_{o2}}{v_{in}} &= \frac{Z_{ds}^2 + Z_{ds} R'_D + g_m Z_{gs} Z_{ds}^2 + g_m Z_{gs} Z_{ds} R_d - g_m R'_D Z_{gs} Z_{ds}}{Z_{ds} Z_{gs} R'_S + Z_{ds}^2 R'_S + Z_{ds} R'_D R'_S + g_m Z_{gs} Z_{ds}^2 R'_S + Z_{gs} Z_{ds}^2 + Z_{gs} Z_{ds} R'_D} \\
\frac{v_{o1}}{v_{in}} &= \frac{v_{o2} R'_D - g_m R'_D Z_{ds} + g_m R'_D Z_{ds} v_{o2}}{Z_{ds} + R'_D}
\end{aligned} \tag{3.19}$$

The derived transfer function and the more accurate device level model was evaluated in Matlab and ADS with various compensating capacitances to see their effects. Figure 3.9 demonstrates the effects of sweeping C_c from 100 to 400 fF. The original circuit was plotted alongside for comparison and is depicted as the dashed line.

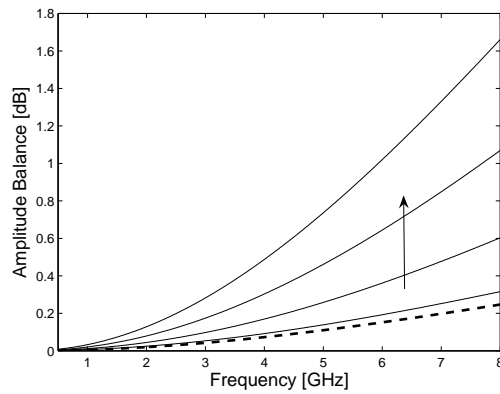
Again, in a perfect balun, the amplitude balance should be exactly 0 dB and the phase balance 180°. The arrow shows the trend as the capacitance is increased. It is seen that as C_c increases, the phase between both outputs also increases. Because of the extra capacitance, the circuit begins to shunt more current at the source when compared to the drain, thus shifting the balance away from the original $\simeq 0$ dB amplitude balance. A compromise needs to be chosen in the selection of C_c that gives a good phase balance and an acceptable amount of amplitude balance. The amplitude balance is clearly the limiting factor. As a result the previously mentioned limit of the phase compensation due to the roll-off of the effectiveness of C_c is at a much higher frequency in comparison to the amplitude balance increase making this factor less of a concern. Comparing the ADS simulated device in Figures 3.9c) and 3.9d) to the analytical equations from Matlab that produced Figures 3.9a) and 3.9b), it is



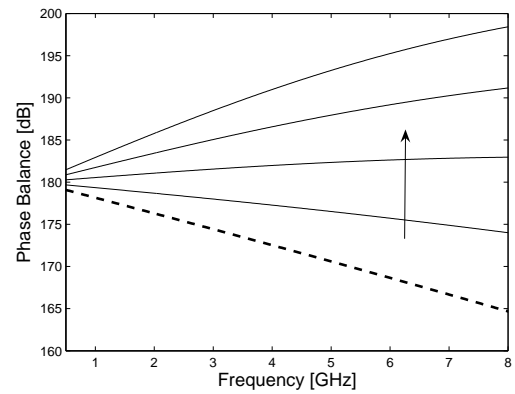
(a) Simulated amplitude balance using Matlab



(b) Simulated phase balance using Matlab



(c) Simulated amplitude balance using ADS



(d) Simulated phase balance using ADS

Figure 3.9: Simulated results for analytical equations in Matlab and circuit level simulations in ADS when various values of C_c are swept from 100 to 400 fF

noted that the amplitude balance is predicted (seen as the dashed line) to be larger than the actual device level simulation but the phase balance produced is remarkably close (within 3°).

3.3.2 Common Gate Input Matching

The single transistor circuit introduced earlier has the input applied to the gate of the transistor. The input impedance for the balun is given in Equation 3.21. Because C_{gs} and C_{ds} are low, the resulting gate input impedance is very high and looks practically like an open circuit. Substituting typical values of C_{ds} and C_{gs} and the values of R'_D and R'_S in a $50\ \Omega$ for this circuit, the corresponding S_{11} is $-0.23\ \text{dB}$, or essentially an open circuit. Having such a high input impedance produces an undesired amount of reflection and reduces the amount of power that can be delivered to the device as well as potentially damaging the source as the waves reflect back into it. Several methods exist to improve the input matching. A simple inductor capacitor matching network is one example, however because they are tuned for one particular frequency and because of the large amount of space required for an inductor, it was elected to use a common gate amplifier to provide input matching.

$$Z_{in} = \left(\frac{1}{j\omega C_{gs}} + R'_S \right) \parallel \left(\frac{1}{j\omega C_{gs}} + R'_S \right) \quad (3.20)$$

$$Z_{in} = \frac{R'_S C_{gd} C_{gs} \omega^2 + R'_D C_{gd} C_{gs} \omega^2 - C_{gd} j\omega - C_{gs} j\omega}{C_{gd} C_{gs} \omega^2} \quad (3.21)$$

The schematic of the amplifier is shown in Figure 3.10. The input looking into the source of the transistor is approximately $1/g_m$ [23]. From Equation 3.22 it is seen that g_m is proportional to the width of the transistor. As a result the transistor size

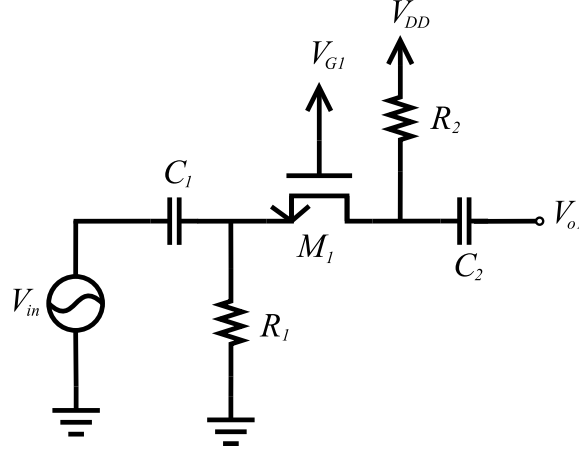


Figure 3.10: Schematic of common gate amplifier used for input matching

can easily be set to match the input impedance of the $50\ \Omega$ system.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t) \quad (3.22)$$

The gain of this circuit would like to be determined, but the output will be connected directly to the gate of the balun circuit which looks like an open circuit to the common gate amplifier. Consequently, the conventional way of measuring gain in simulations using S-parameters gives misleading results. This is because the port at the output of the amplifier will be loaded with very small $50\ \Omega$ resistance. This is very different from the actual load of something closer to an open circuit at the gate of the balun. To get a more accurate picture, an ideal buffer circuit with infinite input impedance and a perfectly matched output impedance is connected to the output of the common gate amplifier will provide an open circuit to the output while matching the $50\ \Omega$ load at the S-parameter output port. This method will provide a more accurate picture of the gain produced by this circuit.

The results of the two methods are shown in Figure 3.11a) where the circuit loaded with the $50\ \Omega$ load and Figure 3.11b) in which a buffer circuit is placed before the load. Note that there is an 8.5 dB difference between the two. Accordingly, the use

of the buffer tells us that we can reasonably expect a gain of about 3.5 dB from the common gate amplifier in addition to helping provide an input match. The dip at the low frequencies is because of the bypass capacitor placed at the input and output. At low frequencies, the bypass capacitor acts as an open circuit, significantly attenuating the signal, however as this circuit will be operating typically above 0.5 GHz, this will not be an issue.

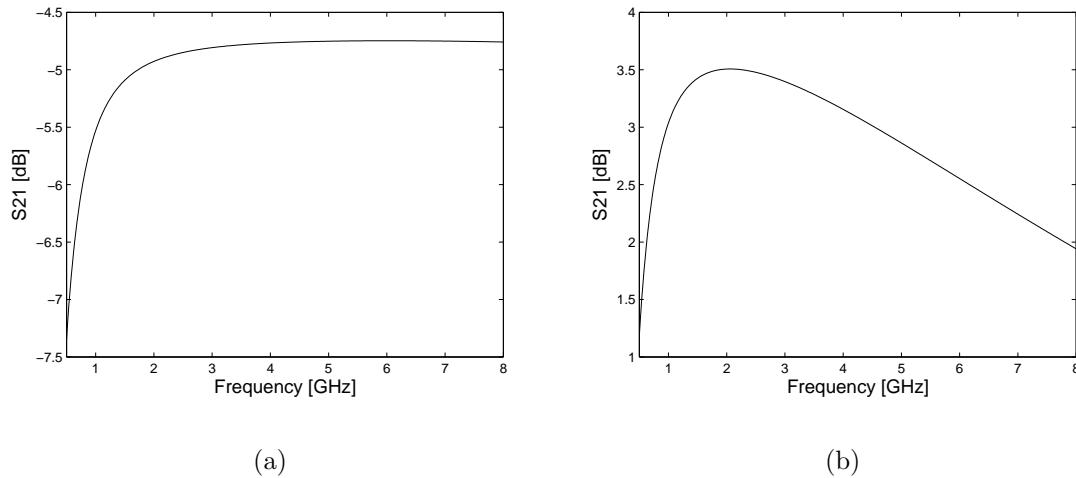


Figure 3.11: S_{21} of common gate amplifier if a) $50\ \Omega$ is placed directly at the output or b) Buffer circuit is used to match

The resulting input reflection S_{11} proves to be a good match and gives an average of 20 dB return loss (note that S_{11} is unaffected by the load at the output of the circuit) and is shown in Figure 3.12a). The input referred 1 dB compression point (P_{1dB}) is determined to be 2 dBm. This shows good power handling which enables us to operate this amplifier to very high power levels by CMOS standards.

3.3.3 Final circuit

The final design with both the input matching common gate amplifier along with the one transistor balun is shown in Figure 3.13. The appropriate C_c of 260 fF was

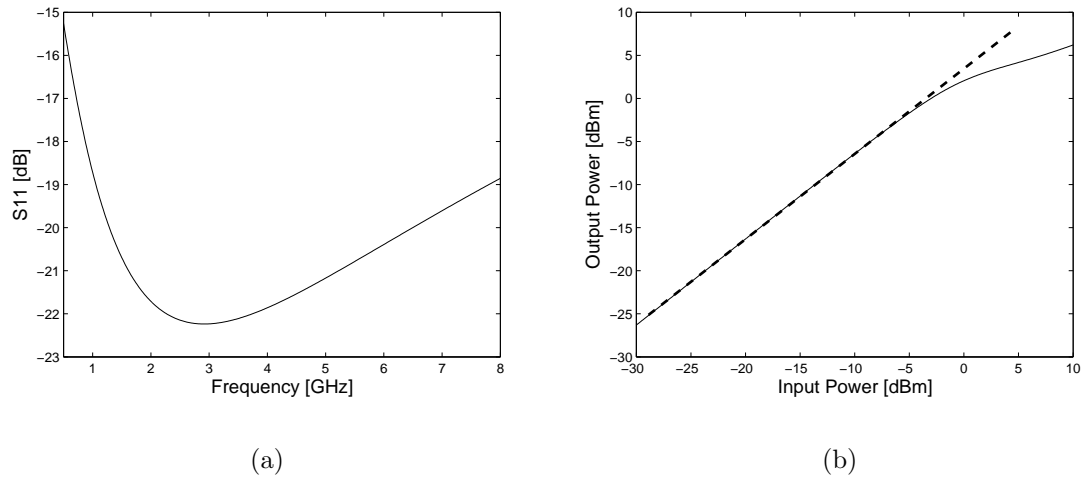


Figure 3.12: a) Input reflection, b) P_{1dB} compression point of the common gate amplifier used for input matching

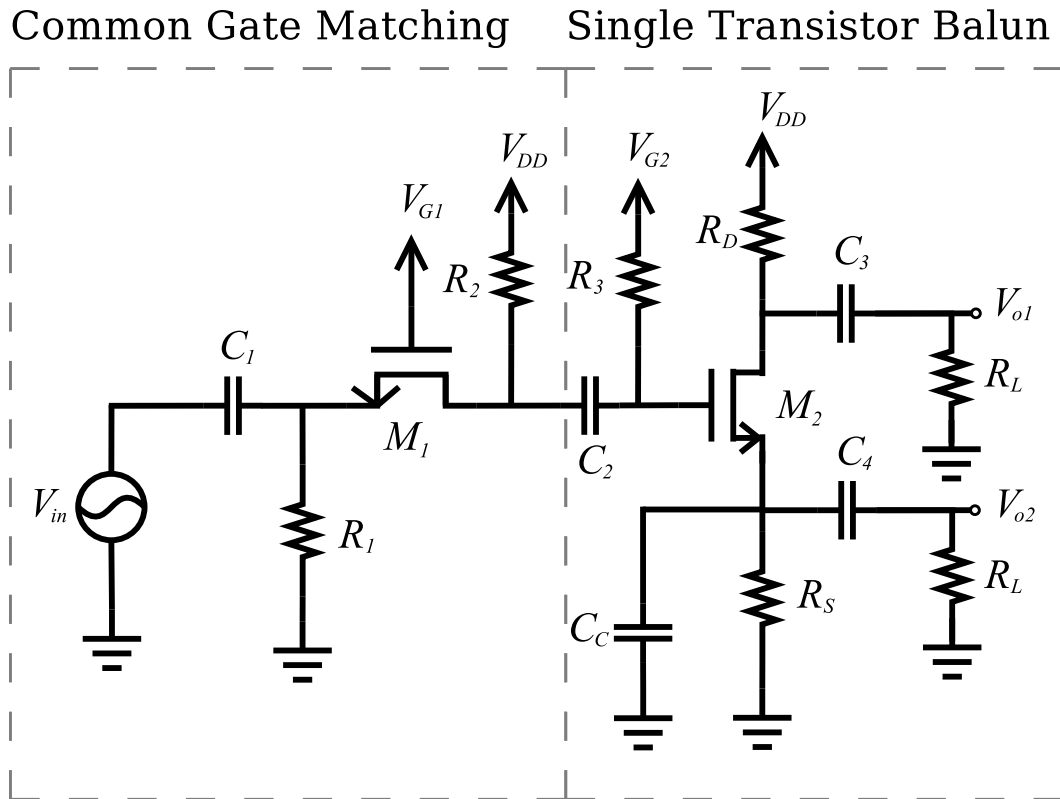


Figure 3.13: Schematic of the full capacitor compensated single transistor balun including the common gate input stage

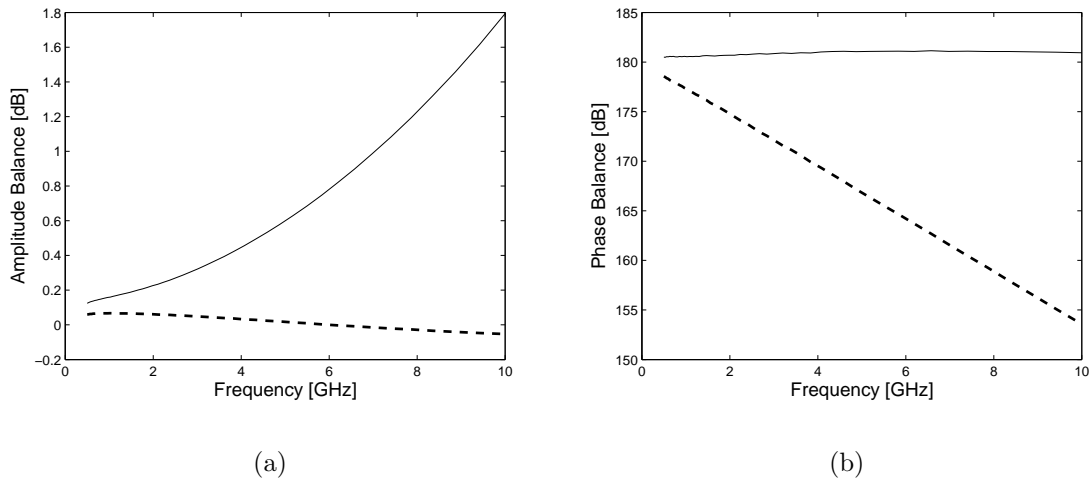
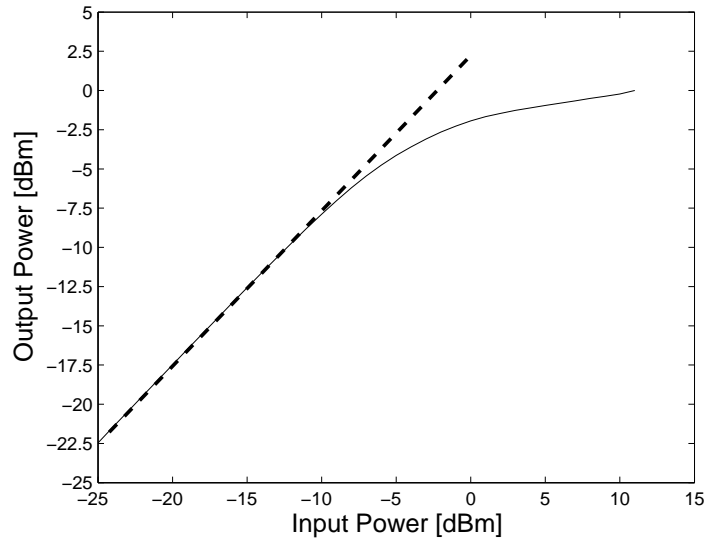


Figure 3.14: Simulated a) Amplitude Balance and b) Phase balance where the dashed line is the original design and the solid line is the compensated balun

selected. This gives the best phase and amplitude balance. The final layout was simulated in SpectreRF. For reference, the design was simulated with and without the compensating capacitor. The original circuit is shown as the dashed line and demonstrates that the amplitude balance is closely matched past 8 GHz, however the phase balance decreases very rapidly. With the addition of the extra compensating capacitor C_c , the phase is kept to slightly above 180° and is shown as a solid line in Figure 3.14. However, the tradeoff here is that the amplitude imbalance has increased. Overall the circuit provides good amplitude and phase balance past 8 GHz. Along with this, the device will provide a peak 0.75 dB gain and produce a low input reflection.

The final P_{1dB} shown in Figure 3.15 is determined to be -5 dBm. The compression point is reduced because of the balun, however overall the performance is still acceptable and is still considered good power handling.

Figure 3.15: Simulated P_{1dB} compression point

3.4 Measurement Results

The device was fabricated and connected to the test equipment on a Wentworth probe station using a 40 GHz coplanar waveguide (CPW) ground signal ground (GSG) probe for the input and a ground signal ground signal ground probe (GSGSG) of the same type for the outputs. The Agilent 8510C 50 GHz vector network analyzer that was used to measure the phase and amplitudes was calibrated with a SUSS MicroTec calibration substrate using a full two port short-open-load-through (SOLT) calibration method. A -10 dBm power level was chosen for the network analyzer and the device was swept from 500 MHz to 8 GHz. The gate voltage of the balun was chosen to be 1.1 V to match the simulations and V_{DD} was set to 1.8 V.

Figure 3.16 shows the amplitude and phase balance for the chip. The amplitude balance does not increase more than ± 1 dB over the frequency range between 500 MHz to 8 GHz. The phase balance begins just below 180° but increases to a maximum of 190° over the same frequency range. It is concluded that this device performs exceptionally well across over a 7.5 GHz bandwidth. The reason for the discrepancy

between the measured results and those predicted in simulations is because the small value of the compensating capacitor used in this circuit will be significantly affected if there is any slight variation in the metal-insulator-metal (MIM) capacitor model that is used.

For the input referred P_{1dB} compression point, Anritsu MG3694A signal generator for the input signal and an Agilent E4446A spectrum analyzer to determine the output. The results are depicted in Figure 3.18. The input referred P_{1dB} was measured at 2 GHz and it is found to be -5.8 dBm.

The phase balance performs worse in the measured results when compared to the SpectreRF simulations. In Figure 3.9 the compensating capacitor was swept from 0 to 400 fF. When the value of C_c was too large, the phase would increase past 180° . Conversely the amplitude imbalance would also increase proportionally to the size of C_c . The measured data confirms simulations of the compensating capacitor that has been chosen to be too large. It is thus concluded that the MIM capacitor models used in the simulations either made C_{gd} or C_{gs} too small. This resulted in the selection of an overcompensated C_c that gave us these measured results. Nevertheless, the measured data results in a balun that provides good performance over a 7.5 GHz bandwidth with good input reflection, gain and 1 dB compression point.

A micro-photograph of the device is seen in Figure 3.19. Note the input used a GSG probe while the output was extracted using a GSGSG probe. 3 DC pads were used to provide power, gate bias voltage and a ground connection. The total size of the device was $300 \times 510 \mu m$ or $0.153 mm^2$ and $160 \times 425 \mu m$ or $0.068 mm^2$ without the DC and RF bonding pads. As the selection of C_c proved that we have overcompensated for the phase, future work will encompass a reduction in C_c that will significantly improve the amplitude and phase balance.

It is difficult to compare this work to existing literature on active baluns because each circuit functions over very different frequency bandwidths. In addition, each

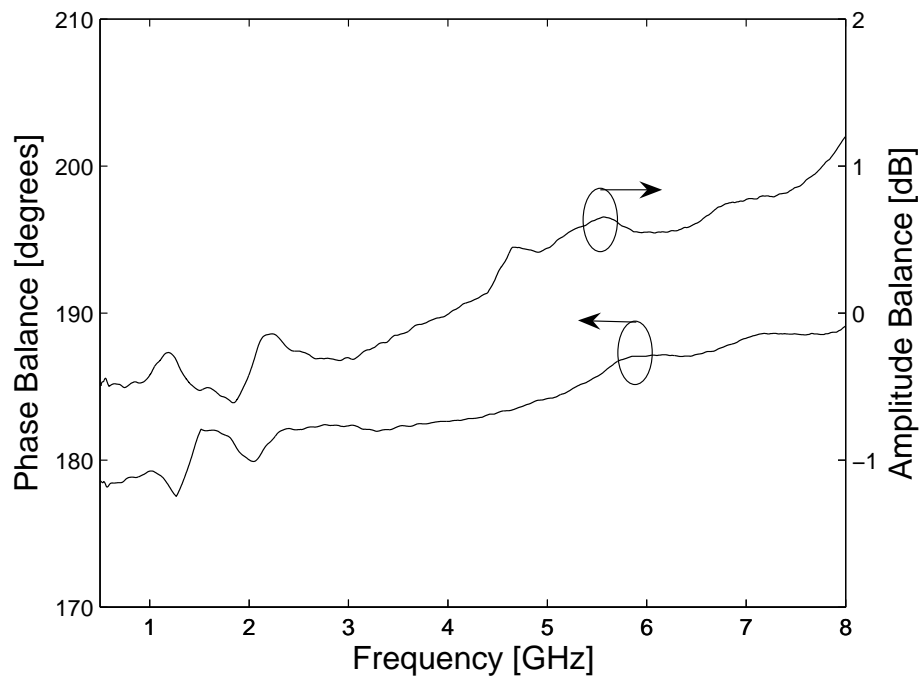


Figure 3.16: Measured Phase and Amplitude Balance for capacitor compensated balun

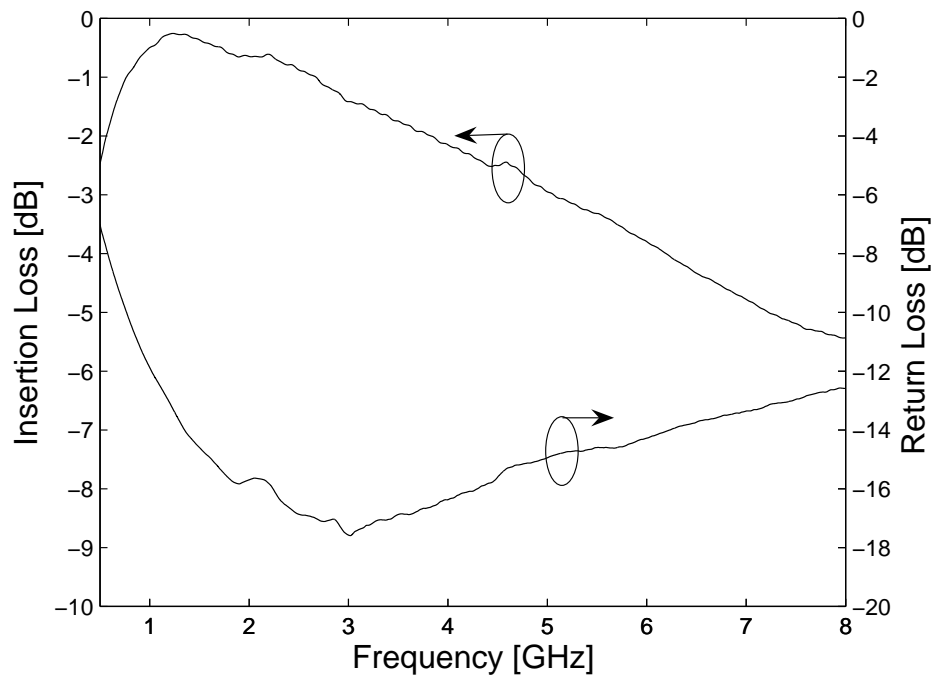


Figure 3.17: Measured transmission gain and return loss for capacitor compensated balun

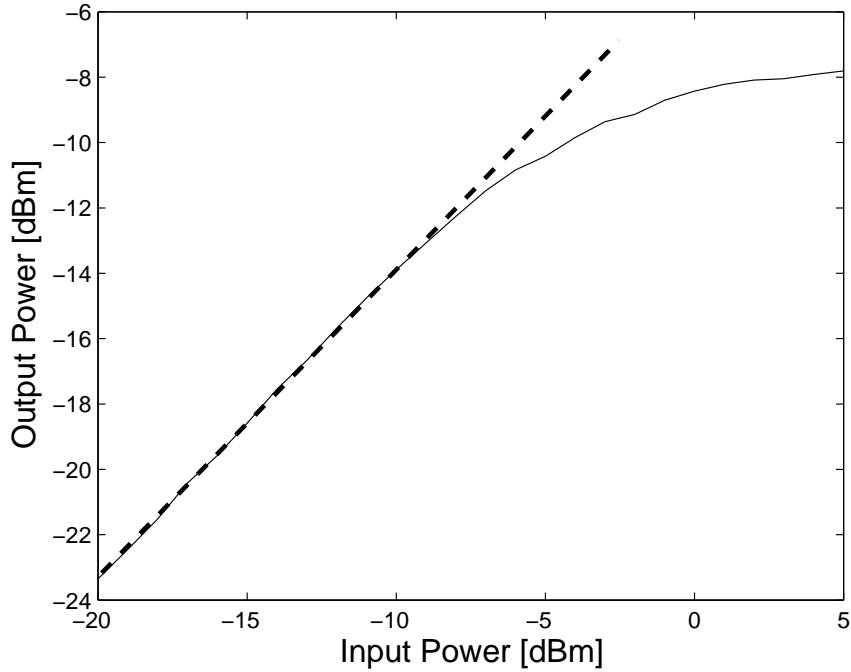


Figure 3.18: Measured P_{1dB} of capacitor compensated balun

circuit has its own metrics on what was the acceptable amount of phase or amplitude imbalance. Thus a figure of merit (FOM) was devised in order to place all the metrics on equal ground. As all three criteria are crucial in any balun design, the exact weighting of each metric is quite arbitrary. That is to say, one might consider one metric to be of high importance while another may consider another metric to be of high importance and weigh them accordingly. The weighting of each element has thus been left equal in order to provide a unbiased weighting on any of the three metrics.

The total change in phase and amplitude balance ($\Delta\phi\Delta A$) across the bandwidth was placed inversely proportional to the total bandwidth (Δf). The resulting FOM formula used is found in Equation 3.23. Any balun with the largest bandwidth and

	Δf [GHz]	$\Delta\phi$ [°]	ΔA [dB]	FOM [$GHz/^\circ dB$]
This work	7.5	8	1.5	0.625
[16]	1	4	0.8	0.313
[17]	3.5	5	2	0.35
[18]	10	8	4	0.313

Table 3.1: Values used to calculate figures of merit

the smallest phase and amplitude balance will result in the largest FOM value.

$$FOM = \frac{\Delta f}{\Delta\phi\Delta A} \quad (3.23)$$

The data used and the resulting FOM is found in Table 3.1. The devised FOM shows that this device outperforms the existing literature for CMOS processes by almost a factor of two.

	Freq. Band	S_{21}	S_{11}	P_{1dB}	Size	FOM	Technology
TW	0.5-8 GHz	-3 dB	-16 dB	-5.8 dBm	0.068 mm^2	0.625	0.18 μm Si CMOS
[16]	5-6 GHz	16 dB	-20 dB	-14.4 dBm	0.840 mm^2	0.313	0.25 μm Si CMOS
[17]	1.5-4 GHz	-3 dB	-16 dB	-10 dBm	—	0.350	0.18 μm Si CMOS
[18]	10 GHz	—	—	—	0.570 mm^2	0.313	0.18 μm Si CMOS

Table 3.2: Comparison of various active baluns

Table 3.2 shows the other properties of existing baluns in literature. Both these baluns found literature rely on two transistors, one providing the 180° phase shift through a common source amplifier and the other providing a 0° through a common gate amplifier.

This balun is able to perform with excellent phase and amplitude performance while maintaining very low power consumption and device area. In addition, its power handling capabilities as shown in the P_{1dB} compression point.

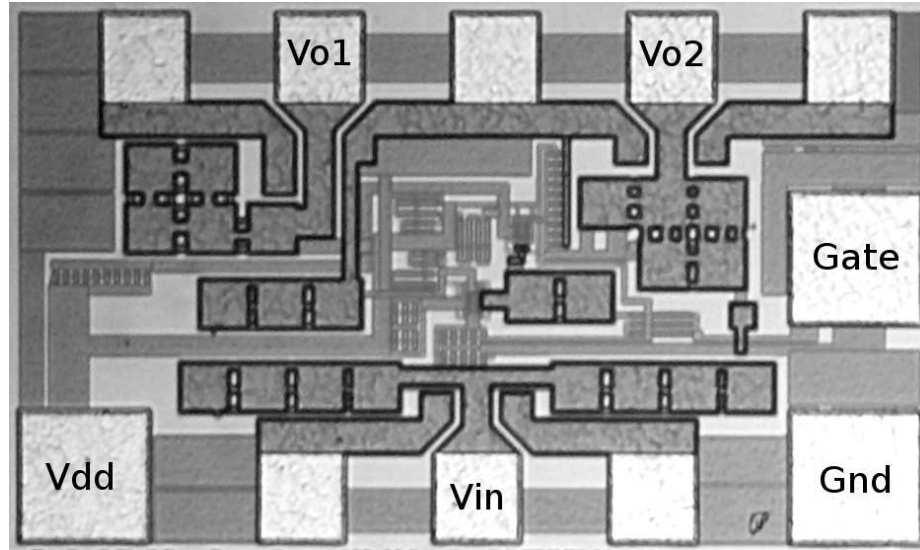


Figure 3.19: Micro-photograph of capacitor compensated balun circuit

3.5 Conclusions

In this chapter, a single transistor active balun was introduced and analyzed. A set of equations were produced and plotted to show the limited bandwidth of this design. A compensating capacitor was then introduced to counter the effects of the parasitic capacitances C_{gs} and C_{gd} . The new simulated results show that the usable bandwidth is increased dramatically as the phase balance is compensated with the new capacitor C_c . A common gate amplifier was placed at the input to improve the return loss and as a byproduct the loss through the balun was counteracted through the moderate gain of the input stage. The measured results showed that the value of the compensating capacitor was selected too high, however the device still showed a marked improvement over the original design. Future work involving more accurate MIM capacitor models will enable this device to further increase its bandwidth. This new device has a 7.5 GHz bandwidth with a -3 dB insertion loss, 16 dB return loss, -5.8 dBm compression point while only consuming 12 mW. These parameters when compared to existing devices prove to be very competitive, improving or equaling most devices in its class.

Chapter 4

Inductorless Quadrature VCO

4.1 Introduction

Voltage controlled oscillators (VCO) can be used in a wide variety of applications. Most frequently they are used as part of a phase locked loop (PLL) system because of their tunability. The ability to generate a quadrature signal allows the elimination of an additional quadrature generator that is required in addition to an oscillator for a quadrature phase shift keying system (QPSK). Conventional oscillators require large inductors for use in a resonator tank, however because this device synthesizes one, such a tank this is not necessary. This results in substantial space savings. However the trade off for inductorless oscillators is that the overall phase noise is higher. In this chapter we demonstrate a very wide band tunable dual integrator oscillator based on operational transconductance amplifiers (OTA) that produces a quadrature output at a reasonably high power.

4.1.1 Oscillator Model

Oscillators can be modeled through a feedback model shown in Figure 4.1. In general, an input signal is passed through a very sharp high Q resonator $T(s)$ in order to produce a single tone sinusoid and filter out all other frequencies. The output is then

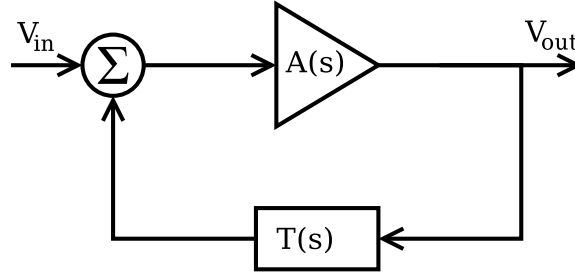


Figure 4.1: Generalized feedback model for a negative feedback system

passed through an amplifier $A(s)$ to recover any losses through either the resonator or other parasitic elements. The signal is then fed back into the resonator to complete the feedback loop. Contrary to a typical negative feedback system, the desire here is to produce an unstable system that will synthesize the sinusoid.

Examining the transfer function, it is seen that if Equation 4.2 is true then Equation 4.1 will reach infinity. This requisite is called the Barkhausen criterion [23][42].

$$F(s) = \frac{v_{out}}{v_{in}} = \frac{A(s)}{1 - A(s)T(s)} \quad (4.1)$$

$$A(s)T(s) = 1 \quad (4.2)$$

It also follows that if $A(s)T(s) < 1$, then the sinusoid will die down and no oscillations will occur. In addition if $A(s)T(s) > 1$, then the oscillations will increase exponentially. These three conditions are all highlighted in Figure 4.2a). In this situation, if no input is applied, (i.e. $v_{in} = 0$), a sinusoidal output will still be produced.

It seems logical to set the parameters for the oscillator to be exactly unity, however under this condition, any small amount of fluctuations in tolerances or changes in environment (such as temperature) will alter the conditions and potentially allow the poles of $A(s)T(s)$ to move from their position on the imaginary axis. As such this will cause the oscillations to either increase to infinity or attenuate to zero.

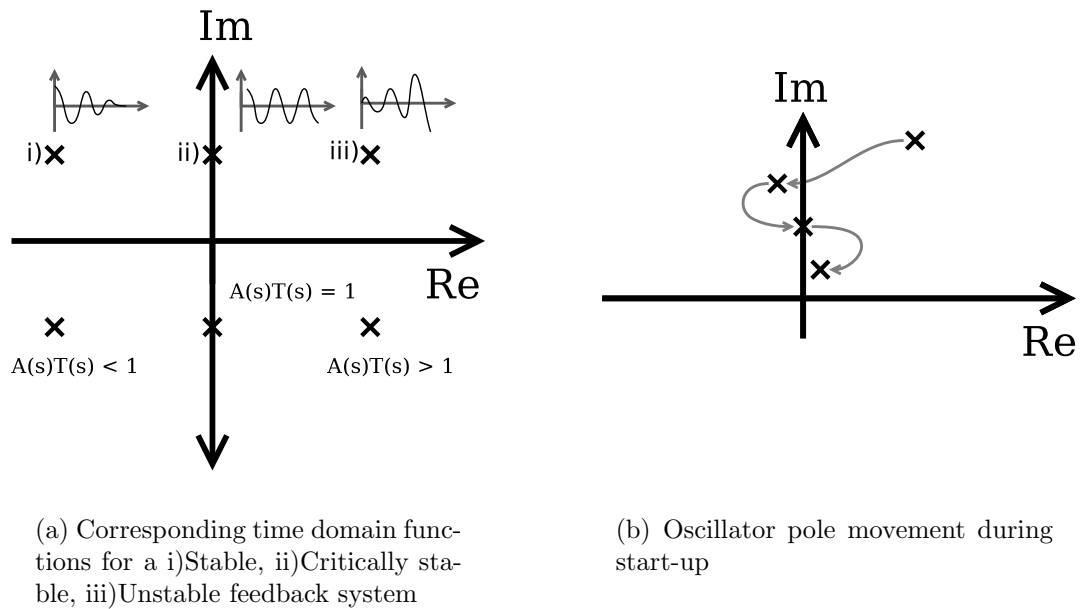


Figure 4.2: Poles of an oscillator on the S-plane

In practice, in order to avoid the latter condition, the oscillator is designed to be on the right hand plane (RHP). It follows that if the poles are on the RHP, then oscillations will increase to infinity. However this does not occur because no real world device can produce an infinite voltage. From Figure 4.2b), when oscillations start, the poles are located in the RHP, at a certain point the transistors in the amplifier will begin to saturate and in effect the system will self limit the oscillations. In doing so, will move the poles back towards the imaginary axis. There may be additional subtle movements from the poles that try to adjust itself to find its equilibrium. Nevertheless the poles will eventually settle down onto the imaginary axis. Subsequently, all practical oscillators are designed to be on the RHP and through non-linear effects the poles are moved back to the imaginary axis.

If $T(s)$ is of the standard form as shown in Equation 4.3, the quality factor and resonator frequency (ω_o) can be derived from the transfer function of the resonator [43].

$$T(s) = \frac{sA_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \quad (4.3)$$

4.1.2 Quality Factor

The Q factor for a sinusoidal system is a measurement of the ability of a system to retain energy over the energy lost. Equation 4.4 is the standard definition of the Q factor [24].

$$Q = \omega \frac{\text{energy stored}}{\text{average power dissipated}} \quad (4.4)$$

This general definition can be used for many applications in a wide variety of fields such as a mechanical spring system or optical resonant cavities as well as to describe our sinusoidal oscillator system. Figure 4.3 depicts a visual representation of quality factor for a resonator or filter system.

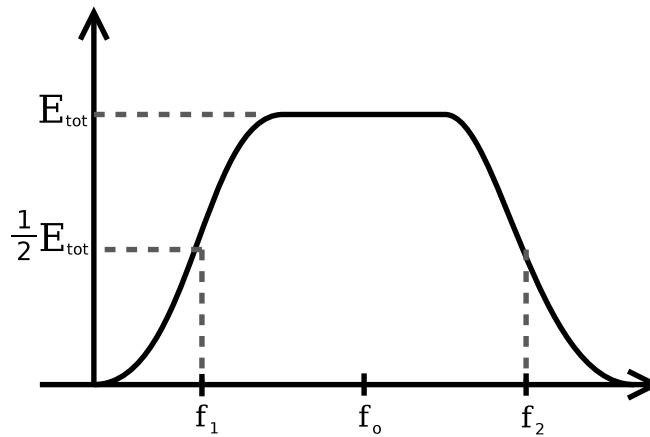


Figure 4.3: Visual representation of a filter function

It can be shown for a given system, the Q factor is the ratio of the center frequency over the bandwidth. The cutoff for the bandwidth is when the total energy is half of the maximum. It is clear that the wider the bandwidth, the lower the Q.

In a high Q resonator, the bandwidth is very narrow and produces a very sharp peak. For a given oscillator system with a high Q, this translates to a system that will

resonate at one and only one specific frequency. Thus it is desired for any resonator to contain a high Q resonator.

4.1.3 Phase Noise

An ideal oscillator is described as an impulse function in frequency domain. However due to noise within the system and non-ideal components, the oscillator will produce slight amounts of phase irregularities and spread in the frequency domain. The mathematical characterization of this is called phase noise and is given in Equation 4.5 [8].

$$L(f) = \frac{P_n}{P_c} \quad (4.5)$$

Phase noise is defined as the ratio of noise power in a single sideband to the carrier power. Most frequently, this ratio is expressed in decibels relative to the carrier. Phase noise is a particular issue in transceiver systems. Figure 4.4a) depicts a receiver situation in which there are two signals, the desired channel and an adjacent channel. Both signals are then received into the system and downconverted with a dirty local oscillator (LO) using a mixer. Because of the phase noise within the LO, the adjacent channel's spectrum 4.4b) spreads out after mixing. This spread then overlaps with the desired spectrum, thus causing interference and corruption. For a transmitter system, a dirty LO will cause the corrupted upconverted signals to interfere with adjacent channels causing significant problems as it affects other systems. As a result, phase noise is strictly monitored and many standards require LO to meet stringent requirements.

Once again examining the standard oscillator model in order to relate this to phase noise, we examine what causes this spread. If the feedback amplifier $A(s)$ is assumed to be noiseless (its actual noise contribution especially in an inductorless oscillator is far below that of the resonator), then sole contributor of phase noise is the filter $T(s)$. So far the filter has been assumed to be perfectly sharp and as such only allows

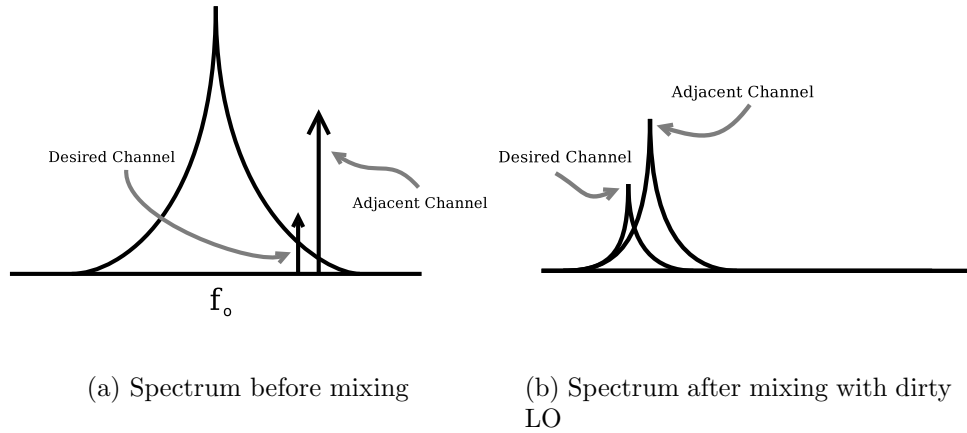


Figure 4.4: Effects of receiving with dirty LO [44][45]

one frequency to resonate. If this is the case, then the phase noise is limited to only the thermal background noise in the system. However in any real filter system, there are associated non-ideal components. In a typical LC tank resonator, there exists a series resistance that occurs in the coil. In addition, for voltage controlled oscillators, varactor are typically used in place of capacitors so that the frequency can be changed. A typical transistor type varactor has significant serial resistance from the transistor, thus adding to this parasitic resistance and lowering the Q .

For such a LC tank oscillator assuming a noiseless environment (e.g. the only noise is caused by the lossy parasitic resistance), the general phase noise equation for this system can be found in Equation 4.6 [24][45][44].

$$L(\Delta\omega) = 10\log \left(\frac{2kT}{P_{sig}} \left(\frac{\omega_o}{2Q\Delta\omega} \right)^2 \right) \quad (4.6)$$

Note that this ignores other noise sources such as noisy resistors, noise from the amplifiers, pink ($1/f$) noise and the overall noise floor which results in a phase noise that is in reality much higher [24].

P_{sig} is the output power of the oscillator and $\Delta\omega$ is the distance away from the oscillation frequency ω_o . Note that the output power and Q are inversely proportional

to the phase noise. It then follows that for a higher output power or Q , a lower phase noise will result. This is not surprising as the definition shows that for a high Q , the resulting resonator will restrict any other frequency from resonating. As a result of this, a large research area is dedicated in finding materials or methods of developing high Q resonators.

The goal in this design is consequently to maximize Q and P_{sig} . As discussed before, this oscillator is “self-limiting” and the circuit will be already operating with maximum power output. Limited by the inability to increase the output power without increasing overall power consumption, the only other degree of freedom is changing the quality factor of resonator tank. A more detailed look at how the Q factor can be changed is covered in a later section. However it is sufficient to say that certain circuit limitations prevent the circuit from producing a very high Q .

4.1.4 Harmonic Oscillators

In general the expression for a second order harmonic oscillator is given below in Equation 4.7. Where b determines the locations of the poles on the s -plane. If the Laplace transform is applied, then the result is seen in Equation 4.8 [46].

$$\frac{dx^2}{dt^2} + b\frac{dx}{dt} + \omega_o^2x = 0 \quad (4.7)$$

$$s^2 + bs + \omega_o^2 = 0 \quad (4.8)$$

The harmonic oscillator model can be derived from the feedback equation mentioned in 4.3 if the input is set to zero (as in the case of a self sustaining oscillator, no input signal is required). The frequency of oscillation is expressed as ω_o in rad/s. For a harmonic oscillator, the oscillation condition now rests with b . The variable b dictates the location the poles are relative to the imaginary axis. As discussed before b needs to be set slightly negative in order for oscillations to begin.

There are two equations that define the functionality of an oscillator. The harmonic equation (4.7) defines the oscillation conditions determined by the location of b and the oscillation frequency determined by ω_o^2 . The second equation (4.3) is the resonator transfer function. This equation demonstrates the quality of the resonator along with its oscillation frequency. As mentioned before, the Q factor is directly correlated with the phase noise. These two equations can be derived from each other, however each equation gives pertinent information about the oscillator.

4.2 Circuit Description

4.2.1 Operational Transconductance Amplifiers

Operational Transconductance Amplifiers (OTA) are amplifiers in which the input is a voltage differential and the output is given as a current. In this chapter the basic cell of the device was kept straightforward through the use of a simple MOSFET differential pair with active loading in the form of a current mirror at the output. The circuit symbol, idealized circuit and the actual schematic are given in Figure 4.5. The OTA model for amplifiers is particularly suited for MOSFETs as it emulates the internal circuit model of an input v_{gs} and the current controlled output i_{out} . The advantage of using this OTA cell is that the first order idealized version is almost identical to the actual cell that is used. This relationship is seen in Equation 4.9.

$$\frac{i_{out}}{v_{in}} = \frac{i_{out}}{(v_{in+} - v_{in-})} = g_m \quad (4.9)$$

$$g_m = \frac{I}{V_{GS} - V_t} \quad (4.10)$$

The transconductance g_m can easily be controlled with a current source I as shown in Equation 4.10. One method of controlling the current source is through a current mirror depicted in Figure 4.6. It follows that for a current mirror, the currents (I_R

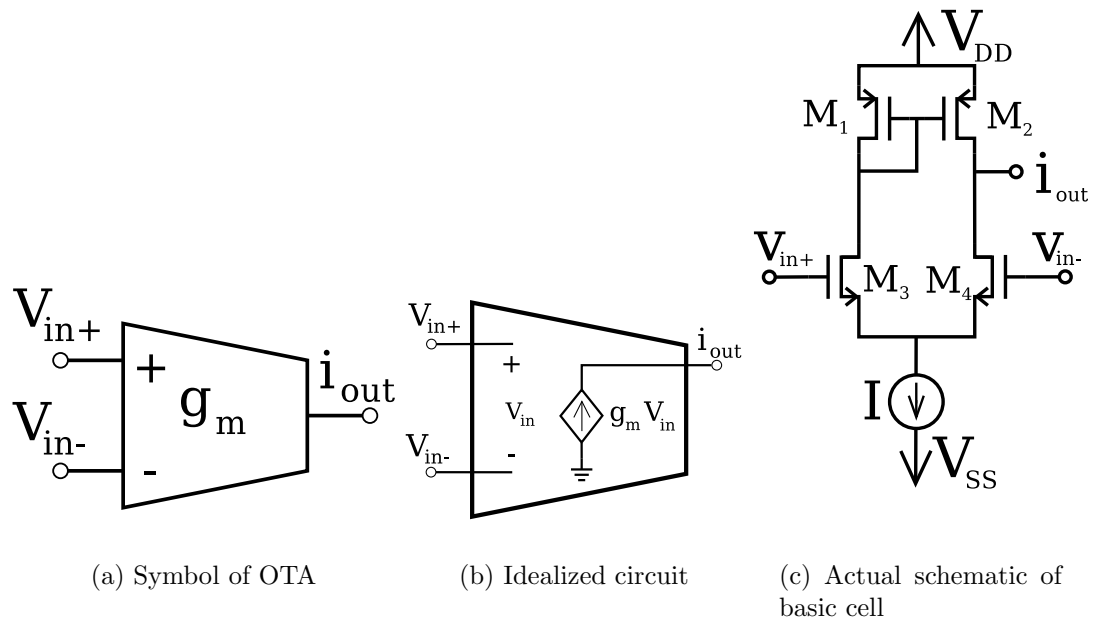


Figure 4.5: Various representations of OTA models in this chapter

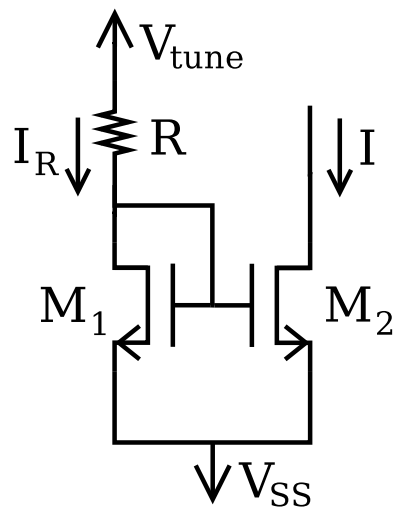


Figure 4.6: Schematic of a method for controlling the OTA current

and I) are proportional to each other. Thus the current I_R (and as a result I) can be controlled by altering V_{tune} allowing us to directly control g_m .

The parasitics such as r_o , C_{gs} , C_{gd} have all been omitted in order to simplify the analysis and to allow a concise hand derived transfer function to be obtained. These parasitics are later added in the simulations.

4.2.2 Oscillator Circuit

The overall system level schematic for this circuit is a dual integrator quadrature oscillator taken from [43] and updated. The entire system is depicted in Figure 4.7. Similar to the derivation of the Colpitts we begin with the basic feedback model shown in Figure 4.1 where $T(s)$ emulates a resonator while $A(s)$ is the feedback amplifier.

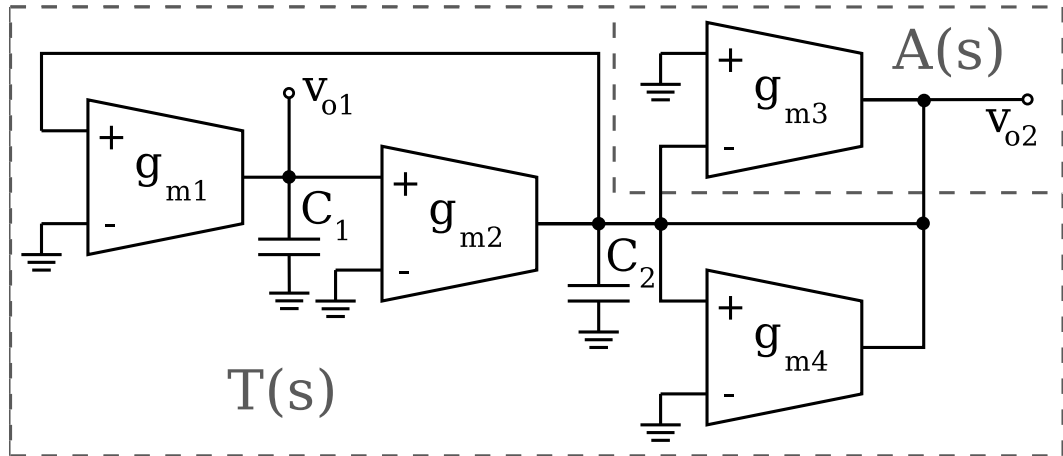


Figure 4.7: Schematic of OTA voltage controlled oscillator

The components that compose the transfer function $T(s)$ and amplifier $A(s)$ are distilled from this circuit and are shown to be Equations 4.11 and 4.12. Note the location of $T(s)$ and $A(s)$ in the original schematic.

$$T(s) = \frac{s \frac{1}{C_2}}{s^2 + s \frac{g_{m4}}{C_1} + \frac{g_{m1}g_{m2}}{C_1C_2}} \quad (4.11)$$

$$A(s) = g_{m3} \quad (4.12)$$

Since $T(s)$ is the analogous resonator function of this oscillator, examining and comparing Equation 4.11 to Equation 4.3, Q and ω_o can be distilled from this and the result can be found to be Equations 4.13 and 4.14.

$$Q = \sqrt{\frac{g_{m1}g_{m2}C_2}{g_{m4}^2C_1}} \quad (4.13)$$

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (4.14)$$

As discussed before, if $T(s)$ and $A(s)$ are placed into the feedback function found in Equation 4.1 and the input is set to zero for the case of an oscillator, the characteristic equation results. For this system, the characteristic equation is then found to be Equation 4.15.

$$s^2 + s\frac{g_{m4} - g_{m3}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2} = 0 \quad (4.15)$$

The characteristic equation further yields the expression for b and is found in Equation 4.16. In addition, the characteristic equation also confirms the frequency of oscillation is the same as Equation 4.14. Again, b must be set to slightly larger than zero in order to induce oscillations.

$$b = \frac{g_{m4} - g_{m3}}{C_2} \quad (4.16)$$

It is clear that 4.13 and 4.14 are highly correlated. For a specified frequency, in order to increase Q while leaving ω_o the same, the only degree of freedom is to decrease g_{m4} . Because the selection of g_{m3} is independent of frequency or Q as it comes from $A(s)$, g_{m4} can be set relatively low and correspondingly g_{m3} can be easily scaled down in order that $g_{m4} \simeq g_{m3}$ (for the condition of $b \simeq 0$ to be set in order to minimize phase noise).

Based on providing a maximum Q , the circuit was then designed to produce a low transconductance for g_{m4} and g_{m3} . It then follows g_{m1} and g_{m2} were then set

to a higher transconductance in order to produce a frequency of around 2.4 GHz. As mentioned previously, g_m can be easily controlled through current mirrors. Thus a separate tuning voltage V_{tune} was devised to independently control the frequency by manipulating both g_{m1} and g_{m2} . The mismatch in output powers can easily be corrected with a variable gain amplifier at the output.

The $T(s)$ resonator contains g_m terms inherited from the OTA cell, whereas a typical LC tank has its terms inherited from the lumped LC components. Because of this, there are limits on how low or how high g_{m4} can be set.

Referring back to the overall schematic in Figure 4.7 a transfer function is found that relates v_{o1} to v_{o2} . This relationship is shown in Equation 4.17.

$$\frac{v_{o2}}{v_{o1}} = \frac{j\omega C_1}{g_{m1}} \quad (4.17)$$

Because there is no real component, then the phase in relation to each other is then found to be exactly 90° . Note that this holds regardless of the circuit conditions (according to our parasitic-less model) because it is purely imaginary.

4.2.3 Buffer Circuit

An oscillator system is very sensitive and any type of loading as it will change the system loop feedback equation. If a low impedance load is placed at the output, much of the current will be shunted away from the loop causing oscillations to cease. Because of this, it is required that this circuit contain buffers at the outputs in order that any load placed at the output will not affect the oscillator's oscillation conditions. In this circuit it was elected to place a source follower amplifier at both outputs. The source follower circuit is shown in Figure 4.8. The input of the buffer is the gate of the transistor M_1 , which acts like an open circuit. Because of this, there are minimal loading effects on the oscillator and the addition of the buffer will not

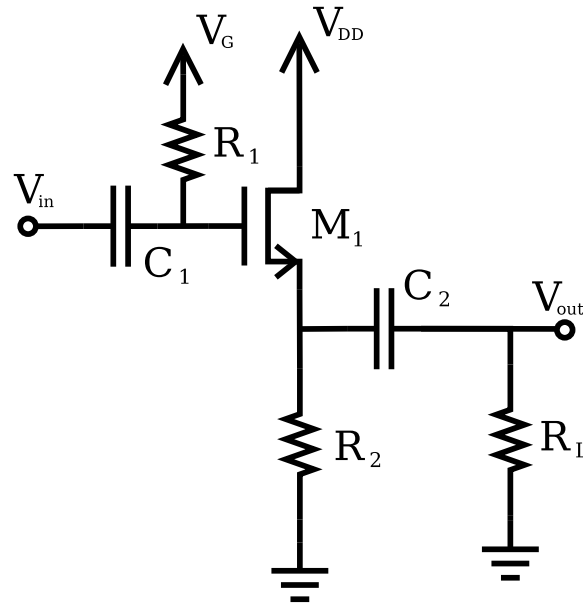
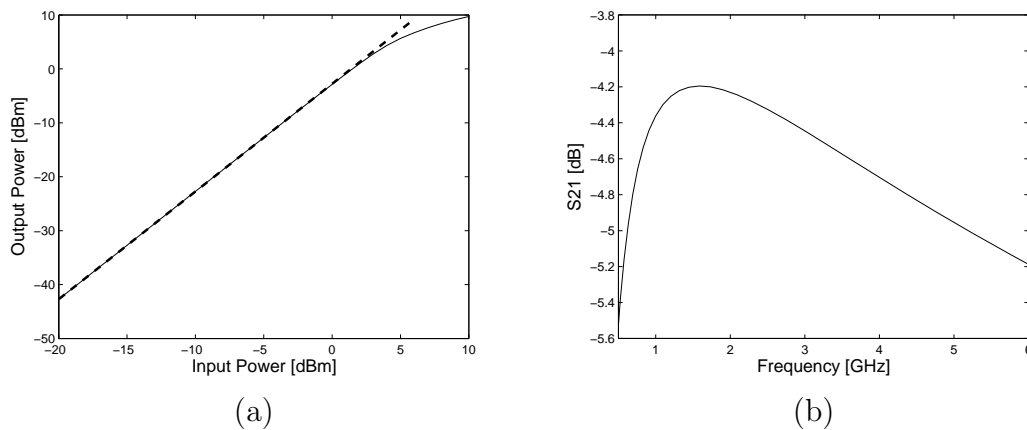
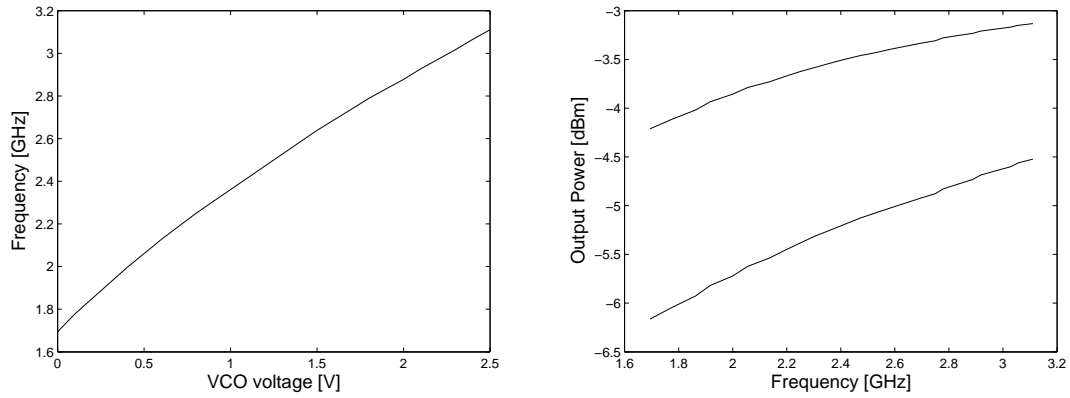


Figure 4.8: Schematic of buffer circuit for VCO

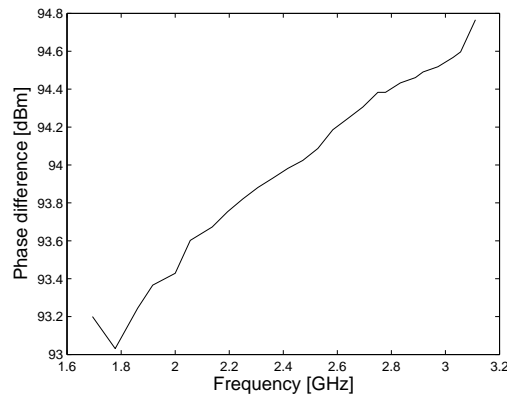
affect the oscillation conditions. It is known that the oscillator circuit produces up to $1.573 V_{pk-pk}$ for an open circuit. Therefore a buffer circuit that provides good linearity at high input voltage levels is required. Typical buffer circuits produce approximately -3 dB loss when connected to a low 50Ω load. However, because the input voltage is much higher than what is normally used, a specialized buffer that can handle high power was required. The high power handling of the buffer was offset by a reduction

Figure 4.9: Buffer circuit a) Input referred 1 dB compression point and b) S_{21}

in gain. The gain and input referred 1 dB compression point (P_{1dB}) were simulated in SpectreRF and are shown in Figure 4.9. The P_{1dB} is calculated to be 3.8 dBm and the peak gain is -4.2 dB.

(a) Frequency as V_{tune} is swept

(b) Output power levels over frequency range



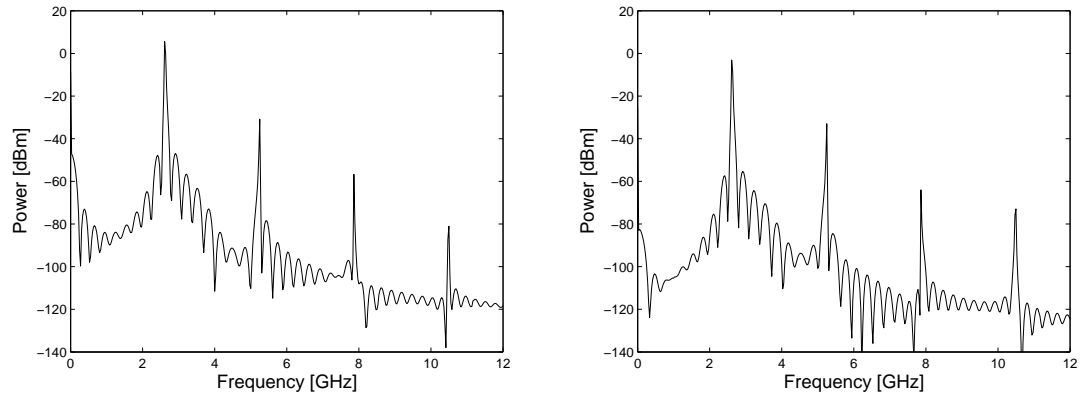
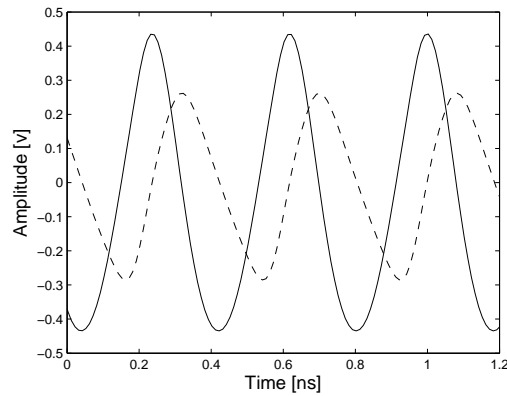
(c) Phase difference over frequency range

Figure 4.10: Various simulated parameters for VCO

4.2.4 Simulated Results

The final layout was simulated in SpectreRF and the results are depicted in Figure 4.10. The tuning range for this VCO is approximately 1.42 GHz if V_{tune} is swept

from 0 to 2.5 V. For the same sweep, it is seen that the phase stays at a consistent $\sim 94 \pm 1^\circ$. The higher than 90° phase as predicted in the equations is a result of the previously ignored parasitics in the transistors.

(a) Frequency spectrum of v_{o1} (b) Frequency spectrum of v_{o2} 

(c) Time domain simulations

Figure 4.11: Time domain and frequency spectrum of simulated data at 2.611 GHz

In order to maximize the frequency and Q factor, the tradeoff was that the output levels would not be the same. The results reflect this as v_{o2} is consistently 1.5 dB above v_{o1} . This can easily be fixed with the addition of a variable gain amplifier on

v_{o1} . A snapshot of the time domain output along with the frequency response at $V_{tune} = 1.8\text{ V}$ is shown in Figure 4.11.

4.3 Measured Results

To measure this device a Wentworth probe station was used along with two 40 GHz coplanar waveguide (CPW) ground signal ground (GSG) probe to measure the two quadrature outputs. For power, V_{SS} was connected to -1.8 V and V_{DD} to $+1.8\text{ V}$. V_{tune} was also connected to a voltage supply and swept across various voltages. In total four DC probes were used to connect this device. The probe layout is illustrated in Figure 4.12.

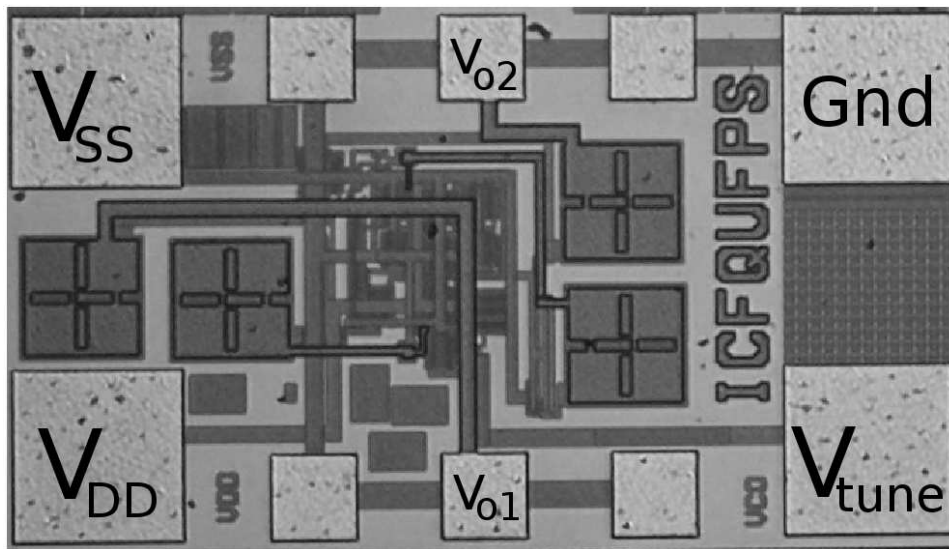


Figure 4.12: Micrograph of quadrature voltage controlled oscillator

The test setup is shown in Figure 4.13. A Tektronix DSA 8200 digital signal analyzer was used with the 80E06 digital sampling module to function as an oscilloscope. In addition to the two quadrature inputs, a trigger signal is needed. Consequently, one of the signals was split using a power divider. A splitter was placed on the other side in order to keep the setup symmetrical so that the attenuation caused by the

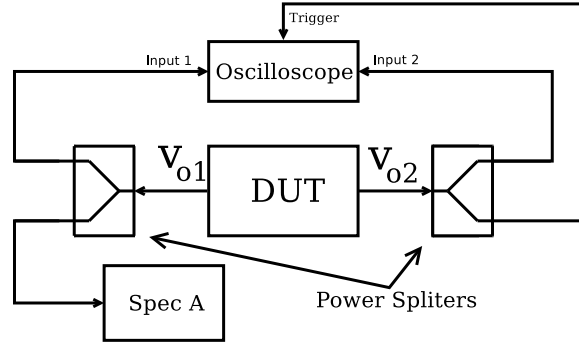
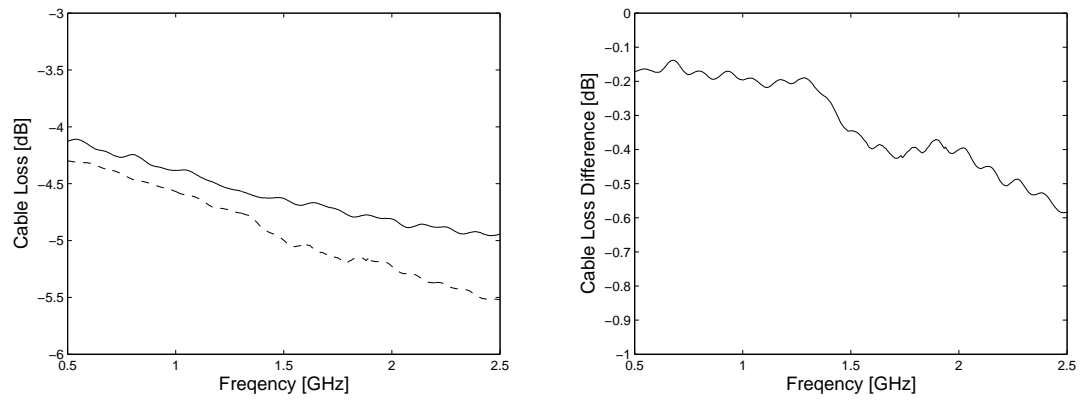


Figure 4.13: Test setup used to measure spectral and time domain outputs for VCO splitter and the cables are approximately the same. For this splitter, the second connection was connected to an Agilent E4446A spectrum analyzer in order to monitor frequency.

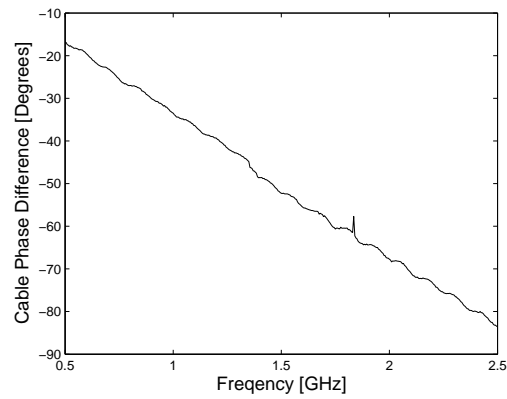
The time domain measurements when V_{tune} was then swept from 0 to 2 V were taken from the oscilloscope and signal processing was done in Matlab in order to extract the phase, magnitude and spectrum from the signal. Several chips were tested and the various results are represented as different symbols in the figure. When comparing the time domain signal power to the results from the spectrum analyzer, there was a systemic error of approximately 0.75 dB. This is most likely the result of a slight mis-calibration of either the spectrum analyzer or the oscilloscope, or both. The results of the oscilloscope were taken instead of the spectrum analyzer because a complete set of data for both outputs were available.

In order to measure the phase offset and the power loss of the cables and power splitter, the S-parameters of the setup were measured using an Agilent 8510C 50 GHz vector network analyzer. The results of the cable loss and phase offset are depicted in Figure 4.14. The following results have the cable loss and the phase offsets compensated. It is noted the large difference in the cable and phase offsets between the two outputs are attributed to the use of a slightly longer cable at one side compared to the other. Because these effects are compensated, this will not affect



(a) Cable loss of both paths

(b) Difference in loss



(c) Difference in phase

Figure 4.14: Cable loss and phase for the two paths to the oscilloscope

the overall experimental results.

Time Domain Results

The time domain results were taken from the oscilloscope and compensated for the phase loss of the cables. The results from this are plotted in Figure 4.15. Note that there is a slight amount of distortion in both of the outputs.

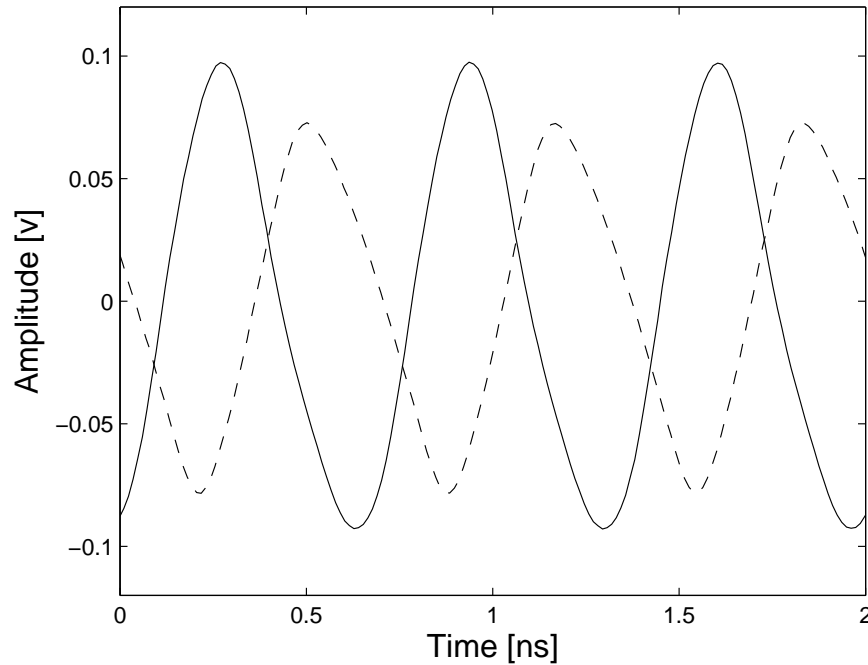


Figure 4.15: Time domain oscilloscope plot at 1.502 GHz where the solid line is v_{o2} and the dashed line is v_{o1}

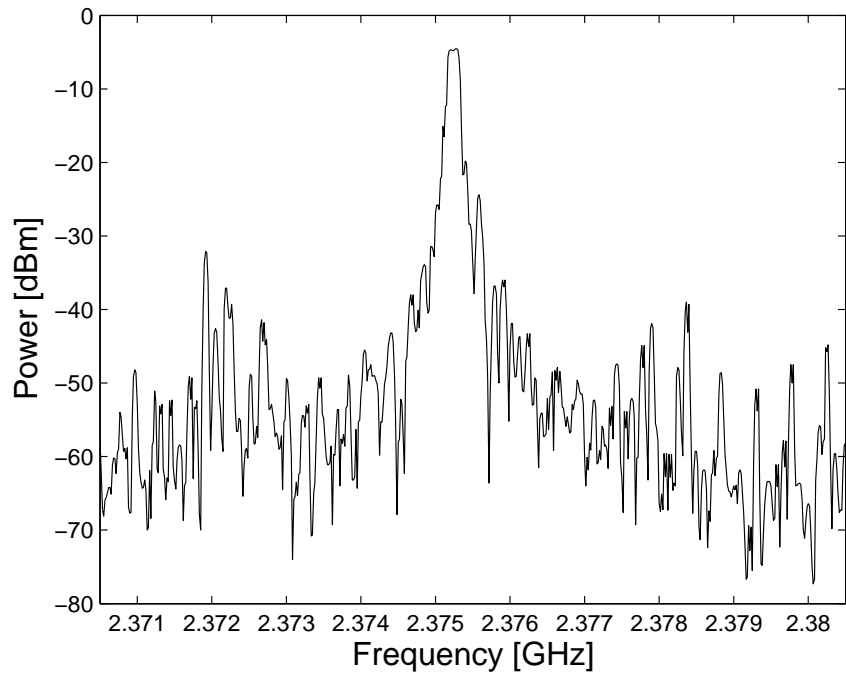
Frequency Results

The frequency results were taken using the spectrum analyzer instead of the oscilloscope because the results from the spectrum analyzer are more accurate. A snapshot of the frequency is shown in Figure 4.16. Note the different power levels corresponding to the different frequencies. When comparing these measured results to simulation, the center frequency does not match those of the simulation. The frequency is based

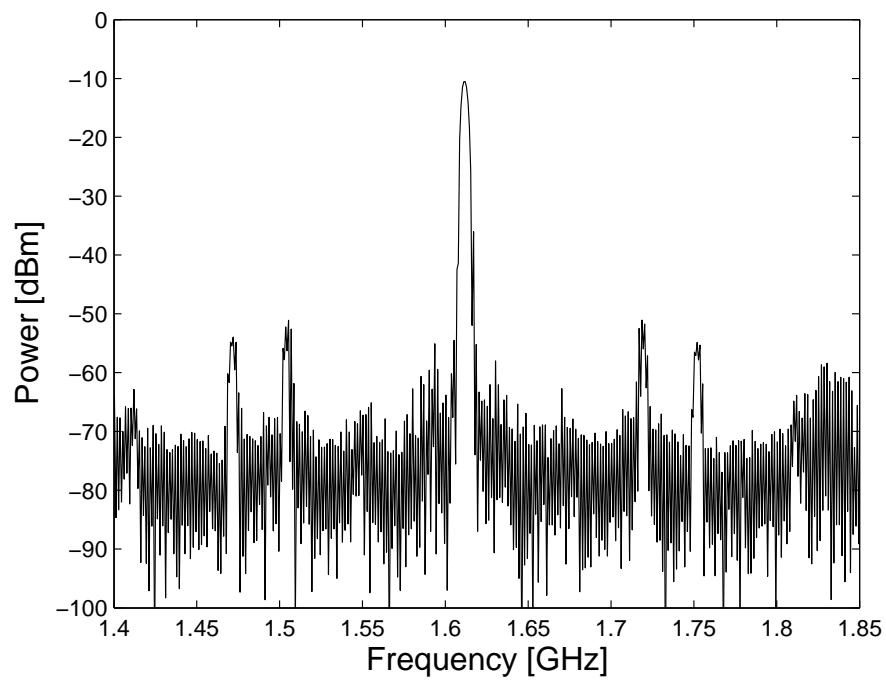
upon the transconductance and capacitor. It then can be concluded that since the specified capacitor was made to be very small, any small amount of unaccounted parasitic capacitance in parallel with C_1 or C_2 will severely affect the frequency of oscillation.

The results of frequency as the voltage was swept is depicted in Figure 4.17. As the voltage is swept, the frequency increases lineally, however at one point, the frequency jumps ~ 400 MHz. This can be attributed to stability issues within the system. As mentioned previously, changing g_{m1} and g_{m2} allows the changing of the oscillation frequency. However, doing so changes the loop equation and affects the stability conditions. As a result of this, at some threshold, the frequency jumps. Along with the obvious ~ 400 MHz jump, there is yet another jump at a lower frequency of ~ 40 MHz. Thus the device can be partitioned into three continuous different zones of operation. Zooming into each “zone”, we arrive at Figure 4.18.

From the beginning, the equations produced in Section 4.2.2 are based on the first order approximation for a model of an OTA. The actual model of the OTA is considerably more complicated (it is both non-linear and time variant). Thus the transfer function and the corresponding set of design equations only provide a very generalized result. In reality, instead of a second order system, the transfer function is more like: $T(s) = \frac{(s-z_1)(s-z_2)\dots(s-z_{m-1})(s-z_m)}{(s-p_1)(s-p_2)\dots(s-p_{n-1})(s-p_n)}$, which contains multiple zeros and poles. Consider an example of pole movement shown in Figure 4.19, if the oscillator tuning voltage is increased, then the original set of poles (that lie on the imaginary axis) move away from the origin (this corresponds to an increase in frequency). However additional unmodeled poles that exist on the S-plane also move. As one set of poles cross the axis, another set repositions itself at another location when the tuning voltage is changed. These additional movements are the reason for the unexpected instability which causes changes and jumps in frequency as exhibited in the experimental results.



(a) Spectrum at 2.37 GHz



(b) Spectrum at 1.62 GHz

Figure 4.16: Snapshots of measured spectrum at different points

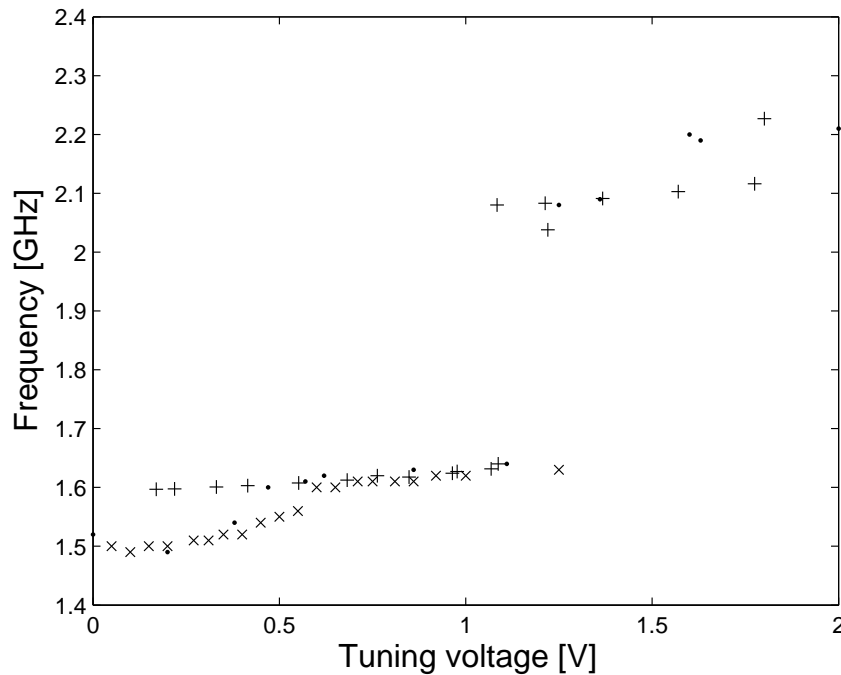
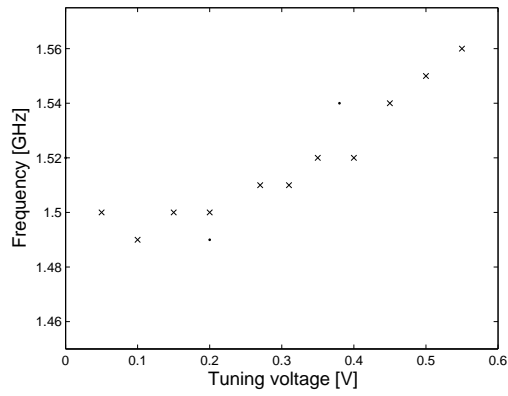


Figure 4.17: Measured VCO results

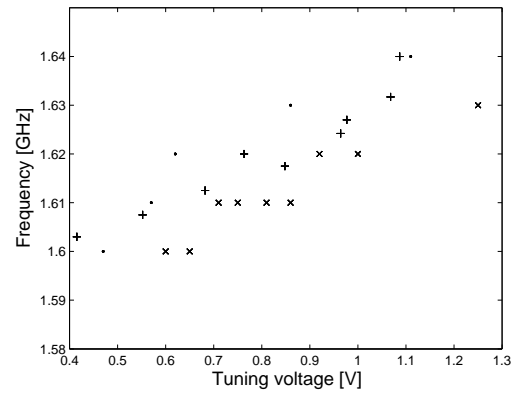
Power Level Results

As mentioned before, the power level outputs cannot be taken from both sides of the oscillator at the same time. As a result, the Fourier transform performed on the time domain measurements were used instead. It is recognized that these results are less accurate. It can be noted that while the overall power levels may not be accurate, the measured power levels between the two output signals are. Since the accuracy of the power level difference is a more important criteria in quadrature oscillators than the overall power output, the results from the time domain measurements were used. The reasoning behind this is because any signal can easily be amplified or attenuated to suit the systems specifications, however manipulating the difference in the two quadrature power levels proves to be much more difficult.

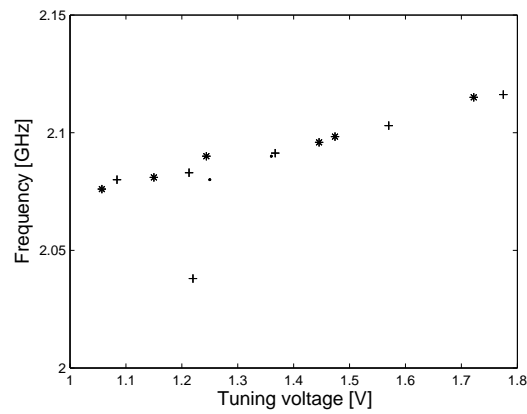
The results of the measurements are depicted below in Figure 4.20. The two quadrature outputs are at different power levels and are in line with the results obtains



(a)



(b)



(c)

Figure 4.18: Various sections of Figure 4.17 magnified

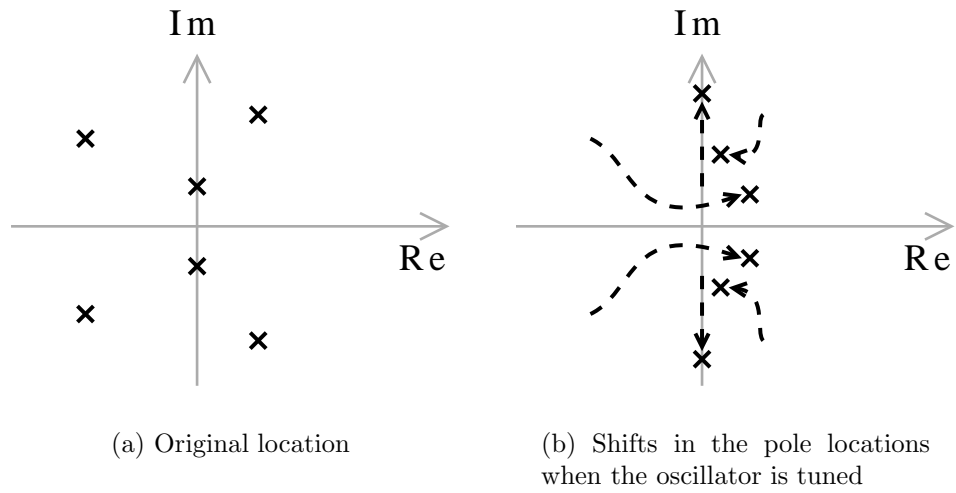


Figure 4.19: Example of the movements of multiple poles in the oscillator

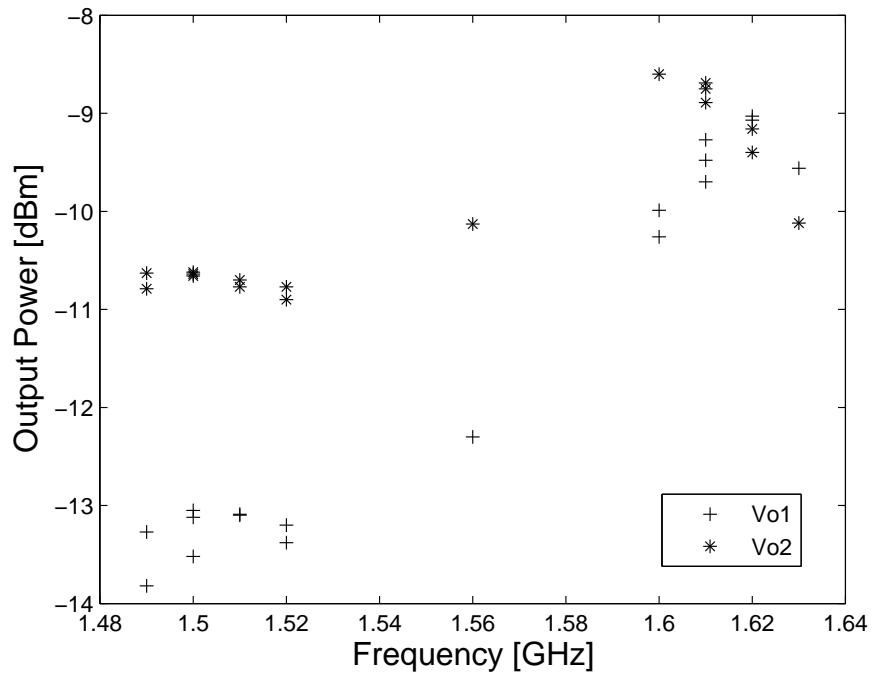


Figure 4.20: Measured output power levels

from simulation. However at higher frequencies, the two power levels converge. This does not match with the simulated results and it can only be inferred that this is the result of stabilization issued mentioned earlier. These results can be seen in Figure 4.21.

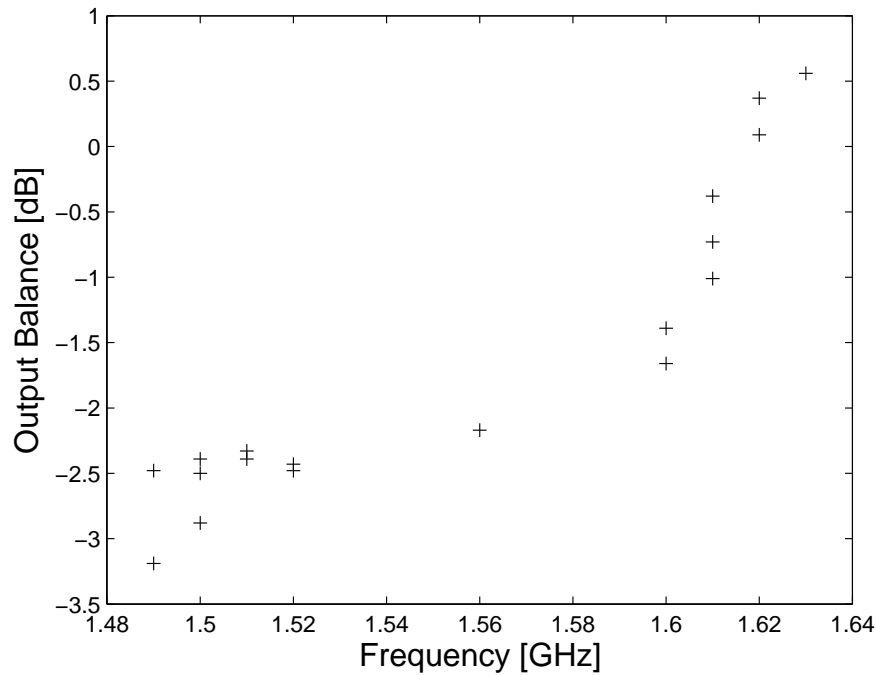


Figure 4.21: Measured output power balance

Quadrature Results

The phase results were taken from the Fourier transform algorithm in Matlab mentioned previously. The phase difference is then plotted and depicted in Figure 4.22. It was noted earlier that the quadrature output predicted is a result of the transfer function without any parasitics. However the parasitics that were included in the SpectreRF simulations predicted a 94° difference between outputs. This does not match up with the measured results. This mismatch can be attributed to wire resistances or inductances that are not included in the models. It also follows that there

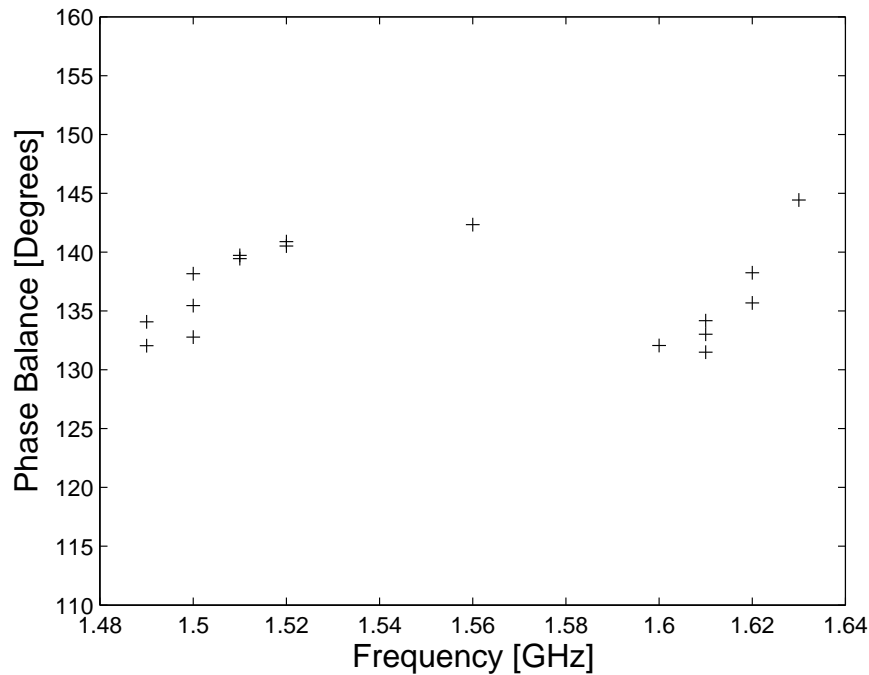


Figure 4.22: Measured output phase balance

could be additional parasitics that are not predicted in the SpectreRF models.

Phase Noise Results

Conventional means of measuring phase noise poses a problem with low Q inductorless oscillators. Because the oscillation frequency is entirely dependent on the synthetic LC tank, the frequency of oscillation is very sensitive to variations in the environment. Noise from the power supply and the environment in addition to other elements will cause the oscillation conditions to be altered. Although this frequency fluctuation is only on the order of a few kilohertz, this poses a problem for measuring phase noise.

The phase noise is determined at frequency offsets at various points. However because of the frequency fluctuations, offsets close to to the carrier cannot be accurately gauged. In order to circumvent this problem,[47] describes a method in which a stable oscillator is injected into the system to stabilize the oscillation.

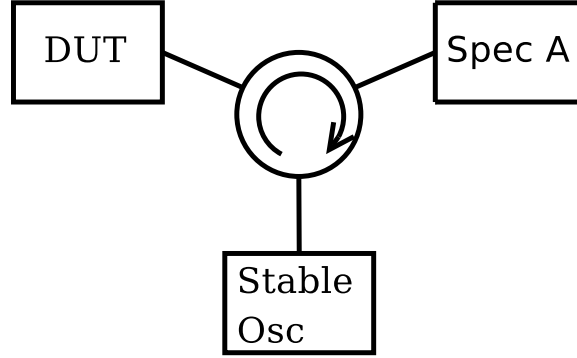
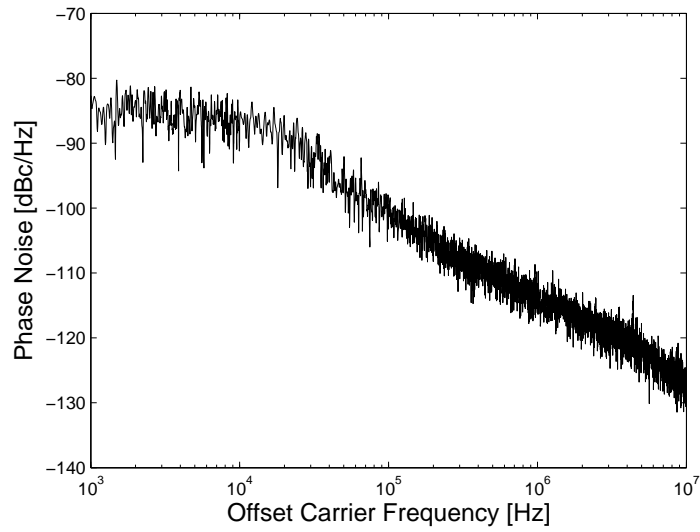


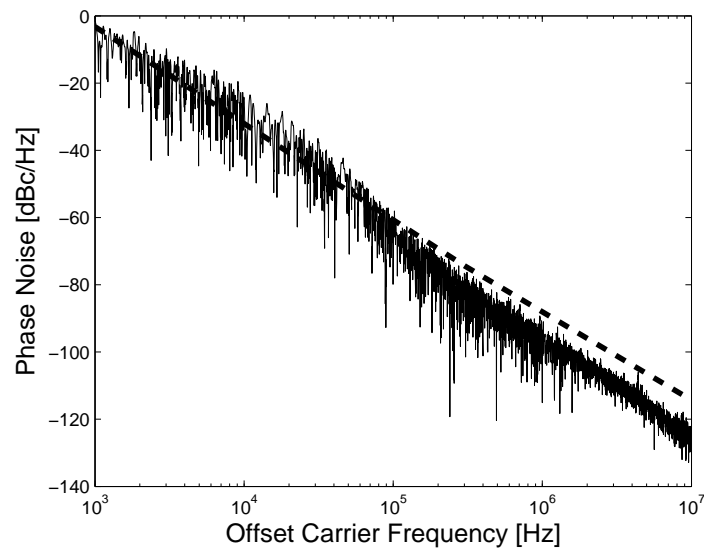
Figure 4.23: Test setup for injection locked stabilization phase noise measurement

A modified test setup depicted in Figure 4.23 was used to inject the stable oscillator signal into the device under test (DUT). An Anritsu MG3694A signal generator was used for the stable generator with a power level of -20 dBm. Although the output of the oscillator contains a buffer circuit, small fraction of the injected power will still leak though via C_{gs} into the feedback loop, thus locking the oscillator signal onto the stabilized one. A circulator was used in order to ensure the injection went from the Anritsu signal generator to the oscillator but not the other way around so that the generator would not be damaged. Equation 4.18 was the original equation from [47]. If Φ_{detune} is equal to zero (as in the case of a locked signal) then this equation can be simplified and rearranged to determine the uncoupled free running oscillator's phase noise $\langle \delta\phi_{free}^2(\Omega) \rangle$.

The final result is shown in Equation 4.19. The locking bandwidth is determined experimentally is defined as the range in which the free running oscillator is able to lock onto the stabilized signal and is shown as $\Delta\omega$. $\langle \delta\phi_{lock}^2 \rangle$ is the original phase noise of the setup in Figure 4.23, Ω is the frequency offset from the carrier, and $\langle \delta\phi_{inj}^2(\Omega) \rangle$



(a) Phase noise of locked oscillator



(b) Extracted phase noise along with simulated results from SpectreRF depicted as a dashed line

Figure 4.24: Phase noise of oscillator

is the stable oscillator's stand alone phase noise.

$$\langle \delta\phi_{lock}^2(\Omega) \rangle = \frac{4\Omega^2 \langle \delta\phi_{free}^2(\Omega) \rangle + \Delta\varpi^2 \cos^2(\Phi_{detune}) \langle \delta\phi_{inj}^2(\Omega) \rangle}{4\Omega^2 + \Delta\varpi^2 \cos^2(\Phi_{detune})} \quad (4.18)$$

$$\langle \delta\phi_{free}^2(\Omega) \rangle = \left[4\Omega^2 \langle \delta\phi_{lock}^2(\Omega) \rangle + \langle \varpi\phi_{lock}^2(\Omega) \rangle \Delta\varpi^2 - \Delta\varpi^2 \langle \delta\phi_{inj}^2(\Omega) \rangle \right] \frac{1}{4\Omega^2} \quad (4.19)$$

The phase noise performance was measured and the aforementioned algorithm was applied. The original measured locked phase noise is found in Figure 4.24a). The decoupled phase noise was plotted along with the simulated results from SpectreRF is shown in Figure 4.24b). It is seen that the two results are very similar with the phase noise from the oscillator performing marginally better. This is most likely due to inaccurate noise models within the simulator.

At 1 MHz and 10 MHz offset the phase noise were determined to be -97.66 dBc/Hz and -125.4 dBc/Hz respectively. As discussed before, this is noisier than most oscillators because of the low Q, however this result is in line with other inductorless oscillators in literature.

4.4 Conclusions

In this chapter an inductorless quadrature voltage controlled oscillator was presented. The oscillator is composed of a synthetic resonator tank using OTA amplifiers. The result is an oscillator with a simulated bandwidth of 1.42 GHz. However because of stability issues, the actual measured bandwidth of 100 MHz is considerably less. The phase noise was determined to be -97.66 dBc/Hz at 10 MHz. This is on par with other inductorless oscillators found in literature [33][48][49][50]. The simulated phase of $\sim 94^\circ$ was not achieved when measured and was found to be 135° . The power level that was produced was significantly below the simulated results. It is then concluded that the cumulation of all these results are indicative of incorrect transconductances being used in the system. This incorrect transconductances could either be a result of

incorrect modeling within the OTA or incorrect currents being fed into the OTA. Thus future work will correspond to more accurate modeling of these transconductances. In addition separate and more strict control of each of the four transconductances will help to mitigate any instability issues. By being able to control all the elements of the system, we have the ability to control the frequency, Q factor and power output. Nevertheless this circuit demonstrates that an artificial OTA resonator can be used in an oscillator system. The result is an oscillator with a limited tuning bandwidth that can be created and used in a PLL system.

Chapter 5

Wideband Feedback Quadrature Generator

5.1 Introduction

By far the most common way to generate a quadrature signal in MMIC (Monolithic microwave integrated circuit) is to use a Resistor-capacitor capacitor-resistor (RC-CR) network [24]. While it is quite easy to generate a 90° phase, providing a constant amplitude balance between the outputs proves to be quite difficult. In the case of the RC-CR circuit, the system can only provide a perfect amplitude balance at one specific frequency. In addition, resistor tolerances in MMIC technology are known to be very loose. A design calling for a specific resistor value can sometimes result in a 20% difference in the final manufactured value. Assuming that the capacitor is manufactured exactly as modeled, an incorrect resistor value with a 20% tolerance can result in a circuit designed for 2.4 GHz to function at 2 GHz.

In this chapter a circuit is introduced that uses a feedback network to eliminate this problem. A functional block diagram followed by a more complete one depicted every individual stage underneath is depicted in Figure 5.1. By using a combination of a simple RC-CR network (Figure 5.1a)) to produce the 90° phase shift and variable

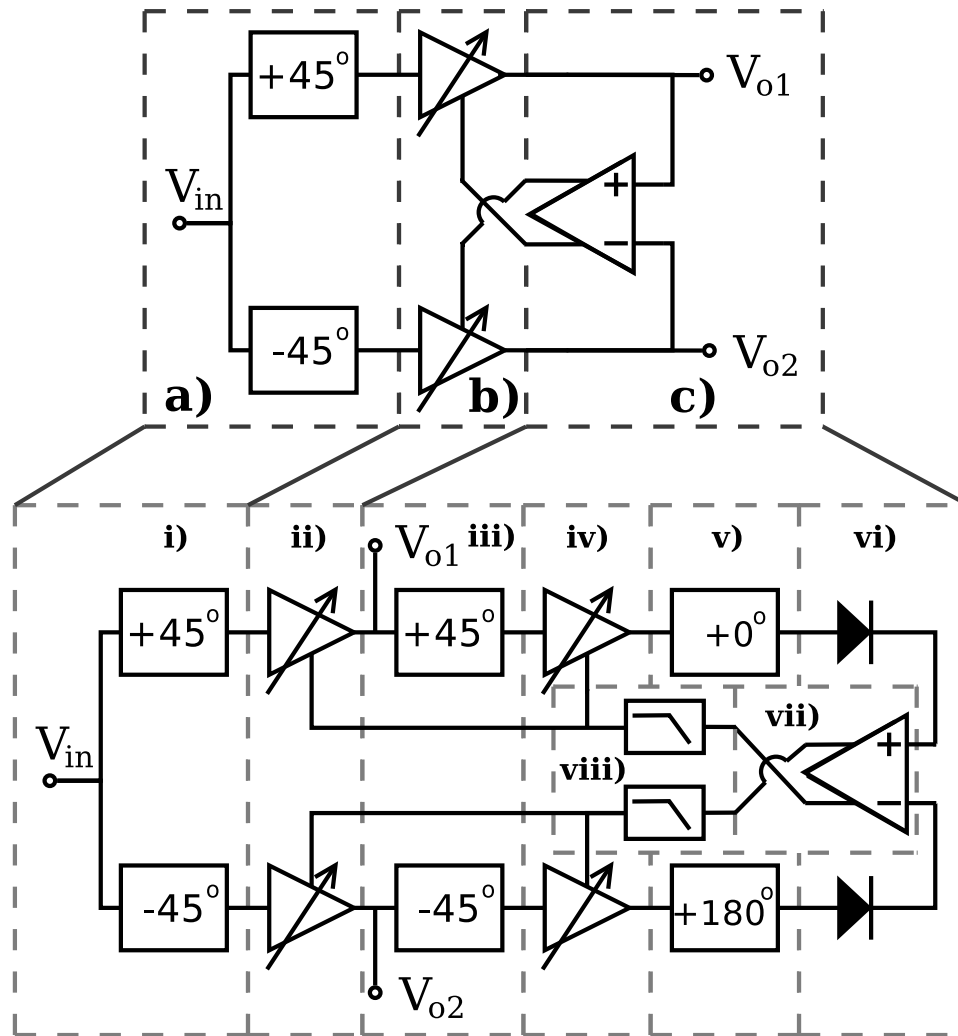


Figure 5.1: Block diagram of feedback quadrature generator

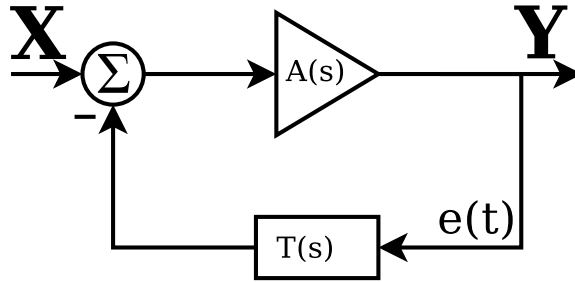


Figure 5.2: Generalized feedback model

gain amplifiers (Figure 5.1b)) in a feedback loop, the bandwidth of the network can be expanded significantly. The amount of gain that needs to be compensated is determined with an amplitude detector and comparator circuit (Figure 5.1c)).

5.2 Control System Analysis

Negative feedback systems are used in many fields to compensate for disturbances and changes that occur in a system. In this instance, a negative feedback system is used to automatically detect an amplitude imbalance in the quadrature generator and compensate accordingly using variable gain amplifiers. For any given feedback system, the general form was introduced in Section 4.1.1. The same model discussed previously is found in Figure 5.2. This model depicts a system with input X and output Y . The generalized feedback equation is then found to be Equation 5.1.

$$\frac{X(s)}{Y(s)} = \frac{A(s)}{1 + A(s)T(s)} \quad (5.1)$$

5.2.1 Modeling the Quadrature Generator

The basic conceptual block diagram is found in Figure 5.3. The details of the circuitry will be discussed in a later section, however a minimalized system level block diagram

will be discussed here to introduce the control theory from a systems perspective. In order to provide a concise circuit, instead of considering the whole system, only the control part of the circuit is explored. Therefore a simplification from a control systems perspective is to examine this circuit as a simple situation in which two input signals (V_{in1} and V_{in2}) are of unequal magnitude and a feedback system is used to compensate the mismatch. Therefore consider the following feedback system found in Figure 5.3. If there are two input signals V_{in1} and V_{in2} traveling into the system, it is desired that the outputs V_{o1} and V_{o2} be of the same amplitude. The amplitudes are modified using a feedback path that contains two variable gain amplifiers. By comparing the two signals at the output, an appropriate amount of tuning can be applied to the variable gain amplifiers through the feedback path.

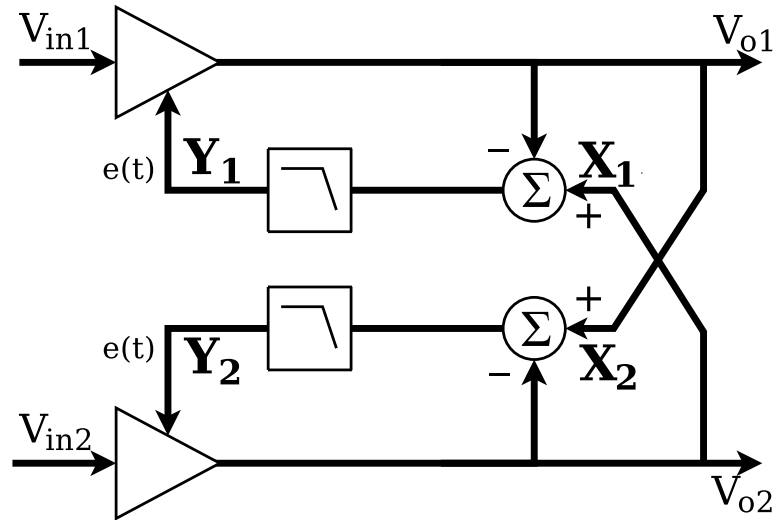


Figure 5.3: Control system level block diagram of the feedback quadrature generator

In the most general system, the reference signal is the signal in which the system strives to match. In this case, the reference signal is labeled as \mathbf{X} . The output error signal $e(t)$ feeds back into the system in order to compensate the original signal.

A classical example of a similar feedback system is a phase locked loop (PLL) and is presented here in order to gain some insight and to draw parallels that will make

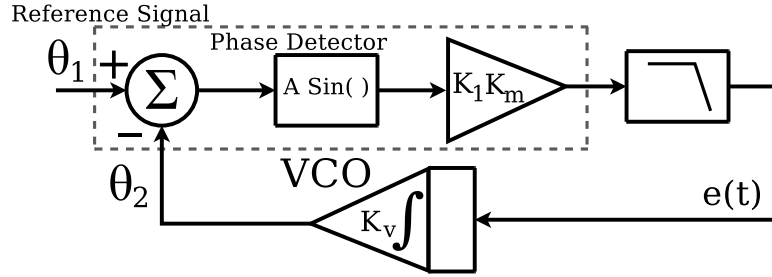


Figure 5.4: Block diagram description of a classical phase locked loop [51]

it easier to model our system. The difference between this system and that of a PLL is that instead of trying to match the phase, this circuit will attempt to match the amplitude. Thus the approach to model this system is to compare this system with that of a PLL. The classical PLL circuit is depicted in Figure 5.4.

In this PLL system, a reference signal θ_1 is compared with the actual signal θ_2 through the phase detector. If there is a difference in the phase of the signals, then an error signal $e(t)$ will be produced to adjust the VCO's operating frequency. There are three essential elements present in any PLL: Phase detector, Low pass loop filter and VCO. In addition to this, there are three crucial signals present: Input reference signal (θ_1), error signal ($e(t)$) and output feedback compensated signal (θ_2).

If the PLL system is compared to our system depicted in Figure 5.3, it is possible to draw parallels. Thus there are also three similar essential elements: Amplitude comparator, Low pass loop filter and voltage controlled amplifier. In addition there are also three sets of signals: Input reference signal (\mathbf{X}_1 and \mathbf{X}_2), error signal ($e_1(t)$ and $e_2(t)$), and output feedback compensated signal (v_{o1} and v_{o2}). However unlike the reference signal that is given in a PLL system, the reference signal comes from another branch that is being compensated at the same time. In our system, there are two feedback systems working in parallel providing two different reference signals for each other. As one feedback system adjusts to match the other branch, the other branch is also compensating and adjusting to match. The basic principles of the feedback

system can still be applied in this case, however in order to enable a more concise analysis, only one branch will be analyzed. It is assumed in this analysis that the reference signal (\mathbf{X}) from the other branch will be constant. In reality both reference signals will be constantly changing. In fact, because they are changing to match each other, the time required for the system to reach steady state will be significantly reduced.

While the assumption of a constant reference is simplistic, modeling both branches together proves to be needlessly complicated. Many of the values and functions of the system are not exactly known or accurately modeled, thus the addition of a more complex model does not add much more to the understanding of the system. The approach to rectify this issue is to produce a simplistic model and run simulations using SpectreRF based on this model. Knowing the model derived here will aid to tune the final system in order to produce the minimum settling time. In addition, this model is crucial to understanding how to avoid the case of an unstable system in which the system never settles.

The analysis of this feedback system begins with the separation of both branches. In addition, the voltage controlled oscillator will be rewritten to now compose of two separate components. Finally, an analog comparator unit that was previously represented with a simple subtractor block will now compose of additional components to provide a more accurate picture. The analog comparator was chosen to be modeled by two components: $K_{AC} \int$ and $F(s)$. The $K_{AC} \int$ represents the integrator function within the comparator circuit while the $F(s)$ term represents an unknown transfer function. In order to provide a first order analysis, simplifications have been made and is represented here as an unknown transfer function $F(s)$. The variable gain amplifier consists of two blocks: A multiplier and an integrator. Figure 5.5 reflects the changes and additions to the block diagram.

Furthermore, in order to aid in analysis, the block diagram is rotated and put

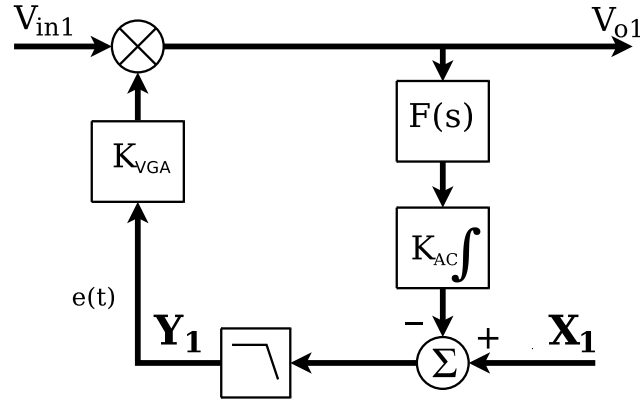


Figure 5.5: Detailed block diagram of the feedback quadrature generator

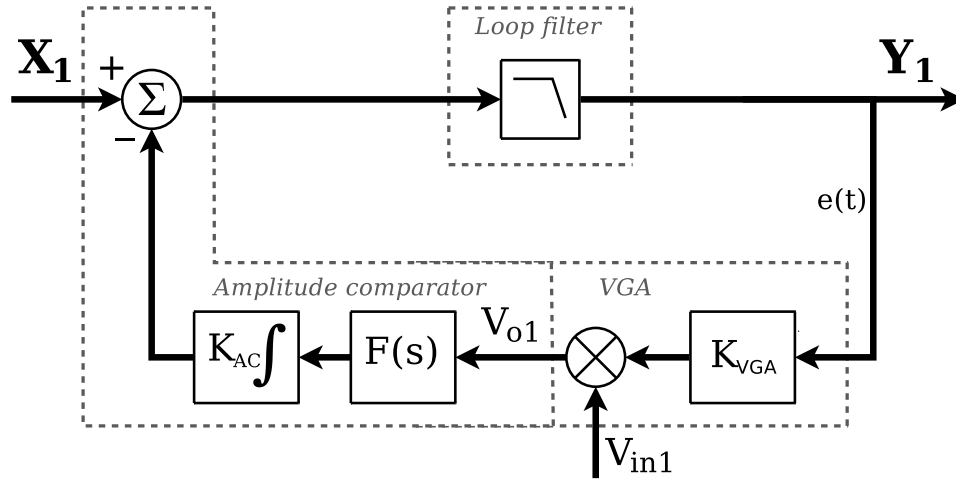


Figure 5.6: Rearranged block diagram of feedback quadrature generator

into the more typical feedback model form. The final diagram found in Figure 5.6 has been changed accordingly. This diagram now makes it very clear where the feedback path is occurring as well as clearly defining the three crucial components mentioned previously. The transfer function of the circuit is now extracted from the block diagram and is shown in Equation 5.2.

$$\frac{Y_1}{X_2} = \frac{\frac{1}{1+RCs}}{1 + \frac{1}{1+RCs} \frac{1}{s} K_{AC} K_{VGA} F(s)} \quad (5.2)$$

5.2.2 RC-CR Network

The generic RC-CR network is depicted in Figure 5.7. The transfer function of an RC and CR network can be shown to be Equations 5.3 and 5.4 respectively.

$$H_{RC}(\omega) = \frac{1}{j\omega RC + 1} \quad (5.3)$$

$$H_{CR}(\omega) = \frac{j\omega RC}{1 + j\omega RC} \quad (5.4)$$

Their phase and magnitude can then be shown to be Equations 5.5, 5.6, 5.7 and 5.8.

$$\angle H_{RC}(\omega) = -\tan^{-1}\omega RC \quad (5.5)$$

$$\angle H_{CR}(\omega) = \tan^{-1}\frac{1}{\omega RC} \quad (5.6)$$

$$|H_{RC}(\omega)| = \frac{\sqrt{1 + (\omega RC)^2}}{1 + (\omega RC)^2} \quad (5.7)$$

$$|H_{CR}(\omega)| = \frac{\sqrt{(\omega RC)^2 + (\omega RC)^4}}{1 + (\omega RC)^2} \quad (5.8)$$

The phase of each network can then be equated through the identity found in Equation 5.9 and when substituted becomes Equation 5.10. This shows that for any frequency, as long as the resistance and capacitance for each network is the same, there will always be a 90° phase between the two branches.

$$\frac{\pi}{2} = \tan^{-1}\frac{1}{x} + \tan^{-1}x \quad (5.9)$$

$$\frac{\pi}{2} = \tan^{-1}\frac{1}{\omega RC} - \tan^{-1}\omega RC \quad (5.10)$$

If the two magnitudes are equated, then Equation 5.11 shows the condition in which the two magnitudes are equal.

$$\omega = \frac{1}{RC} \quad (5.11)$$

It is determined that while the phase is constant across the whole bandwidth, the

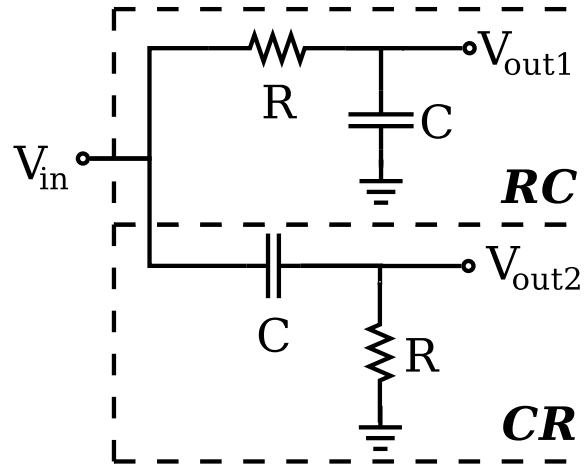


Figure 5.7: Schematic of RC-CR network

condition in which both magnitudes are equal applies to only one frequency.

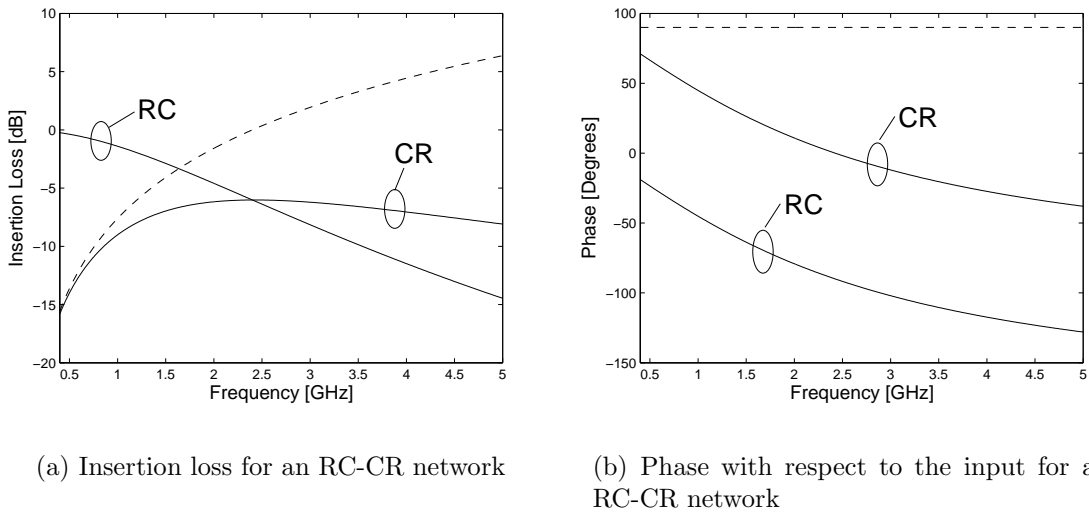


Figure 5.8: Simulated results for both RC and CR networks of Magnitude and Phase where the dashed line is the difference

For this circuit, the center frequency was chosen to be around 2.4 GHz. The RC-CR network was simulated in ADS and the results for the magnitude and phase are shown in Figure 5.8. The mathematical results are validated in simulation and the magnitudes are shown to be equal at only one point while the phase remains at a consistent 90° .

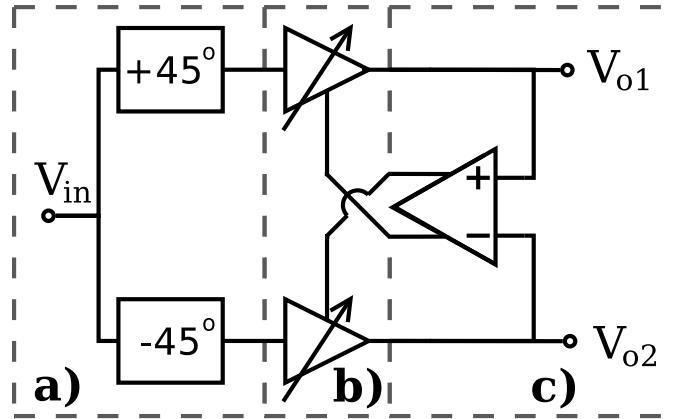


Figure 5.9: Simplified block diagram of feedback quadrature generator

The circuit introduced in this chapter uses this basic RC-CR circuit to produce the 90° and then applying a combination of a feedback loop and a VGA to adjust for the amplitude imbalance.

5.3 Circuit Description

The simplified block diagram for this design is shown in Figure 5.9. A 90° RC-CR phase shifter is implemented followed by the use of a VGA. A comparator at the output is then used to determine their amplitude difference. The result is then used to adjust the VGA and equalize the output's amplitudes. This block diagram is slightly different from the one that was introduced previously in Figure 5.3 for the control system analysis. The previous block diagram was framed in order to ease the analysis of deriving the feedback equations and as a result some blocks were omitted (such as the RC-CR phase shifters). The block diagram depicted here is put in terms of a circuit perspective and thus certain details are either described differently or substituted in. The circuit is divided into three functional circuit blocks: a)RC-CR, b)VGA and c)Comparator feedback network.

5.3.1 Variable gain amplifier

There are several metrics which the VGA must meet. A large tuning range is required as the larger the tuning range, the larger the amplitude it can correct. The larger the amplitude it can correct, the larger the frequency bandwidth of the resulting circuit. It is acceptable for the VGA to produce a phase shift between the output and the input as the same VGA is used in both the v_{o1} and v_{o2} branches. However if the phase changes in relation to the tuning voltage, the result is that the amplitude feedback system will no longer produce outputs that are 90° apart. Therefore a VGA needs to be found that produces no phase change throughout its tuning range. There were some VGAs that were explored which produced different phase shifts depending on the applied control voltage, but only the common source type amplifier that was controlled through varying the drain current provided a stable phase in relation to the varying gain. The schematic of the circuit is shown in Figure 5.10.

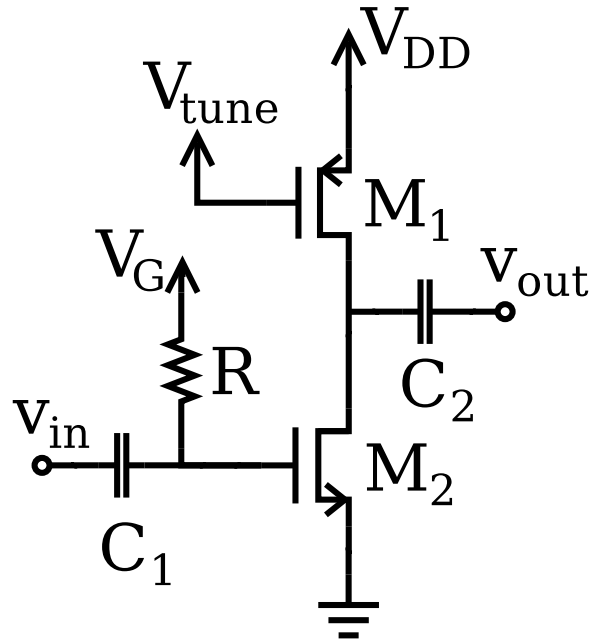


Figure 5.10: Schematic of variable gain amplifier

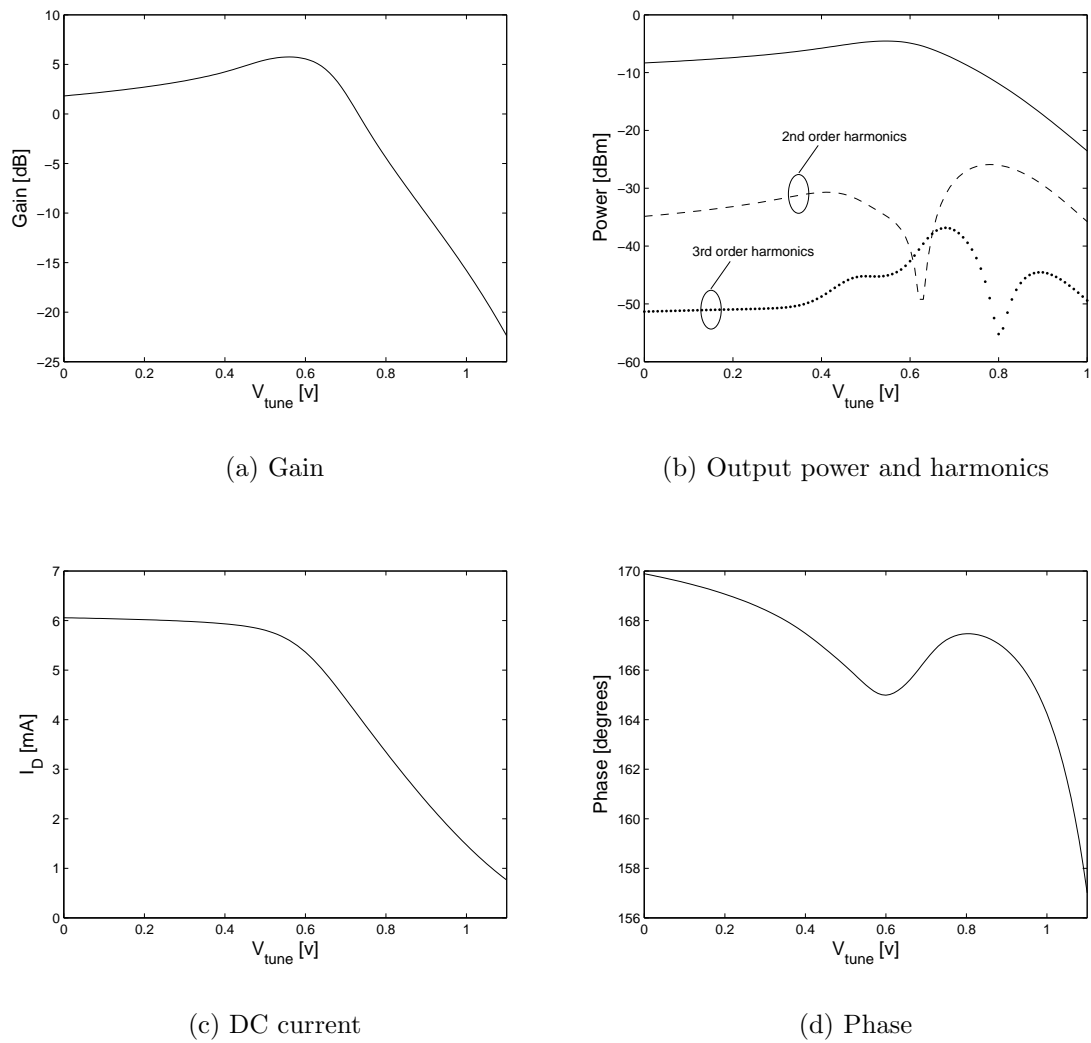


Figure 5.11: Various parameters for variable gain amplifier at 2 GHz

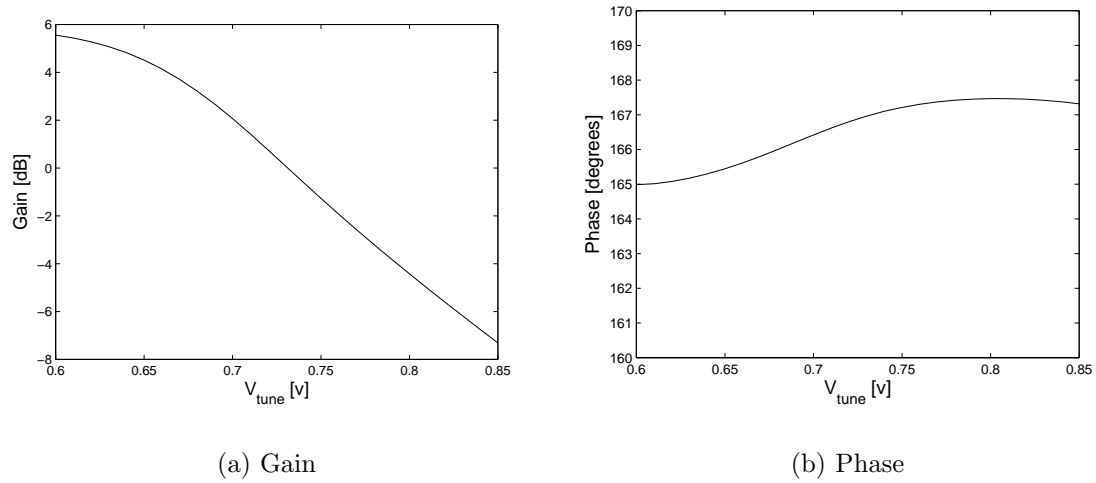


Figure 5.12: Gain and phase of variable gain amplifier for the specified area of operation at 2 GHz

The circuit is composed of the main transistor M_1 in common source type configuration. The capacitors C_1 , and C_2 are used as DC blocks and R is used as an RF choke. These components are assumed to be sufficiently large and therefore can be ignored. The gain is then controlled through another transistor M_2 . Because M_2 is in saturation, the DC current I_D can easily be controlled by the gate voltage V_{tune} . The amplifier was then simulated in ADS at 2 GHz (2 GHz was selected because it will be approximately the midpoint of the operating bandwidth) and the results are depicted in Figure 5.11. The dashed and dotted lines in Figure 5.11b) are the second and third harmonics respectively. It would be ideal to avoid the the region of operation where there is more distortion (> 0.6 V), however V_{tune} provides the greatest rate of change when operated in this zone and this slight distortion will have to be a compromise.

The selected area of operation for V_{tune} to be operated at was from 0.6 to 0.85 V. In this zone, the gain varies from 5.6 to -6.7 dB while the phase stay constant and only varies $\pm 1.25^\circ$. A zoomed in view of just this area of operation for gain and phase are shown in Figure 5.12. This device will be operated at a nominal voltage of ~ 0.73 V, producing a gain of about 0 dB. From there the voltage will be varied up

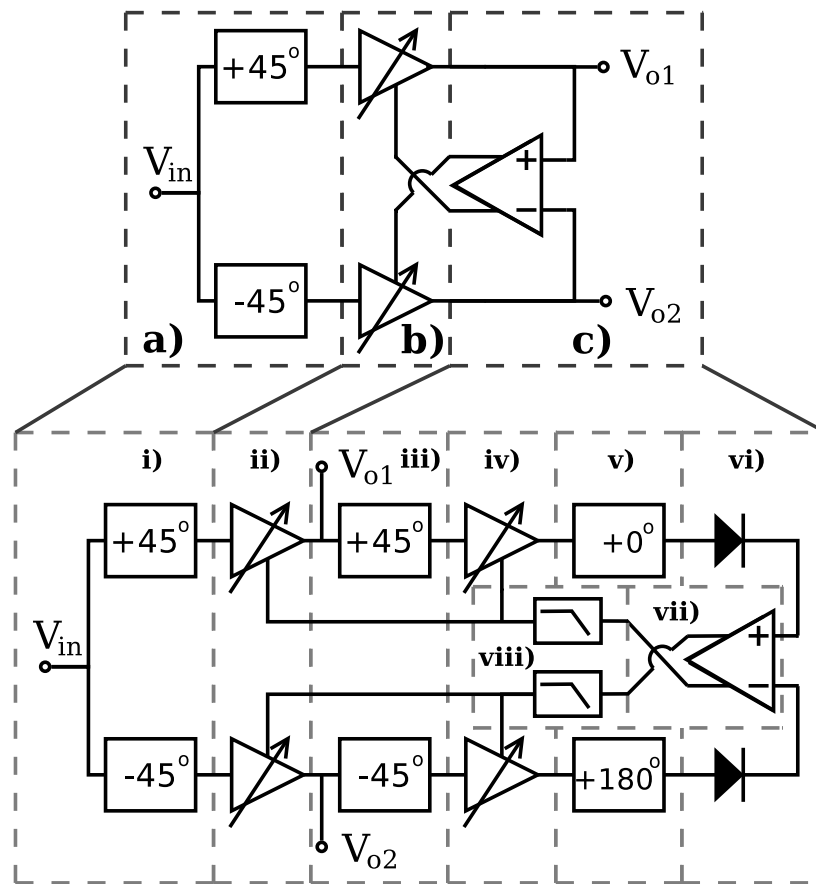
and down from this operating point to produce the varying gain.

5.3.2 Amplitude Detector and Comparator Feedback

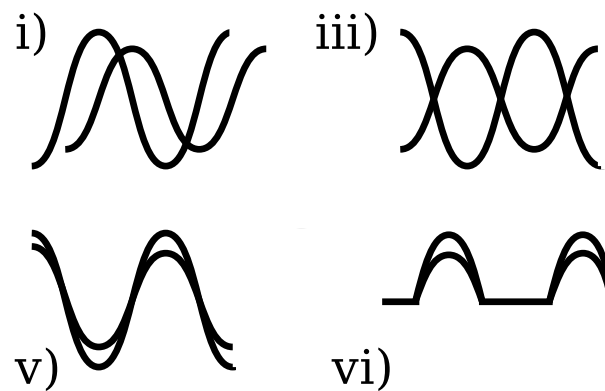
When the signals exit the variable gain amplifier, they are 90° apart. Figure 5.13a) depicts the stages that are explained next. The original simplistic block diagram is placed above this figure and the equivalent stages from each diagram are equated. Because the comparator that is used is essentially a subtractor unit, subtracting two voltages that are 90° apart does not produce any significant results. Thus another 90° RC-CR phase shifter is employed to shift the signals yet another 90° apart (Figure 5.13 iii)). The signals are again passed through another VGA (Figure 5.13 iv)) which will compensate for the amplitude imbalance caused by the previous RC-CR network. The signals are now 180° from each other. They are then passed through a differential pair (Figure 5.13 v)). This stage will move the phase back to 0° from one another. It may seem logical at this point to compare the two signals, however, if the two different amplitude signals are subtracted from each other, another sinusoid will result. Thus at this point, a rectifier circuit (Figure 5.13 vi)) will need to be employed to remove the negative half of the signal. Once this has taken place, the signal can now be subtracted from each other. This process is done using another differential amplifier (Figure 5.13 vii)). A low pass filter (Figure 5.13 viii)) that also functions as the loop filter is then used to smooth out the resulting wave to then produce a DC signal. This DC signal is then fed into the VGA to complete the feedback loop.

Differential Pair and OTA

For Figure 5.13 v), a circuit is required to produce a 180° phase. The use of a simple common source amplifier configuration was not used because the phase is not always exactly 180° between the input and the output as discussed in Chapter 3. In addition another circuit would be needed to ensure that any gain/loss in the v_{o1} half of the



(a) Block diagram



(b) Associated sinusoids at various points

Figure 5.13: Detailed block diagram of circuit

circuit would be reciprocated in the v_{o2} branch (where the phase is supposed to stay at 0°). While this can be done, it would be very difficult to keep both the v_{o1} and v_{o2} branch's phase and amplitude balanced across a very wide band. The use of the same circuit in both branches is thus considered ideal. For the same OTA used in Chapter 4 depicted in Figure 5.14a), if one input (v_{in+}) is grounded while the other input (v_{in-}) is excited, and the output is taken from only (i_{out+}), then the phase will be 180° . If the reverse is done (v_{in+} excited while v_{in-} is grounded and the output taken out of i_{out+}) then the phase will be 0° . However this is only the ideal case, in reality because of the different loading effects of the active loading transistors M_3 and M_4 , the circuit will not give the proper phase.

To remove the mismatch in the output impedance, the use of an alternate configuration is needed. Eliminating the active loading and replacing this with a pair of resistors will restore the symmetry between both sides of the differential pair. This new circuit is shown in Figure 5.14b). The output impedance at the drain of M_1 is just R , while the output impedance at the drain of M_2 is $R \parallel C_{gs} \parallel C_{gd}$ (C_{gs} and C_{gd} are from the next stage). As discussed before in 3.3.2, the input impedance at the gate of a transistor is considered to be sufficiently large that it will not significantly affect the results. Because of this, the two sides M_1 and M_2 can be considered symmetrical and the outputs should provide a 180° phase.

This alternate circuit is tested using the ADS circuit simulator and the results are given in Figure 5.15. As expected, the result of using resistors instead of active loading is that the resulting gain will be theoretically -3 dB rather than 0 dB. In the ADS simulation which includes parasitics, this closely matches the ideal model and results in a loss of approximately -3.7 dB. The phase stays close to 180° , however starts to drift lower and at 8 GHz the phase is 175° . This level of drift is considered acceptable. There is a slight imbalance in the gain, however this is caused by the 50Ω S-parameter load which increases the output impedance. This effect will disappear

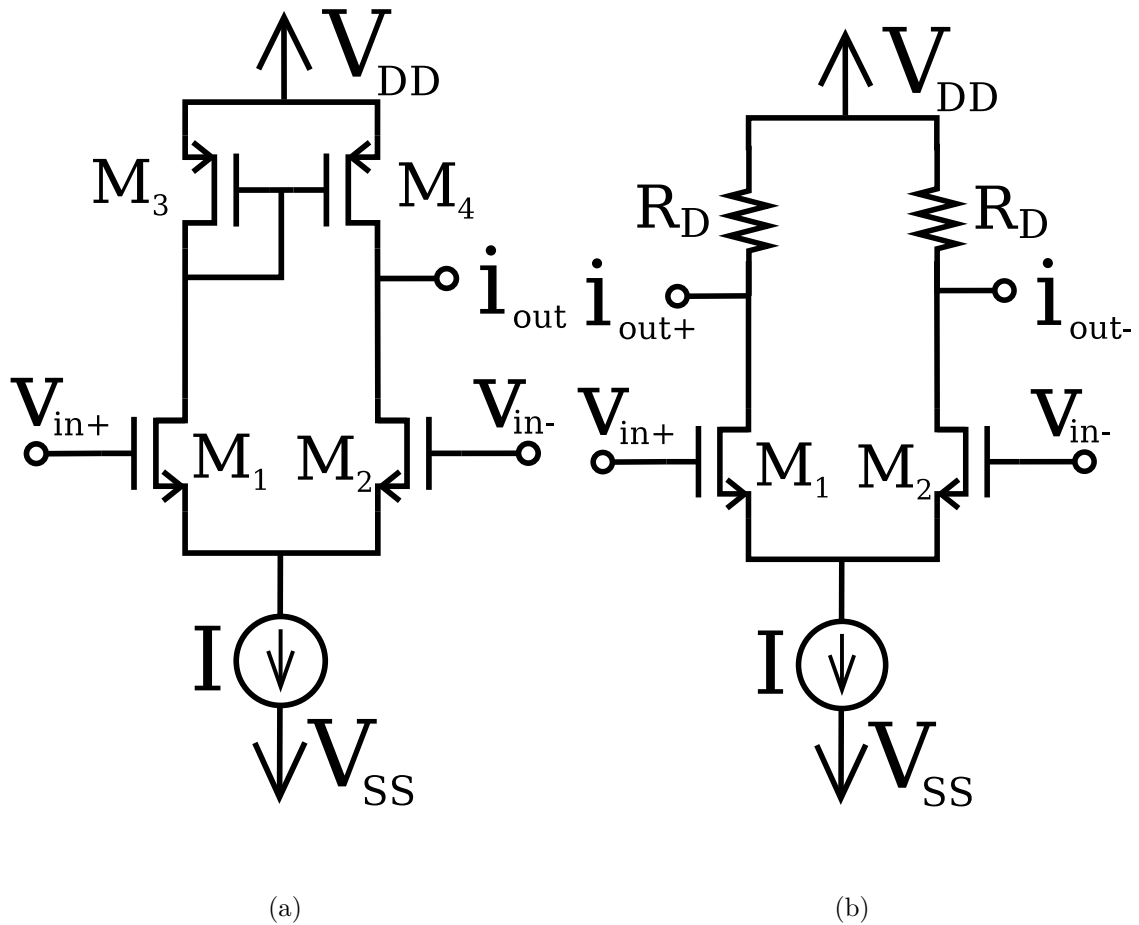


Figure 5.14: Differential pairs used in circuit

when implemented in the actual circuit because the next stage is again connected to a transistor's gate (which is considered an infinite impedance)

Rectifier circuit

Once the signals are aligned, the signal needs to be rectified in preparation for the comparator stage. The ideal rectifier is a diode with a 0 V threshold voltage. This is particularly difficult to implement because the cutoff voltage for this technology is 0.7 V which is approximately the same signal levels used in RF circuits. Because of this, the use of a diode rectifier does not produce the correct result. A new circuit

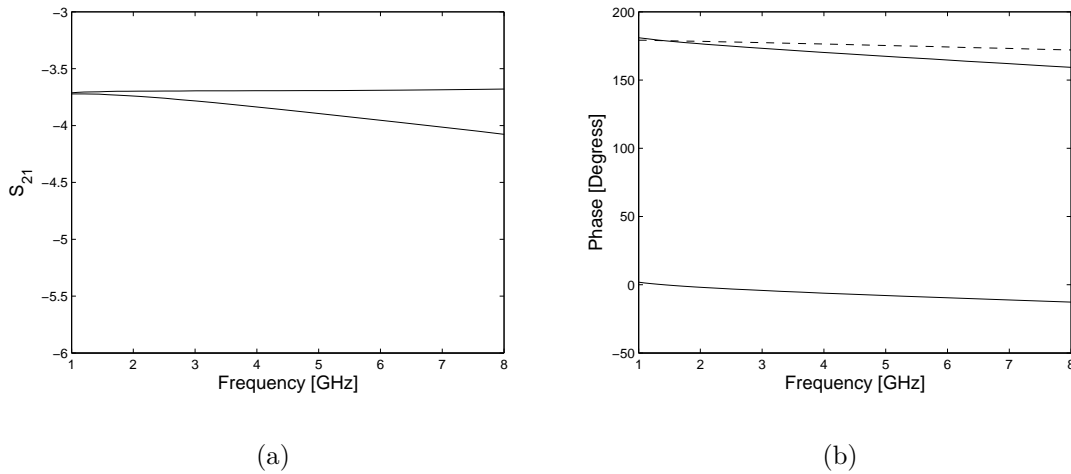


Figure 5.15: Simulated gain and phase of differential amplifier if only one input is excited while the other is grounded

will be needed that emulates a diode rectifier.

A simple common source amplifier is shown in Figure 5.16. Note that in this figure, V_{SS} is replaced with V_{REC} . If V_{REC} is tuned so that the transistor M_1 is on the verge of turning on, then when the input is in the negative region, the output will remain at 0 V. But when the input is positive, the transistor turns on, and the signals is passed. In this manner, a pseudo diode rectifier can be emulated with a 0 V threshold voltage. The result for an ideal rectifier is depicted in Figure 5.13b)iv). When the circuit is laid out and simulated in SpectreRF, the results are seen in Figure 5.17. The dashed line is the original wave and the rectified wave is the solid line. Note that the turning on and turning off points are slightly different and produce some distortion near the 0 V region.

For Figure 5.17, the DC voltages have been manipulated in order to highlight the result of the rectifier. However the slight (0.45 V) DC bias is irrelevant as both the v_{o1} and v_{o2} branches have the same bias and the waveforms are fed into the next stage consisting of a comparator. Because the comparator used here is a simple differential amplifier, the common mode rejection will cancel out any DC bias.

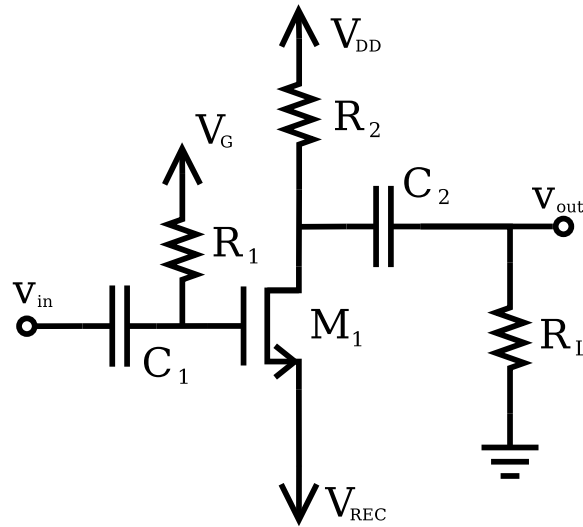


Figure 5.16: A modified common source amplifier with a separate DC source voltage

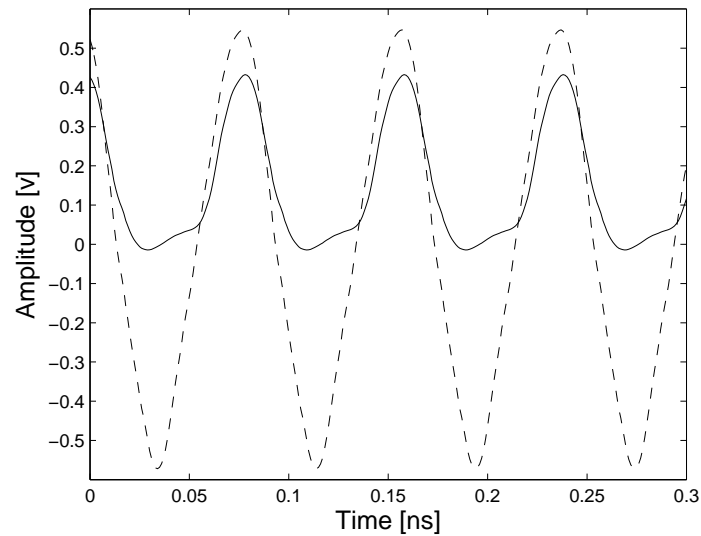


Figure 5.17: Simulations depicting the waveform before and after the rectifier

Comparator

The final stage of the feedback loop is an analog comparator circuit in which the two aligned waveforms are subtracted from each other. The output is connected to the VGAs through an RC filter and is shown in Figure 5.18

As mentioned previously, this system is designed as a dual feedback network in which both branches are both compensated at the same time. Two signals are thus required to compensate the VGAs that adjust the v_{+90} branch and another opposing set of signals to compensate the VGAs at the v_{-90} branch.

Consider a comparator with a differential output: If instead of using the differential output, each output is taken out single endedly, then the two signals are 180° from each other. In other words, each signal is inverted from each other producing a set of opposing signals that is proportional to the difference in the inputs.

$$A_d = \frac{v_{+o}}{v_{+in} - v_{-in}} = \frac{-v_{-o}}{v_{+in} - v_{-in}} = \frac{1}{2}g_m R_D \quad (5.12)$$

$$g_m = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_t) \quad (5.13)$$

$$I_D = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_t)^2 \quad (5.14)$$

Since a differential pair can also function as an analog subtractor, the same differential pair circuit shown previously in Figure 5.13b) is used. The two branches are connected to both v_{in+} and v_{in-} and subtracted from each other. Figure 5.19 depicts the input signals and the corresponding output signals before and after the RC filter. Note that Figure 5.19c) has been exaggerated to highlight the filters smoothing function, in reality, the output from the filter will contain no sinusoid and be strictly DC.

Because the output is a half sinusoid (as a result of the subtraction), further processing needs to be done in order to feed that into the VGAs. A simple RC low pass loop filter is implemented between the stages to smooth out the waveform

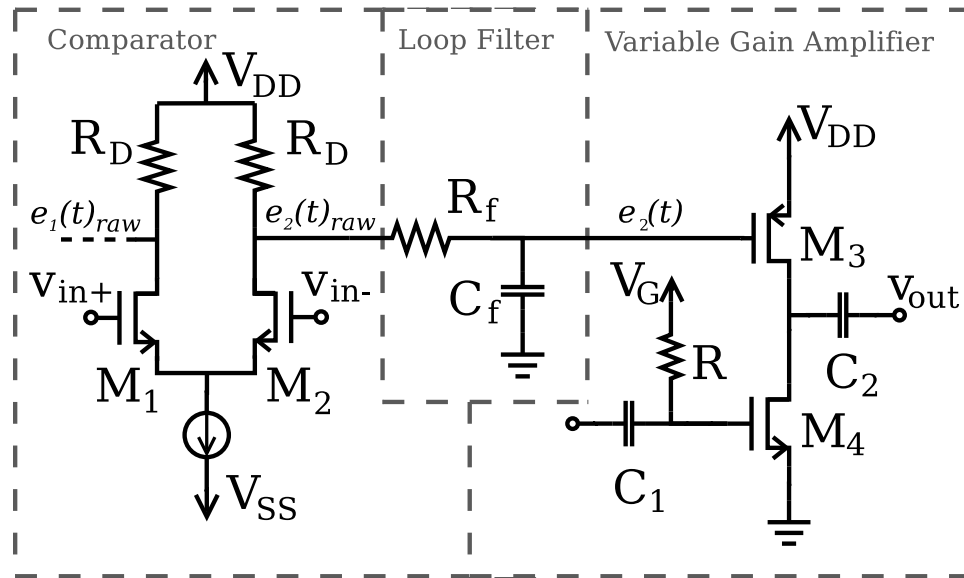


Figure 5.18: Final stages of the feedback loop depicting the interface between the comparator and the VGA

in order to produce a steady DC output. Figure 5.18 depicts the schematic of the comparator circuit connected to an RC filter that is then connected directly to a VGA.

In Section 5.3.1, it was discussed that the VGA operates at a specific operating point and then varies up and down from that voltage point to produce the variable gain. Because the comparator is directly coupled to the VGAs in terms of the DC voltage, the comparator is biased so that the output DC voltage (from the drain of the transistor M_1) is the same as the VGA operating point as seen in Figure 5.20. The accompanying RF (that is subsequently smoothed out) will then produce the additional voltage used to vary the gain. The combination of DC and RF signal used to compose the final output that is fed into the VGAs is seen in Figure 5.19b). The RC filter functions as both a low pass smoothing filter and as a loop filter used to adjust the settling time.

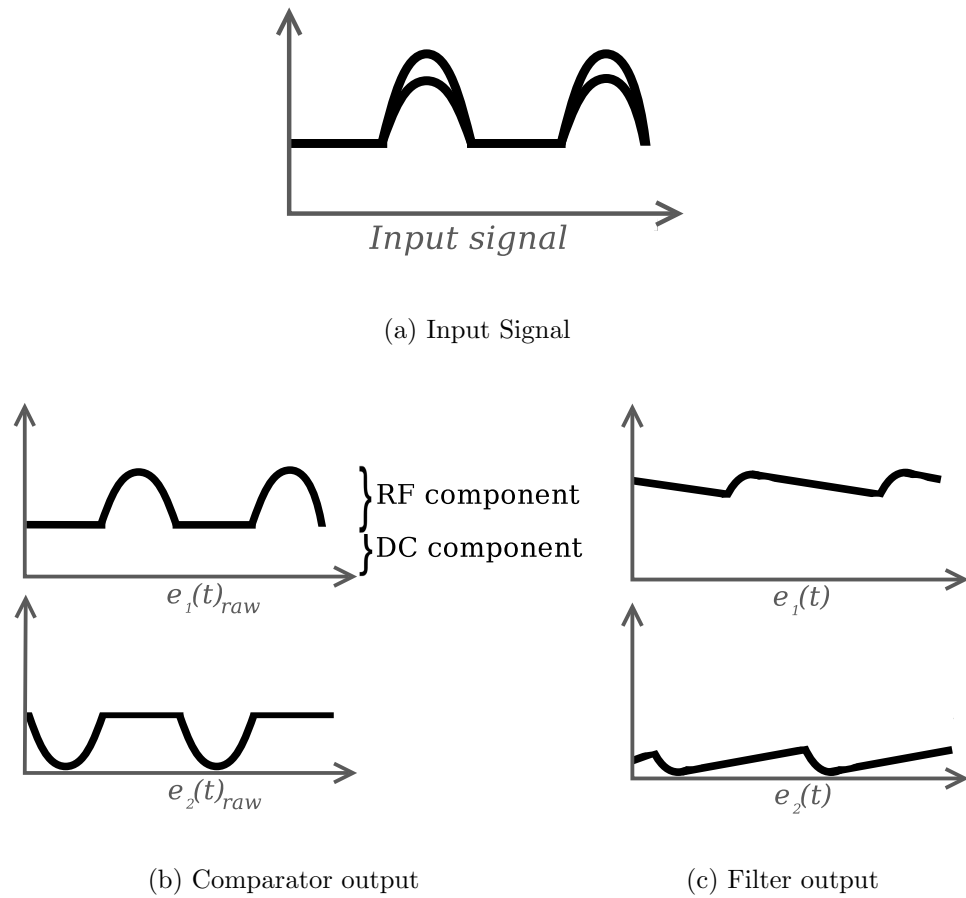


Figure 5.19: Signals associated with comparator stage

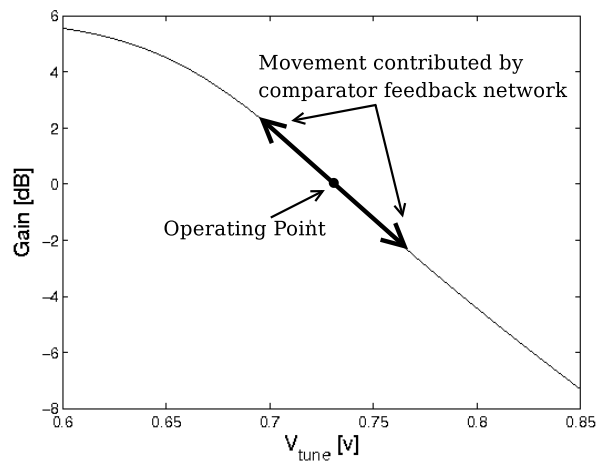


Figure 5.20: Operating point of variable gain amplifier

5.3.3 Circuit Tuning

Resistor Tolerances

There are many parts of this circuit that are particularly sensitive if the models do not exactly match those of the actual manufactured device. One component that is known to have large tolerances is the polysilicon resistors. A diagram of the layout is depicted in Figure 5.21. An N-well is deposited around the device in order to provide RF shielding. To ensure the PN junction formed between the N-well and the P-type substrate is reverse biased, V_{DD} is applied to the N-well. The polysilicon material differs from the one used in the gate of the transistors in that they are not doped to minimize resistance. By varying the length and the width of the polysilicon layer it is possible to produce any resistance required.

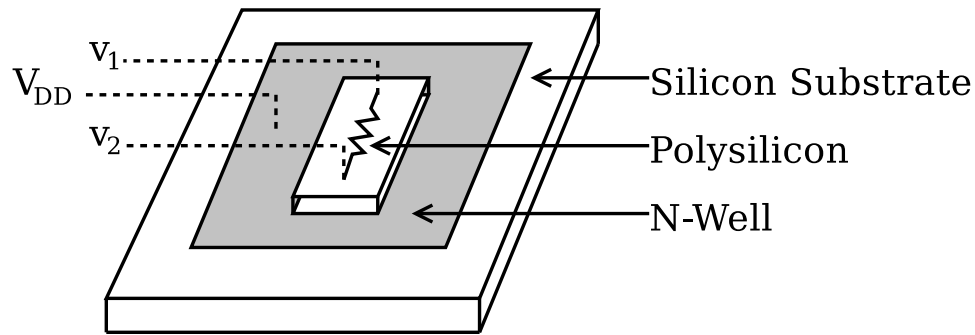


Figure 5.21: Layout of polysilicon resistor

Process variations resulting in different resistances are more profound from one die to another as it depends on the location of the die on the wafer [52]. However within the same die, there is much less variation. Because of the large tolerances, if the polysilicon resistor is used for transistor biasing, then the output is unpredictable and will vary from die to die and not match up with the modeled value. One way to mitigate this issue is to directly control the DC bias points. In a highly sensitive system containing multiple stages variations in resistors is unacceptable, thus direct control of the DC bias point is considered very crucial.

Variable Gain Amplifier Tuning

In order to ensure that the VGAs are biased correctly, the gate of the device is controlled directly instead of being biased using the traditional voltage divider. In the original circuit, Figure 5.10 depicts the use of the voltage V_G . In addition to ensuring that the proper gate bias is applied, it also gives the ability to tune the device if incorrect modeling provides too much or too little gain.

Rectifier Tuning

Because the rectifier circuit is operated at the fringes of the saturation region, it is very sensitive to the operational voltage. Again, in order to mitigate any inconsistent resistor values as well as provide some room for tuning, the negative supply is directly controlled externally in order to provide a way to tune the voltage.

Differential Pair Tuning

Since the differential pair's gain is easily controlled, it was elected to make the gain tunable in order to provide some control over the feedback loop. For example, if there exists a systematic error such that one branch of the circuit has more loss than the other, then the ability to tune the gain of the other branch would have the ability to compensate for such loss. It was described in Section 5.3.2 that there are two differential pairs on both feedback path branches. Since the differential pairs contain a current mirror depicted in Figure 5.22 at the source that, then the current I can easily be tuned by having V_{tune} connected to separate power supplies. In this way, each differential pair's current and subsequently, gain can be independently controlled.

Comparator Tuning

As mentioned in Section 5.3.2, the subsequent VGA stage after the comparator requires that the specific operating point be the same as the DC voltage coming from

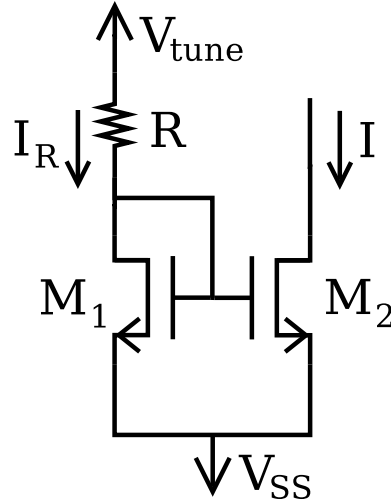


Figure 5.22: Schematic diagram of a current mirror

the comparator. It is trivial to set the DC voltage as it requires only changing the current in the comparator or changing R_D . Again because of inaccurate resistor models there needs to be some way of changing this DC voltage during testing.

An easy way to accomplish this is to separately control the positive supply voltage V_{DD} on the comparator. Because the current is controlled through a current mirror, independent of the positive supply voltage in the comparator. A reduction of the positive supply voltage while the current remains the same will reduce the output DC voltage but still maintain the same circuit operation.

Tuning Pads

Figure 5.23 depicts all the tuning pad connections used in this circuit. The tuning pads are located on the die are labeled as V_G bias, Tune rec, Tune Loop1 and Tune Loop2. These are the gate bias for the VGAs, the rectifier tuning voltage, the tuning voltage for one of the branch's differential pairs and finally the tuning voltage for the other branch's differential pairs. Additionally there are also two more pads: Feedback1 and Feedback2 that are the feedback voltages used to control the VGAs.

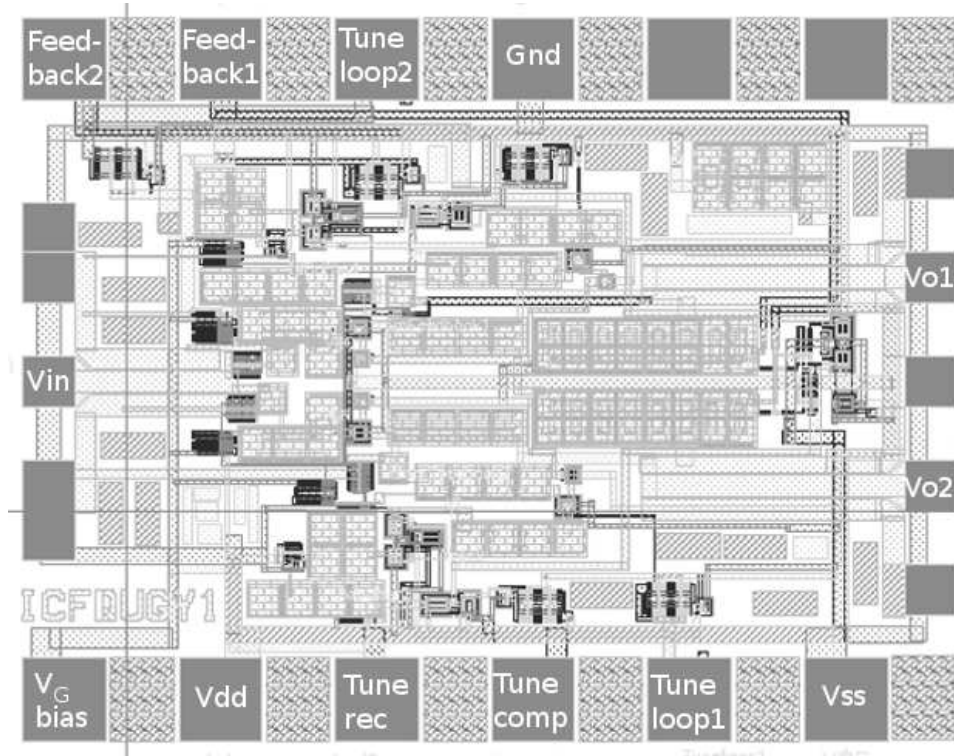


Figure 5.23: Chip layout depicting pad connections

The ability to monitor the feedback voltages will provide insight on what needs to be changed in the circuit.

While the practice for commercial production is to minimize the amount of pad connections and voltages sources, it was decided the effects of the variances in manufacturing coupled with the numerous stages involved in this design made the extra pads a necessity. Further iterations of this design will reduce the amount of external tuning voltages.

5.4 Simulated Results

The completed circuit was simulated in SpectreRF to verify the circuit's operation. In addition many of the circuit's parameters depicted in Figure 5.5 such as the loop gain $K_{AC}f$ and the filter components were adjusted to provide the largest operating

bandwidth and fastest settling time.

5.4.1 Time Domain Results

The circuit simulated at 1.5 GHz is shown below in Figure 5.24. The results of the dual feedback loop that adjusts the variable gain amplifier's gain is seen in Figure 5.24a). As mentioned previously in Section 5.3.1, the operating point at which adjustments are made to is seen here when $t=0$. As the circuit starts up, a typical underdamped response is clearly seen. After a period of approximately $4\ \mu\text{s}$, the system settles into a steady state producing the final compensated response. The result from the output of one of the VGAs as its gain is modified through the feedback loops is shown in Figure 5.24b). Note that since the output is taken over a long period of time, it is impossible to see the actual sinusoid in Figure 5.24.

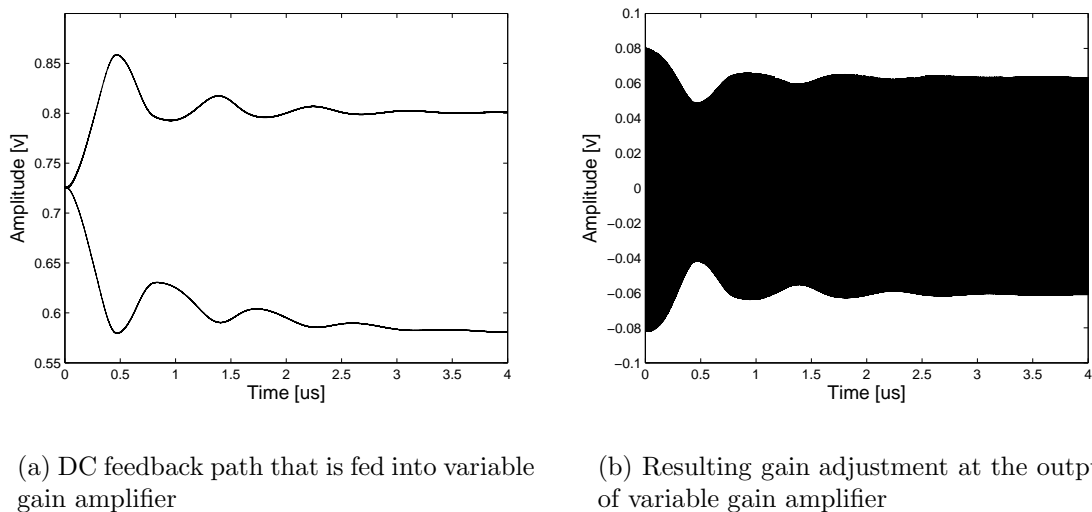
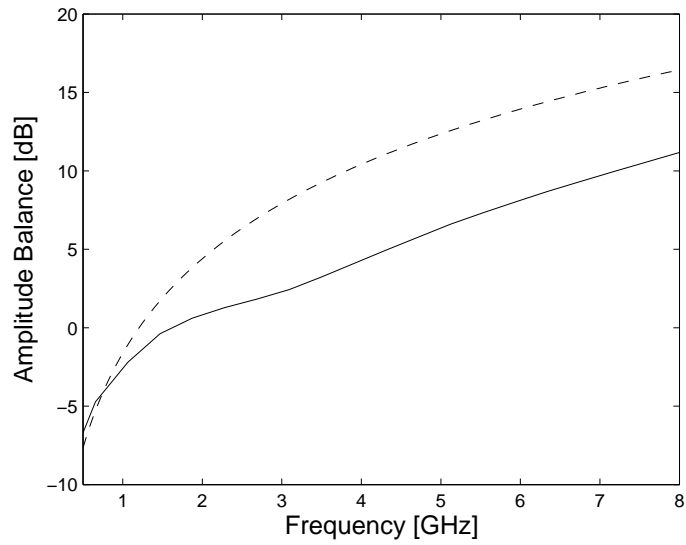
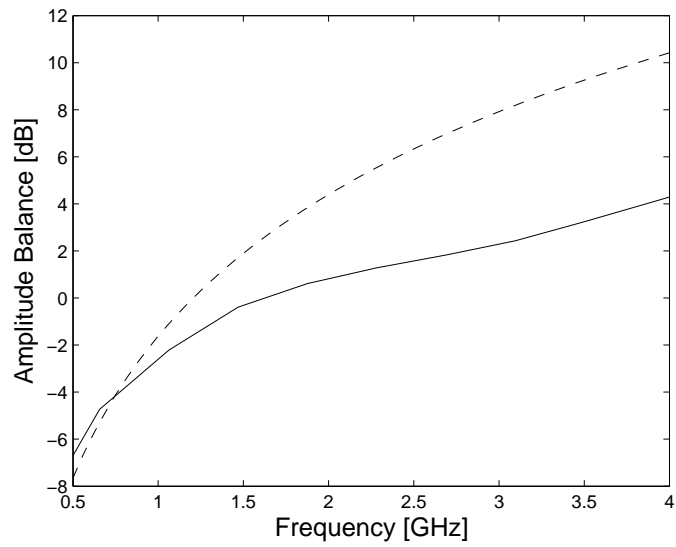


Figure 5.24: Simulated time domain results depicting the feedback settling time of the quadrature generator at 1.5 GHz



(a) Results of a wideband sweep



(b) Zoomed in view of select area of operation

Figure 5.25: Amplitude balance versus frequency for a RC-CR network shown as a dashed line and the feedback quadrature generator shown as a solid line

5.4.2 Wideband Frequency Sweeping Results

Once verification is completed in order to confirm that the feedback loop is functioning, the whole system is swept across a wide frequency band. A fast Fourier transform (FFT) at each frequency point is taken and the output powers at each output is compared to produce a plot of the amplitude balance in Figure 5.25a). The conventional RC-CR network is also plotted to compare the results and is depicted as a dashed line.

The selected area of operation for the device is seen in Figure 5.25b). From this plot, the ± 2 dB bandwidth of the RC-CR network is approximately 700 MHz, while the ± 2 dB of the quadrature generator is a much larger 1.8 GHz. This is a more than double expanded area of operation available to the device. The phase increases slightly from 92.9° at 1.5 GHz to 95.2° at 3 GHz.

5.5 Measured Results

Verification of the circuit was done using a 40 GHz coplanar waveguide (CPW) ground signal ground (GSG) probe for the input and a ground signal ground signal ground probe (GSGSG) of the same type for the outputs on a Wentworth probe station. The Agilent 8510C 50 GHz vector network analyzer that was used to measure the phase and amplitudes was calibrated with a SUSS MicroTec calibration substrate using a full two port short-open-load-through (SOLT) calibration method. As specified from the simulations a -10 dBm output power level was chosen for the network analyzer and the device was swept from 45 MHz to 6 GHz. The overall DC power consumption is found to be 69 mW. A micro-photograph of the circuit is found in Figure 5.26.

As mentioned previously there are 5 separate tuning voltages used to adjust the circuit's operating parameters at the beginning of each sweep in order to produce optimum conditions for maximum bandwidth. In addition two of the the tuning pads

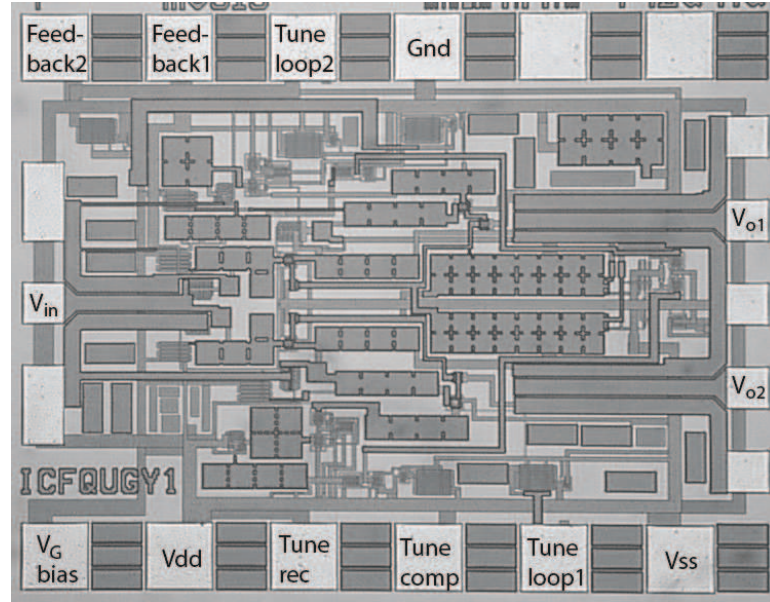
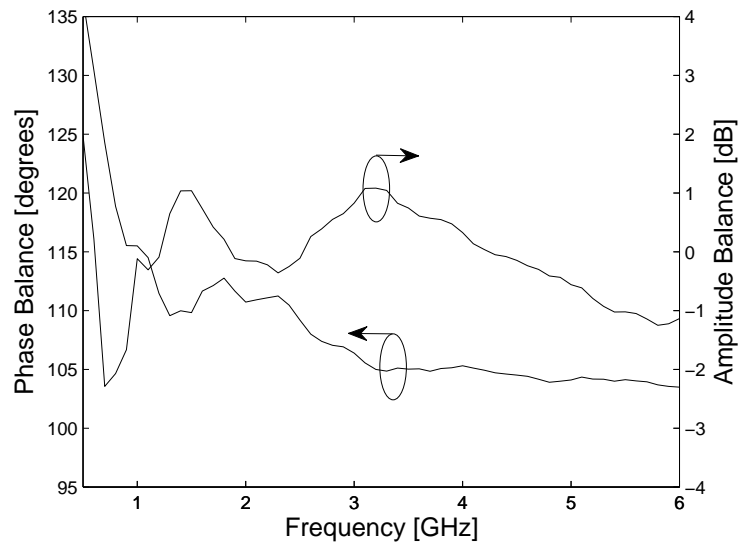


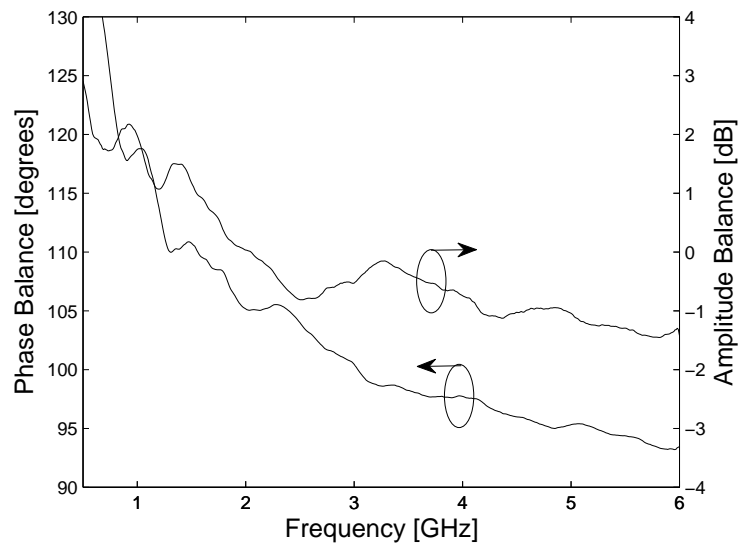
Figure 5.26: Micro-photograph of feedback quadrature generator

were monitored using a low frequency Tektronix TDS 1012 in order to determine the VGA's feedback voltages that are used to compensate the gain. The amplitude balance bandwidth is defined as the bandwidth where the amplitude balance is below ± 1 dB. The results of the sweeps are shown in Figure 5.27. The results of the tuning conditions that yielded the maximum amplitude balance is shown in Figure 5.27a). It shows that the device amplitude balance performs exceptionally from 1 to 6 GHz. However the phase balance varies from 115° to 103° . In order for the feedback loop to work, the comparator tuning voltage (Tune comp) was forced to deviate from the optimum value obtained from simulations producing a phase shift of more than 90° .

Figure 5.28 shows the conditions that were used in order to maximize bandwidth. In the original simulations, the variable gain amplifiers were operated at the range that minimized the amount of phase variations when the gain was tuned. However it was discovered that in order for the feedback loop to function over a large bandwidth, a different operational range was required. As a result the actual operating range forced the phase to deviate from the original 90° phase shift. It is possible to mitigate this

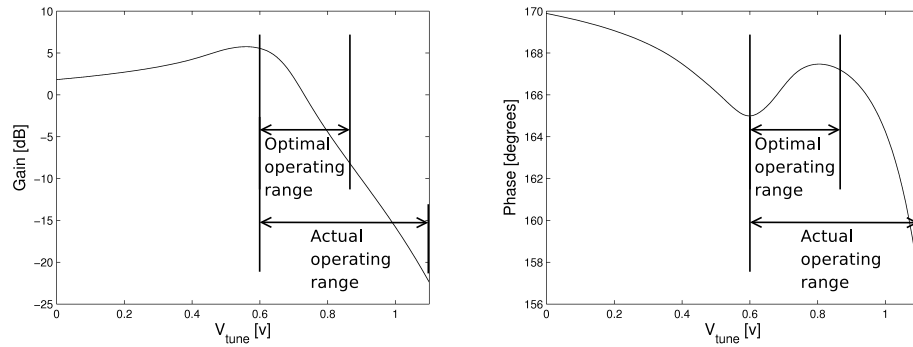


(a) Tuning voltages set to maximize amplitude balance bandwidth



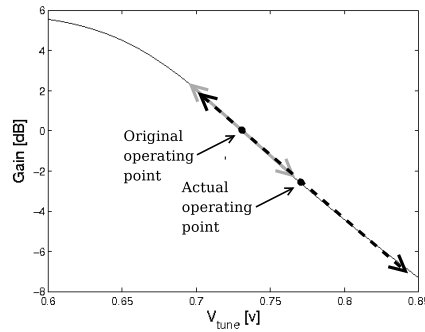
(b) Tuning voltages set to produce 90° phase shift

Figure 5.27: Measured results for quadrature generator



(a) Gain

(b) Phase



(c) Operating point

Figure 5.28: Original and actual operating conditions of the variable gain amplifiers effect by moving the operating point back to its original value. This improves the phase shift to $97 \pm 5^\circ$. However as seen in Figure 5.27b) this improvement becomes a tradeoff as the amplitude balance is reduced to 4 GHz (for an amplitude imbalance of ± 1 dB).

The overall insertion loss for both outputs are shown in Figure 5.29. The RC-CR network itself produces a -6 dB loss because of the input impedance mismatch. At the lower frequencies (≤ 2 GHz), the circuit itself (not including the RC-CR network) produces approximately -2 dB insertion loss. As the frequency increases a combination of the insertion loss of the RC-CR network increasing (as seen in Figure 5.8) and transistor gain rolloff produce a total of -13 dB loss at 6 GHz.

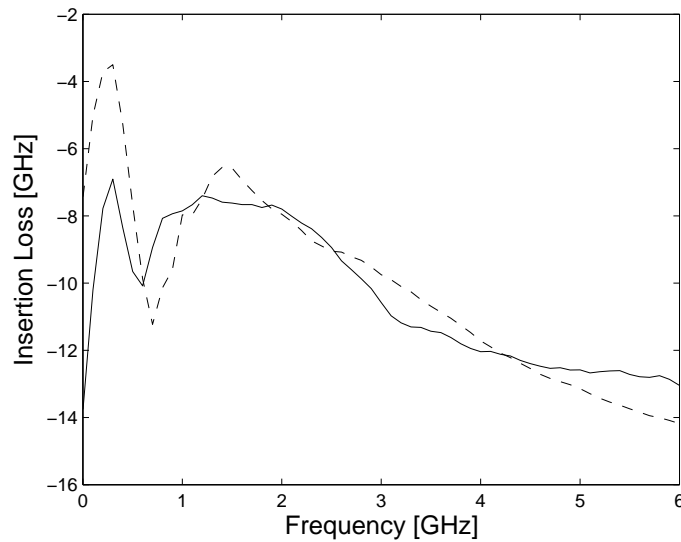


Figure 5.29: Insertion loss for quadrature generator for both outputs

5.6 Conclusions

In this chapter a quadrature wideband balun compensated through a feedback network is presented. The basic RC-CR network used in many circuits lack the ability to function over a large frequency range. This new circuit demonstrates the ability to compensate for an amplitude imbalance through the use of a novel amplitude detector to determine and compare the amplitudes of the two branches. The amount of compensation is then fed into the variable gain amplifiers and the result is that this circuit now has the ability to significantly extend the bandwidth of the original RC-CR network. The experimental results show a device that produces a 4 GHz bandwidth at $97 \pm 5^\circ$ and ± 1 dB amplitude balance. Future work will entail further work on the variable gain amplifiers in order to produce less phase variation when the gain is changed. In addition several improvements on the amplitude detector design can be made to reduce the power consumption as well as reduce the number of stages required. Despite the incorrect phase that is produced, this circuit demonstrates through both simulation and experimentation a completely new conceptual design.

Chapter 6

Conclusions

6.1 Summary

This thesis has discussed the issues with the creation of phase in monolithic microwave integrated circuit (MMIC) designs. The use of precise microstrip layouts in MMIC design are difficult to apply at the radio frequency range because of their large wavelength. As a result the use of lumped components are required. However process variations in the CMOS production produce resistors with very low tolerances.

Low resistivity silicon is used most frequently as it shares most of the same manufacturing process as its digital integrated circuit counterpart which in turn produces significant cost savings. As a result, the inductors that are created have sub par performance because of the low resistivity silicon used. In addition the size of any of these components on these substrates can be a magnitude larger than any active component.

In this thesis, three circuits have been presented that perform over a wide frequency range. In addition, these circuits also demonstrate that neither high Q inductors nor accurate resistors are required for wideband performance.

The balun circuit introduced here used transistors in order to produce the required phase. Consequently to achieve wideband performance, the use of a compensating

capacitor is required. This new circuit is able to increase the bandwidth to over 7.5 GHz. To the best of the author's knowledge, no other circuit found in literature using CMOS technology is able to match the frequency performance while maintaining the same amplitude and phase balance.

Following this, the inductorless quadrature oscillator was designed to operate over a large frequency range. Conventional voltage controlled oscillators often use varactor in order to vary the frequency. It was shown that these varactors have a very limited tuning range. In order to increase the tuning range, the use of a synthetic resonator tank was employed through the use of OTAs. The simulated oscillation bandwidth was shown to be over 1.4 GHz. However due to stability issues, this operating range was reduced when the manufactured device was measured to 100 MHz. Nevertheless, this circuit demonstrates the ability for an artificial OTA resonator to be used in an oscillator.

Finally the quadrature generator was presented. There is a lack of existing circuits that can provide quadrature phase over a large bandwidth. The common RC-CR network was modified with the addition of two VGAs that actively compensate the amplitudes in order to produce wideband performance. The resulting circuit produces quadrature phase over a 4 GHz bandwidth while maintaining an average of $97 \pm 5^\circ$ phase difference and ± 1 dB amplitude balance. The ability to actively compensate the amplitudes has never been applied to such a circuit and this proof of concept design demonstrates the feasibility of such a design.

6.2 Future Work

Several elements can be added to each circuit in order to improve performance or extend the bandwidth. With respect to the balun circuit demonstrated in Chapter 3, the compensating capacitor used was mentioned to be too large. Future work will be done in order to tune the capacitor to produce the bandwidth that is demonstrated

in simulations if the correct capacitance was employed. In addition, fine tuning of the finger size can be employed to further increase the input match.

In the inductorless oscillator circuit, further modeling needs to be done in order to determine to the second and third order equations for the modeling of the system. The addition of separate tuning voltages for each OTA will provide additional control over the oscillation conditions. In this manner the extraneous poles described in the chapter can be either reduced or compensated in order to improve stability.

Finally in the quadrature generator circuit, many refinements can be done in order to improve the design since this is a completely new architecture. The phase performance of this circuit is found to be less than ideal. This is partially due to the VGAs that were employed. In order to increase the phase bandwidth additional work on either the existing VGA architecture needs to be employed or the use of a different VGA that produces the required phase performance is needed. Additionally the amplitude detector and comparator part of the circuit contains numerous stages that will need to be reduced in order to minimize both power consumption and circuit size.

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